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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, HLVD, LCD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f85j94-i-pt

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F97J94
- PIC18F87J94
- PIC18F67J94
- PIC18F96J94
- PIC18F86J94
- PIC18F66J94
- PIC18F95J94
- PIC18F85J94
- PIC18F65J94

This family introduces a new line of low-voltage LCD microcontrollers with Universal Serial Bus (USB). It combines all the main traditional advantage of all PIC18 microcontrollers, namely, high computational performance and a rich feature set at an extremely competitive price point. These features make the PIC18F9XJ94 family a logical choice for many high-performance applications, where cost is a primary consideration.

1.1 Core Features

1.1.1 TECHNOLOGY

All of the devices in the PIC18F9XJ94 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the Internal RC oscillator, power consumption during code execution can be reduced.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **XLP:** An extra low-power Sleep, BOR, RTCC and Watchdog Timer.

1.1.2 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F9XJ94 family offer different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes (HS, MS)
- One External Clock mode (EC)
- A Phase Lock Loop (PLL) frequency multiplier, which allows clock speeds of up to 64 MHz.
- A fast Internal Oscillator (FRC) block that provides an 8 MHz clock (±0.15% accuracy) with Active Clock Tuning (ACT) from USB or SOSC source.
  - Offers multiple divider options from 8 MHz to 500 kHz
  - Frees the two oscillator pins for use as additional general purpose I/O
- A separate Low-Power Internal RC Oscillator (LPRC) (31 kHz nominal) for low-power, timing-insensitive applications.

The internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor (FSCM):** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up (IESO):** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

TABLE 1-4: PIC18FXXJ94 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	100	80	64			
A16/SEG47/AN23/RH0	99	79				
A16				O	DIG	External Memory Address 16.
SEG47				O	Analog	SEG47 output for LCD.
AN23				I	Analog	Analog Input 23.
RH0				I/O	ST/DIG	General purpose I/O pin.
A17/SEG46/AN22/RH1	100	80				
A17				O	DIG	External Memory Address 17.
SEG46				O	Analog	SEG46 output for LCD.
AN22				I	Analog	Analog Input 22.
RH1				I/O	ST/DIG	General purpose I/O pin.
A18/SEG45/AN21/RH2	1	1				
A18				O	DIG	External Memory Address 18.
SEG45				O	Analog	SEG45 output for LCD.
AN21				I	Analog	Analog Input 21.
RH2				I/O	ST/DIG	General purpose I/O pin.
A19/SEG44/AN20/RH3	2	2				
A19				O	DIG	External Memory Address 19.
SEG44				O	Analog	SEG44 output for LCD.
AN20				I	Analog	Analog Input 20.
RH3				I/O	ST/DIG	General purpose I/O pin.
SEG40/AN12/C2INC/RH4	27	22				
SEG40				O	Analog	SEG40 output for LCD.
AN12				I	Analog	Analog Input12.
C2INC				I	Analog	Comparator 2 Input C.
RH4				I/O	ST/DIG	General purpose I/O pin.
SEG41/AN13/C2IND/RH5	26	21				
SEG41				O	Analog	SEG41 output for LCD.
AN13				I	Analog	Analog Input 13.
C2IND				I	Analog	Comparator 2 Input D.
RH5				I/O	ST/DIG	General purpose I/O pin.
SEG42/AN14/C1INC/RH6	25	20				
SEG42				O	Analog	SEG42 output for LCD.
AN14				I	Analog	Analog Input 14.
C1INC				I	Analog	Comparator 1 Input C.
RH6				I/O	ST/DIG	General purpose I/O pin.
SEG43/AN15/RH7	24	19				
SEG43				O	Analog	SEG43 output for LCD.
AN15				I	Analog	Analog Input 15.
RH7				I/O	ST/DIG	General purpose I/O pin.

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
I^2C = I^2C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to V_{DD})

REGISTER 3-7: REFOxCON1: REFERENCE CLOCK OUTPUT CONTROL REGISTER 1

U-0	U-0	U-0	U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
—	—	—	—	ROSEL3	ROSEL2	ROSEL1	ROSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at all Resets	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'
(Reserved for additional ROSEL bits.)

bit 3-0 **ROSEL<3:0>:** Reference Clock Output Source Select bits(1)
Select one of the various clock sources to be used as the reference clock.
0111-1111 = Reserved
0110 = PLL (4/6/8x or 96 MHz)
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = Peripheral clock (reference clock reflects any peripheral clock switching)
0000 = System clock (reference clock reflects any device clock switching)
When PLLDIV<3:0> (CONFIG2H<3:0>) = 1111, ROSEL<3:0> should not be set to '0110'.

Note 1: The ROSEL register field should not be written while the ACTIVE (REFOxCON<0>) bit is '1'; undefined behavior will result.

TABLE 5-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices			Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
POSTINC2	64-pin	80-pin	100-pin	N/A	N/A	N/A
POSTDEC2	64-pin	80-pin	100-pin	N/A	N/A	N/A
PREINC2	64-pin	80-pin	100-pin	N/A	N/A	N/A
PLUSW2	64-pin	80-pin	100-pin	N/A	N/A	N/A
FSR2H	64-pin	80-pin	100-pin	---- xxxx	---- uuuu	---- uuuu
FSR2L	64-pin	80-pin	100-pin	xxxx xxxx	uuuu uuuu	uuuu uuuu
STATUS	64-pin	80-pin	100-pin	---x xxxx	---u uuuu	---u uuuu
TMR0H	64-pin	80-pin	100-pin	0000 0000	uuuu uuuu	uuuu uuuu
TMR0L	64-pin	80-pin	100-pin	xxxx xxxx	uuuu uuuu	uuuu uuuu
T0CON	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
RESERVED	64-pin	80-pin	100-pin	---- ----	---- ----	---- ----
OSCCON	64-pin	80-pin	100-pin	0qqq -qqq	uuuu -uuu	uuuu -uuu
IPR5	64-pin	80-pin	100-pin	-111 -111	-uuu -uuu	-uuu -uuu
IOCF	64-pin	80-pin	100-pin	0000 0000	0000 0000	qqqq qqqq
RCON(4)	64-pin	80-pin	100-pin	0-11 11qq	0-qq qquu	u-qq qquu
TMR1H	64-pin	80-pin	100-pin	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	64-pin	80-pin	100-pin	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	64-pin	80-pin	100-pin	0000 0000	uuuu uuuu	uuuu uuuu
TMR2	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
PR2	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
T2CON	64-pin	80-pin	100-pin	-000 0000	-000 0000	-uuu uuuu
SSP1BUF	64-pin	80-pin	100-pin	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSP1ADD	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
SSP1STAT	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
SSP1CON1	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
SSP1CON2	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
CMSTAT	64-pin	80-pin	100-pin	---- -xxx	---- -uuu	---- -uuu
ADCBUF0H	64-pin	80-pin	100-pin	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCBUF0L	64-pin	80-pin	100-pin	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1H	64-pin	80-pin	100-pin	0--- -000	u--- -uuu	u--- -uuu
ADCON1L	64-pin	80-pin	100-pin	0000 -000	uuuu -uuu	uuuu -uuu
CVRCONH	64-pin	80-pin	100-pin	---0 0000	---u uuuu	---u uuuu
CVRCONL	64-pin	80-pin	100-pin	0000 ---0	uuuu ---u	uuuu ---u

Legend: u = unchanged; x = unknown; - = unimplemented bit, read as '0'; q = value depends on condition. Shaded cells indicate that conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-2 for Reset value for specific condition.

5: Bits 7,6 are unimplemented on 64 and 80-pin devices.

6: If the V_{BAT} is always powered, the DSGPx register values will remain unchanged after the first POR.

REGISTER 11-3: ODCON2: PERIPHERAL OPEN-DRAIN CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP10OD	CCP9OD	CCP8OD	CCP7OD	CCP6OD	CCP5OD	CCP4OD	ECCP3OD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CCP10OD:** CCP10 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 6 **CCP9OD:** CCP9 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 5 **CCP8OD:** CCP8 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 4 **CCP7OD:** CCP7 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 3 **CCP6OD:** CCP6 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 2 **CCP5OD:** CCP5 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 1 **CCP4OD:** CCP4 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 0 **ECCP3OD:** ECCP3 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

11.1.4 ANALOG AND DIGITAL PORTS

Many of the ports multiplex analog and digital functionality, providing a lot of flexibility for hardware designers. PIC18FXXJ94 devices can make any analog pin analog or digital, depending on an application's needs. The ports' analog/digital functionality is controlled by the registers: ANCON1, ANCON2 and ANCON3.

Setting these registers makes the corresponding pins analog and clearing the registers makes the ports digital. For details on these registers, see **Section 22.0 "12-Bit A/D Converter with Threshold Scan"**

11.3 PORTB, LATB and TRISB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding Data Direction and Output Latch registers are TRISB and LATB. All pins on PORTB are digital only.

EXAMPLE 11-2: INITIALIZING PORTB

```
CLRF    PORTB   ; Initialize PORTB by
                ; clearing output
                ; data latches
CLRF    LATB    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISB   ; Set RB<3:0> as inputs
                ; RB<5:4> as outputs
                ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit, RBPU (INTCON2<7>), and setting the associated WPUB bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

The RB<3:2> pins are multiplexed as CTMU edge inputs.

TABLE 11-2: PORTB FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RB0/INT0/CTED13/ RP8/VLCAP1	RB0	0	O	DIG	LATB<0> data output.
		1	I	ST	PORTB<0> data input.
	INT0	1	I	ST	External Interrupt 0 input.
	CTED13	1	I	ST	CTMU Edge 13 input.
	RP8	x	x	DIG	Reconfigurable Pin 8 for PPS-Lite; TRIS must be set to match input/output of module.
	VLCAP1	x	x	ANA	External capacitor connection for LCD module.
RB1/RP9/VLCAP2	RB1	0	O	DIG	LATB<1> data output.
		1	I	ST	PORTB<1> data input.
	RP9	x	x	DIG	Reconfigurable Pin 9 for PPS-Lite; TRIS must be set to match input/output of module.
	VLCAP2	x	x	ANA	External capacitor connection for LCD module.
RB2/CTED1/RP14/ SEG9	RB2	0	O	DIG	LATB<2> data output.
		1	I	ST	PORTB<2> data input.
	CTED1	1	I	ST	CTMU Edge 1 input.
	RP14	x	x	DIG	Reconfigurable Pin 14 for PPS-Lite; TRIS must be set to match input/output of module.
	SEG9	0	O	ANA	LCD Segment 9 output; disables all other pin functions.
RB3/CTED2/RP7/ SEG10	RB3	0	O	DIG	LATB<3> data output.
		1	I	ST	PORTB<3> data input.
	CTED2	1	I	ST	CTMU Edge 2 input.
	RP7	x	x	DIG	Reconfigurable Pin 7 for PPS-Lite; TRIS must be set to match input/output of module.
	SEG10	0	O	ANA	LCD Segment 10 output; disables all other pin functions.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

13.14 Configuring the LCD Module

To configure the LCD module.

1. Select the frame clock prescale using bits, LP<3:0> (LCDPS<3:0>).
2. Configure the appropriate pins to function as segment drivers using the LCDSEx registers.
3. If using the internal reference resistors for biasing, enable the internal reference ladder and:
   - Define the Mode A and Mode B interval by using the LRLAT<2:0> bits (LCDRL<2:0>)
   - Define the low, medium or high ladder for Mode A and Mode B by using the LRLAP<1:0> bits (LCDRL<7:6>) and the LRLBP<1:0> bits (LCDRL<5:4>), respectively
   - Set the VLCDxPE bits and enable the LCDIRE bit (LCDREF<7>)
4. Configure the following LCD module functions using the LCDCON register:
   - Multiplex and Bias mode – LMUX<2:0> bits
   - Timing Source – CS<1:0> bits
   - Sleep mode – SLPEN bit
5. Write initial values to the Pixel Data registers, LCDDATA0 through LCDDATA63.
6. Clear the LCD Interrupt Flag, LCDIF, and if desired, enable the interrupt by setting bit, LCDIE.
7. Enable the LCD module by setting the LCDEN bit (LCDCON<7>)

13.15 Operation During Sleep

The LCD module can operate during Sleep. The selection is controlled by the SLPEN bit (LCDCON<6>). Setting the SLPEN bit allows the LCD module to go to Sleep. Clearing the SLPEN bit allows the module to continue to operate during Sleep.

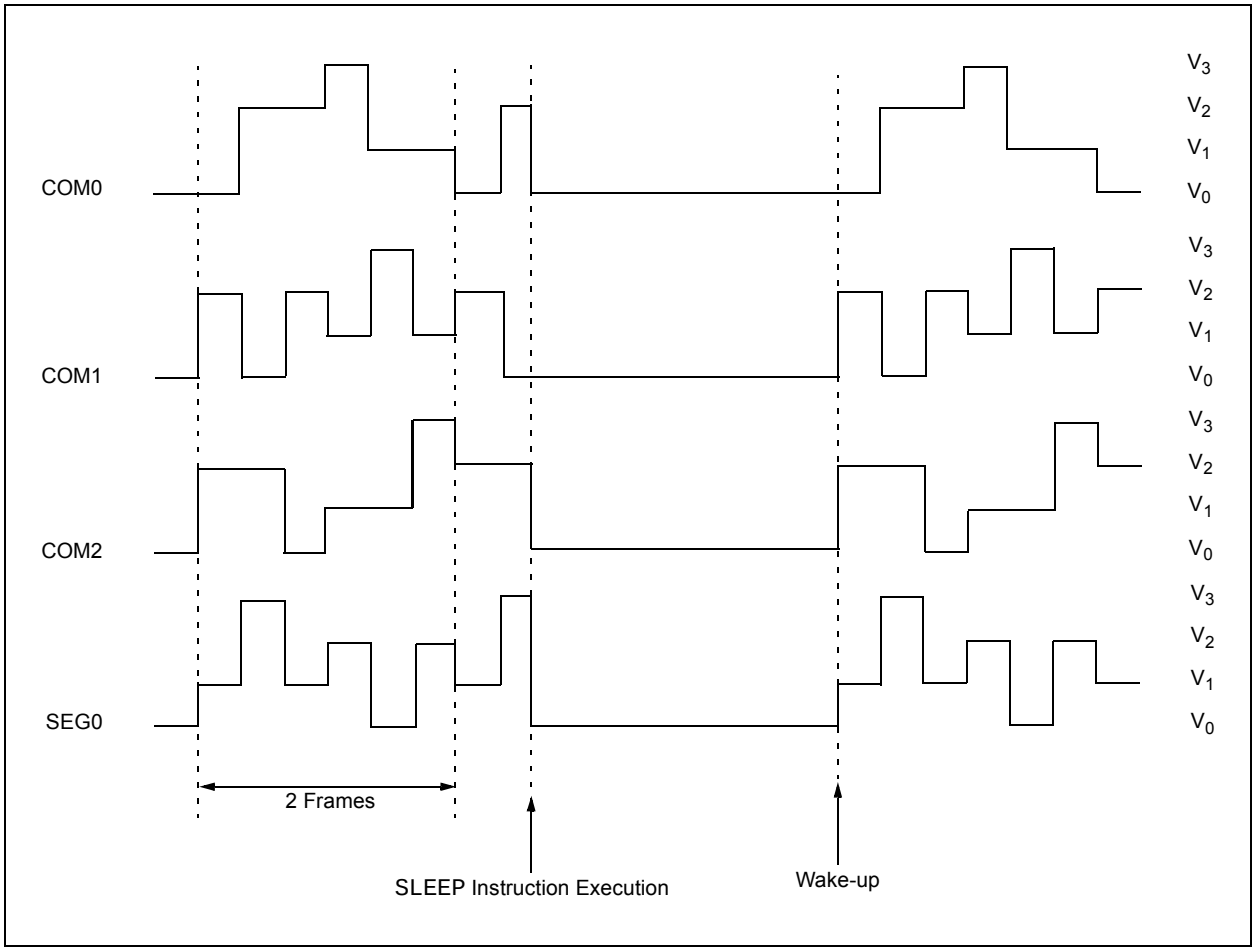
If a SLEEP instruction is executed and SLPEN = 1, the LCD module will cease all functions and go into a very Low-Current Consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 13-23 shows this operation.

The LCD module current consumption will not decrease in this mode, but the overall consumption of the device will be lower due to shut down of the core and other peripheral functions.

To ensure that no DC component is introduced on the panel, the SLEEP instruction should be executed immediately after an LCD frame boundary. The LCD interrupt can be used to determine the frame boundary. See **Section 13.13 “LCD Interrupts”** for the formulas to calculate the delay.

If a SLEEP instruction is executed and SLPEN = 0, the module will continue to display the current contents of the LCDDATA registers. The LCD data cannot be changed.

FIGURE 13-23: SLEEP ENTRY/EXIT WHEN SLPEN = 1 OR CS<1:0> = 00.



Register 17-3: RTCCON2: RTC CONFIGURATION REGISTER 2(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCEN(1)	PWCPOL(1)	PWCCPRE(1)	PWCSPRE(1)	RTCCLKSEL1	RTCCLKSEL0	RTCSECSEL1	RTCSECSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **PWCEN:** Power Control Enable bit(1)
- 1 = Power control is enabled
- 0 = Power control is disabled

bit 6 **PWCPOL:** Power Control Polarity bit(1)
- 1 = Power control output is active-high
- 0 = Power control output is active-low

bit 5 **PWCCPRE:** Power Control/Stability Prescaler bits(1)
- 1 = PWC stability window clock is divide-by-2 of source RTCC clock
- 0 = PWC stability window clock is divide-by-1 of source RTCC clock

bit 4 **PWCSPRE:** Power Control Sample Prescaler bits(1)
- 01 =PWC sample window clock is divide-by-2 of source RTCC clock
- 00 =PWC sample window clock is divide-by-1 of source RTCC clock

bit 3-2 **RTCCLKSEL<1:0>:** RTCC Clock Select bits
Determines the source of the internal RTCC clock, which is used for all RTCC timer operations.
- 11 =60 Hz Powerline
- 10 =50 Hz Powerline
- 01 =INTOSC
- 00 =SOSC

bit 1-0 **RTSECSEL<1:0>:** RTCC Seconds Clock Output Select bit
- 11 =Power control
- 10 =RTCC source clock is selected for the RTCC pin (pin can be LF-INTOSC or SOSC, depending on the RTCOSC (CONFIG3L<1>) bit setting
- 01 =RTCC seconds clock is selected for the RTCC pin
- 00 =RTCC alarm pulse is selected for the RTCC pin

Note 1: The RTCCON2 register is only affected by a POR.

REGISTER 17-7: YEAR: YEAR VALUE REGISTER(1) (RTCVALL when RTCPTR<1:0> = 11)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 17-8: MONTH: MONTH VALUE REGISTER(1) (RTCVALH when RTCPTR<1:0> = 10)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

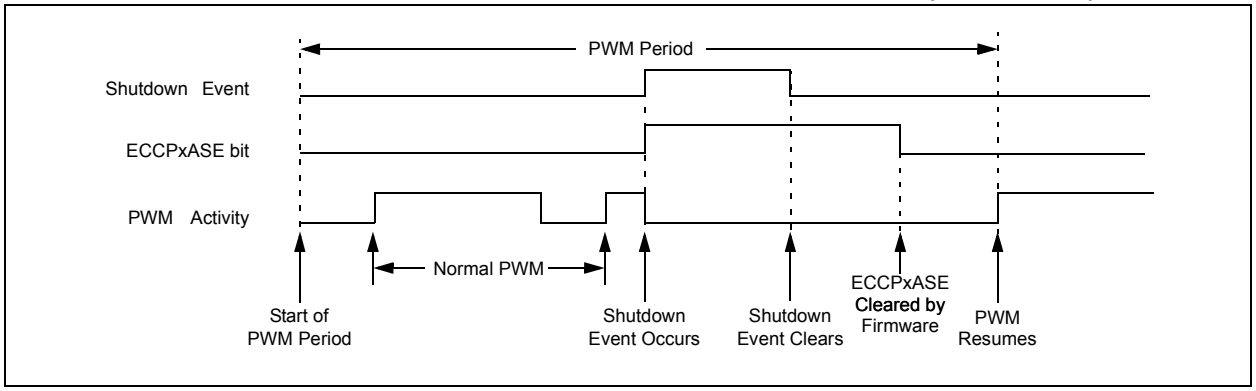
bit 7-5 **Unimplemented:** Read as '0'

bit 4 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.

bit 3-0 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

FIGURE 18-12: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PxRSEN = 0)



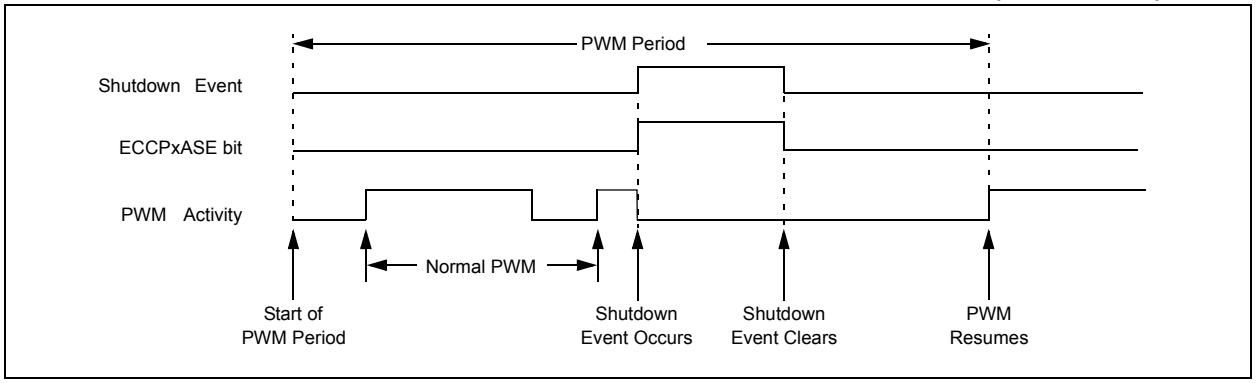
18.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PxRSEN bit (ECCPxDEL<7>).

If auto-restart is enabled, the ECCPxASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPxASE bit will be cleared via hardware and normal operation will resume.

The module will wait until the next PWM period begins, however, before re-enabling the output pin. This behavior allows the auto-shutdown with auto-restart features to be used in applications based on current mode of PWM control.

FIGURE 18-13: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PxRSEN = 1)



EXAMPLE 20-2: 512-BYTE SPI MASTER MODE INIT AND TRANSFER (CONTINUED)

```
;           udata   0x500
;DestBuf    res     0x200               ;Let's reserve 0x500-0x6FF for use as our SPI
;                                       ;receive data buffer in this example
;SrcBuf     res     0x200               ;Lets reserve 0x700-0x8FF for use as our SPI
;                                       ;transmit data buffer in this example

PrepareTransfer:
            movlw   HIGH(DestBuf)       ;Get high byte of DestBuf address (0x05)
            movwf   RXADDRH             ;Load upper four bits of the RXADDR register
            movlw   LOW(DestBuf)        ;Get low byte of the DestBuf address (0x00)
            movwf   RXADDRL             ;Load lower eight bits of the RXADDR register

            movlw   HIGH(SrcBuf)        ;Get high byte of SrcBuf address (0x07)
            movwf   TXADDRH             ;Load upper four bits of the TXADDR register
            movlw   LOW(SrcBuf)         ;Get low byte of the SrcBuf address (0x00)
            movwf   TXADDRL             ;Load lower eight bits of the TXADDR register

            movlw   0x01                ;Lets move 0x200 (512) bytes in one DMA xfer
            movwf   DMABCH              ;Load the upper two bits of DMABC register
            movlw   0xFF                ;Actual bytes transferred is (DMABC + 1), so
            movwf   DMABCL              ;we load 0x01FF into DMABC to xfer 0x200 bytes

BeginXfer:
            bsf     DMACON1, DMAEN      ;The SPI DMA module will now begin transferring
                                        ;the data taken from SrcBuf, and will store
                                        ;received bytes into DestBuf.

    ;Execute whatever                   ;CPU is now free to do whatever it wants to
                                        ;and the DMA operation will continue without
                                        ;intervention, until it completes.

                                        ;When the transfer is complete, the SSP2IF flag in
                                        ;the PIR3 register will become set, and the DMAEN bit
                                        ;is automatically cleared by the hardware.
                                        ;The DestBuf (0x500-0x7FF) will contain the received
                                        ;data.  To start another transfer, firmware will need
                                        ;to reinitialize RXADDR, TXADDR, DMABC and then
                                        ;set the DMAEN bit.
```

REGISTER 22-5: ADCON1L: A/D CONTROL REGISTER 1 LOW

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **SSRC<3:0>:** Sample Clock Source Select bits

1111-1110 = Reserved, do not use
1101 = CMP1
1100 = Reserved, do not use
1011 = CCP4
1010 = ECCP3
1001 = ECCP2
1000 = ECCP1
0111 = The SAMP bit is cleared after SAMC<4:0> number of TAD clocks following the SAMP bit being set (Auto-Convert mode); no extended sample time is present
0110 = Unimplemented
0101 = TMR1
0100 = CTMU
0011 = TMR5
0010 = TMR3
0001 = INT0
0000 = The SAMP bit must be cleared by software to start conversion

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** A/D Sample Auto-Start bit

1 = Sampling begins immediately after last conversion; SAMP bit is auto-set
0 = Sampling begins when SAMP bit is manually set

bit 1 **SAMP:** A/D Sample Enable bit

1 = A/D Sample-and-Hold amplifiers are sampling
0 = A/D Sample-and-Hold amplifiers are holding

bit 0 **DONE:** A/D Conversion Status bit

1 = A/D conversion cycle has completed
0 = A/D conversion has not started or is in progress

REGISTER 22-16: ADCHIT0H: A/D SCAN COMPARE HIT REGISTER 0 HIGH (HIGH WORD)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH15	CHH14	CHH13	CHH12	CHH11	CHH10	CHH9	CHH8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **CHH<15:8>:** A/D Compare Hit bits

If CM<1:0> = 11:

1 = A/D Result Buffer n has been written with data or a match has occurred

0 = A/D Result Buffer n has not been written with data

For all other values of CM<1:0>:

1 = A match has occurred on A/D Result Channel n

0 = No match has occurred on A/D Result Channel n

REGISTER 22-17: ADCHIT0L: A/D SCAN COMPARE HIT REGISTER 0 LOW (LOW WORD)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH7	CHH6	CHH5	CHH4	CHH3	CHH2	CHH1	CHH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **CHH<7:0>:** A/D Compare Hit bits

If CM<1:0> = 11:

1 = A/D Result Buffer n has been written with data or a match has occurred

0 = A/D Result Buffer n has not been written with data

For all other values of CM<1:0>:

1 = A match has occurred on A/D Result Channel n

0 = No match has occurred on A/D Result Channel n

24.2 Voltage Reference Accuracy/Error

The full range of voltage reference cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 24-1) keep CVREF from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the CVREF output changes with fluctuations in that source. The tested absolute accuracy of the voltage reference can be found in **Section 30.0 "Electrical Specifications"**.

24.3 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the CVRCON register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

24.4 Effects of a Reset

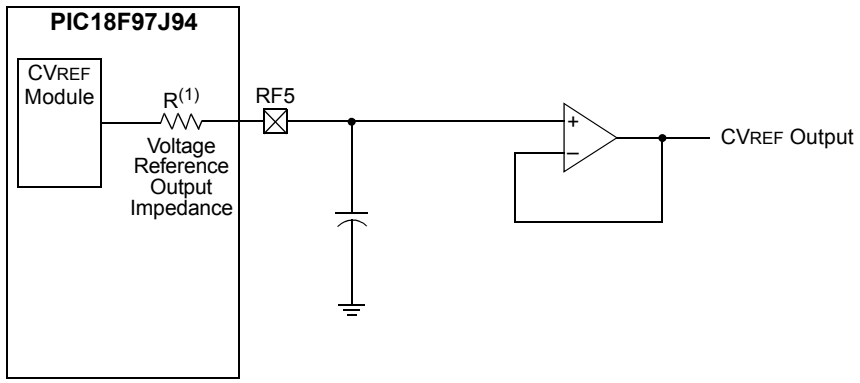
A device Reset disables the voltage reference by clearing bit, CVREN (CVRCONL<7>). This Reset also disconnects the reference from the RF5 pin by clearing bit, CVROE (CVRCONL<6>).

24.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RA0 pin if the CVROE bit is set. Enabling the voltage reference output onto RA0, when it is configured as a digital input, will increase current consumption. Connecting RA0 as a digital output with CVRSS enabled will also increase current consumption.

The RA0 pin can be used as a simple D/A output with limited drive capability. Due to the limited current drive capability, a buffer must be used on the voltage reference output for external connections to VREF. Figure 24-2 shows an example buffering technique.

FIGURE 24-2: COMPARATOR VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



Note 1: R is dependent upon the Comparator Voltage Reference bits, CVRCONH<4:0>, CVRCONL<5:4> and CVRCONL<0>.

27.5.3 USB ERROR INTERRUPT STATUS REGISTER (UEIR)

The USB Error Interrupt STATUS register (Register 27-9) contains the flag bits for each of the error sources within the USB peripheral. Each of these sources is controlled by a corresponding interrupt enable bit in the UEIE register. All of the USB error flags are ORed together to generate the USB Error Interrupt Flag (UERRIF) at the top level of the interrupt logic.

Each error bit is set as soon as the error condition is detected. Thus, the interrupt will typically not correspond with the end of a token being processed.

Once an interrupt bit has been set by the SIE, it must be cleared in software by writing a '0'.

Register 27-9: UEIR: USB ERROR INTERRUPT STATUS REGISTER (ACCESS F63h)

R/C-0	U-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
BTSEF	—	—	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **BTSEF:** Bit Stuff Error Flag bit
1 = A bit stuff error has been detected
0 = No bit stuff error has been detected

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **BTOEF:** Bus Turnaround Time-out Error Flag bit
1 = Bus turnaround time-out has occurred (more than 16 bit times of Idle from previous EOP elapsed)
0 = No bus turnaround time-out has occurred

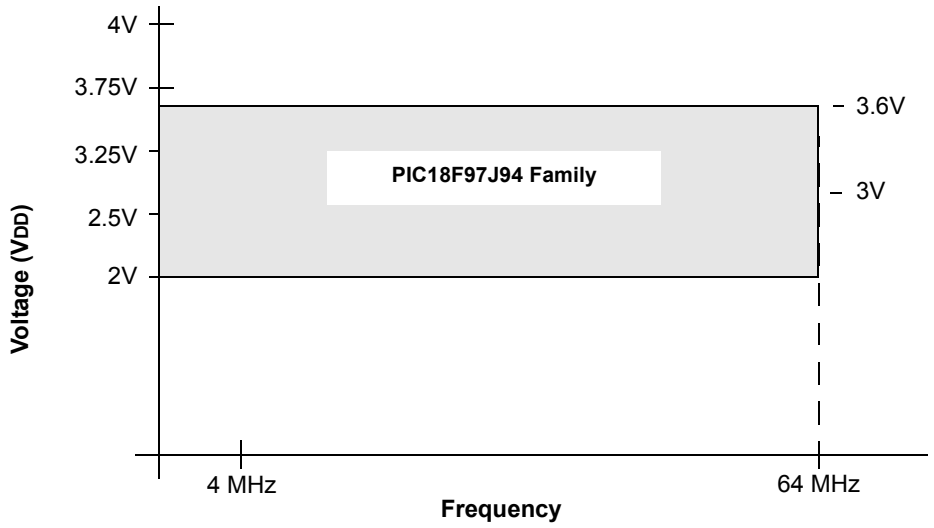
bit 3 **DFN8EF:** Data Field Size Error Flag bit
1 = The data field was not an integral number of bytes
0 = The data field was an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
1 = The CRC16 failed
0 = The CRC16 passed

bit 1 **CRC5EF:** CRC5 Host Error Flag bit
1 = The token packet was rejected due to a CRC5 error
0 = The token packet was accepted

bit 0 **PIDEF:** PID Check Failure Flag bit
1 = PID check failed
0 = PID check passed

FIGURE 30-1: VOLTAGE-FREQUENCY GRAPH, REGULATOR DISABLED (INDUSTRIAL)(1,2)



Note 1: When the USB module is enabled, VUSB3V3 and VDD should be connected together and provided 3.0V-3.6V. When the USB module is not enabled, VUSB3V3 and VDD should still be connected together.

2: VCAP (nominal on-chip regulator output voltage) = 1.8V.

TABLE 30-2: DC CHARACTERISTICS: POWER-DOWN AND SUPPLY CURRENT PIC18FXXJ94 (INDUSTRIAL)

PIC18FXXJ94 Family (Industrial)				**Standard Operating Conditions: 2V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial		
Param No.	**Typ.(1)**	**Max.**	**Units**	**Conditions**		
DC60	3.7	7.0	µA	-40°C	2.0V	Sleep(2)
	3.7	7.0	µA	+25°C		
	5.0	9.0	µA	+60°C		
	9.0	18	µA	+85°C		
	3.7	8.0	µA	-40°C	3.3V	
	3.7	8.0	µA	+25°C		
	5.0	11.0	µA	+60°C		
	10	20	µA	+85°C		
DC61	0.07	0.55	µA	-40°C	2.0V	Retention Sleep or Retention Deep Sleep(3)
	0.09	0.55	µA	+25°C		
	2.0	3.2	µA	+60°C		
	7.0	8.5	µA	+85°C		
	0.10	0.65	µA	-40°C	3.3V	
	0.15	0.65	µA	+25°C		
	2.0	3.5	µA	+60°C		
	7.2	9.0	µA	+85°C		
DC70	0.06	0.5	µA	-40°C	2.0V	Deep Sleep
	0.08	0.5	µA	+25°C		
	0.21	0.8	µA	+60°C		
	0.41	1.5	µA	+85°C		
	0.09	0.6	µA	-40°C	3.3V	
	0.11	0.6	µA	+25°C		
	0.42	1.2	µA	+60°C		
	0.8	4.8	µA	+85°C		
	0.4	3.0	µA	-40°C TO +85°C	0	RTCC with VBAT mode (LPRC or SOSC)(4)

Note 1: Data in the Typical column is at 3.3V, 25°C; typical parameters are for design guidance only and are not tested.

2: Retention regulator is disabled; SRETEN (RCON4<4>= 0), $\overline{\text{RETEN}}$ (CONFIG7L<0>= 1).

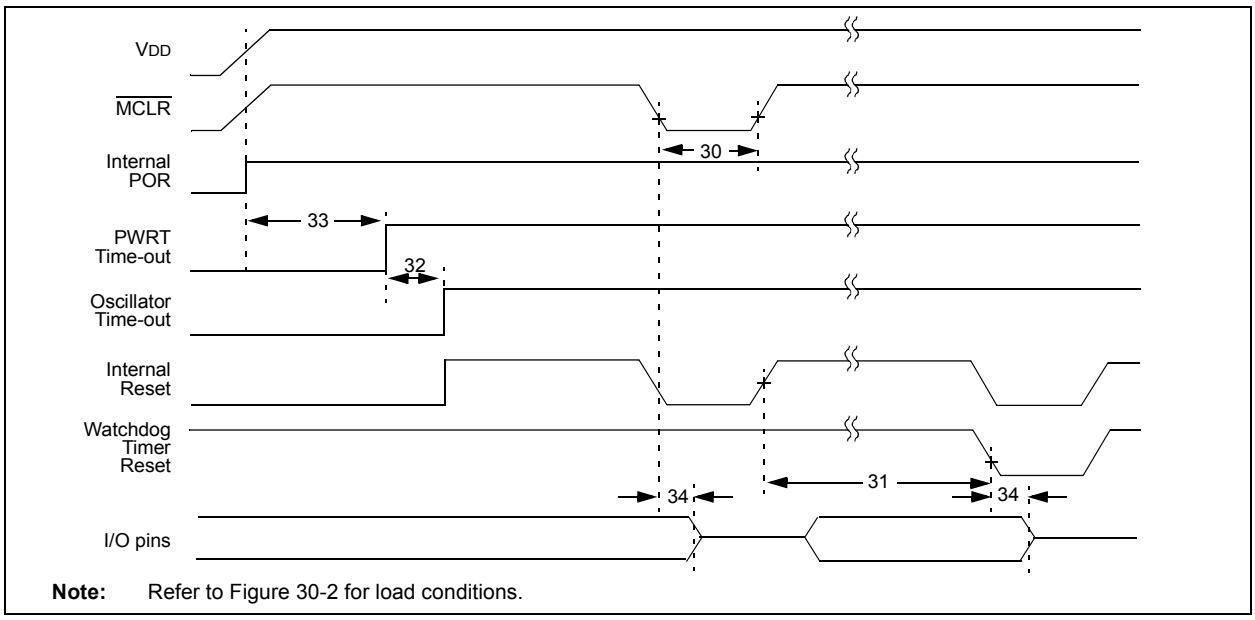
3: Retention regulator is enabled; SRETEN (RCON4<4> = 1), $\overline{\text{RETEN}}$ (CONFIG7L<0> = 0).

4: VBAT pin is connected to the battery and RTCC is running with VDD = 0.

TABLE 30-3: DC CHARACTERISTICS: POWER-DOWN AND SUPPLY CURRENT PIC18F97J94 FAMILY (INDUSTRIAL)

Param No.	**Device**	**Typ.**	**Max.**	**Units**	**Conditions**		
	Supply Current (IDD)						
	All Devices	22	55	µA	-40°C to +85°C	VDD = 2.0V	FOSC = 31 kHz, **RC_RUN**
		23	56	µA	-40°C to +85°C	VDD = 3.3V	
		21	54	µA	-40°C to +85°C	VDD = 2.0V	FOSC = 31 kHz, **RC_IDLE**
		22	55	µA	-40°C to +85°C	VDD = 3.3V	

FIGURE 30-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 30-2 for load conditions.

FIGURE 30-8: BROWN-OUT RESET TIMING

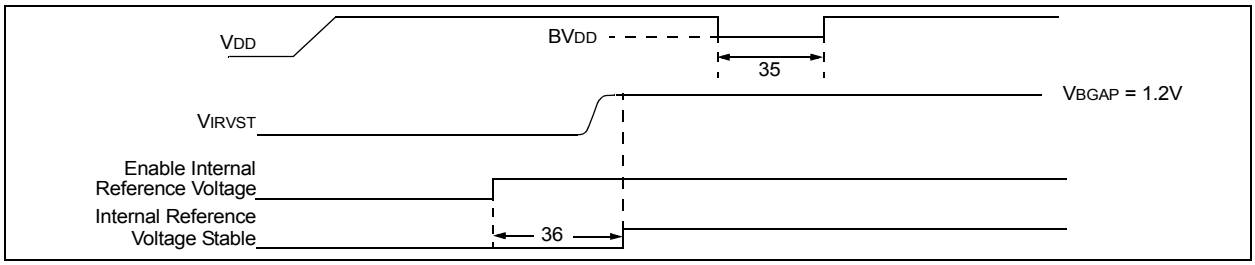
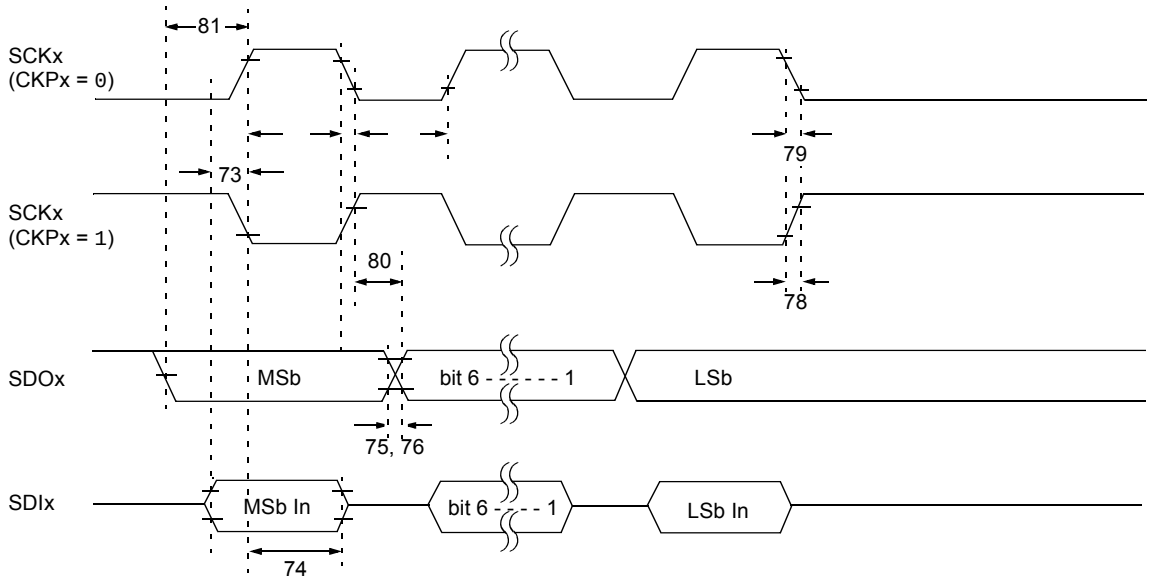


FIGURE 30-13: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)



Note: Refer to Figure 30-2 for load conditions.

TABLE 30-31: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
73	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	20	—	ns	
73A	TB2B	Last Clock Edge of Byte 1 to the 1st Clock Edge of Byte 2	1.5 TCY + 40	—	ns	
74	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	40	—	ns	
75	TDOR	SDOx Data Output Rise Time	—	25	ns	
76	TDOF	SDOx Data Output Fall Time	—	25	ns	
78	TSCR	SCKx Output Rise Time (Master mode)	—	25	ns	
79	TSCF	SCKx Output Fall Time (Master mode)	—	25	ns	
80	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid after SCKx Edge	—	50	ns	
81	TDOV2SCH, TDOV2SCL	SDOx Data Output Setup to SCKx Edge	TCY	—	ns	