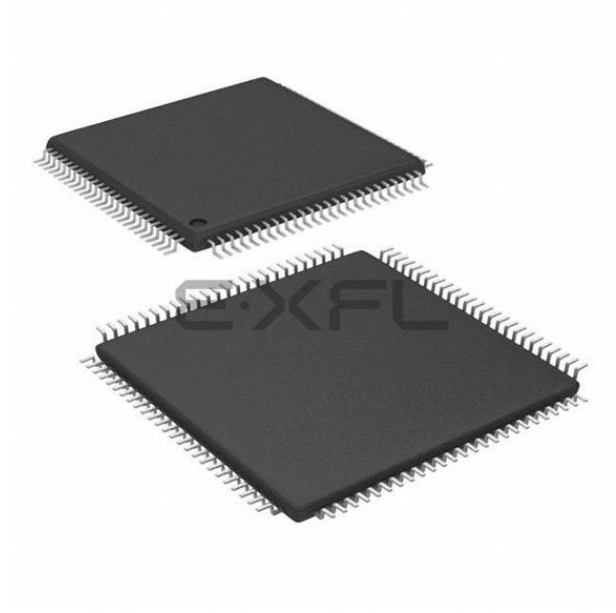
Microchip Technology - PIC18F95J94T-I/PF Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, HLVD, LCD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f95j94t-i-pf

1.1.3 MEMORY OPTIONS

The PIC18F9XJ94 family provides ample room for application code, from 32 Kbytes to 128 Kbytes of code space. The Flash cells for program memory are rated to last up to 20,000 erase/write cycles. Data retention without refresh is conservatively estimated to be greater than 10 years.

The Flash program memory is readable and writable. During normal operation, the PIC18F9XJ94 family also provides plenty of room for dynamic application data with up to 3,578 bytes of data RAM.

1.1.4 UNIVERSAL SERIAL BUS (USB)

Devices in the PIC18F9XJ94 family incorporate a fully-featured USB communications module with a built-in transceiver that is compliant with the USB Specification Revision 2.0. The module supports both low-speed and full-speed communication for all supported data transfer types.

1.1.5 EXTERNAL MEMORY BUS

Should 128 Kbytes of memory be inadequate for an application, the 80-pin and 100-pin members of the PIC18F9XJ94 family have an External Memory Bus (EMB), enabling the controller's internal Program Counter to address a memory space of up to 2 Mbytes. This is a level of data access that few 8-bit devices can claim and enables:

- Using combinations of on-chip and external memory of up to 2 Mbytes
- Using external Flash memory for reprogrammable application code or large data tables
- Using external RAM devices for storing large amounts of variable data

1.1.6 EXTENDED INSTRUCTION SET

The PIC18F9XJ94 family implements the optional extension to the PIC18 instruction set, adding eight new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as 'C'.

1.1.7 EASY MIGRATION

All devices share the same rich set of peripherals. This provides a smooth migration path within the device family as applications evolve and grow.

The consistent pinout scheme, used throughout the entire family, also aids in migrating to the next larger device. This is true when moving between the 64-pin members, between the 80-pin members, between the 100-pin members or even jumping from 64-pin to 80-pin to 100-pin devices.

The PIC18F9XJ94 family is also largely pin compatible with other PIC18 families, such as the PIC18F87J90, PIC18F87J11 and the PIC18F87J50. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining a similar feature set.

1.2 LCD Controller

The on-chip LCD driver includes many features that make the integration of displays in low-power applications easier. These include an integrated voltage regulator with charge pump and an integrated internal resistor ladder that allows contrast control in software and display operation above device V_{DD}.

TABLE 1-4: PIC18FXXJ94 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	100	80	64			
AD0/SEG0/RP20/PSP0/RD0	90	72	58			
AD0				I/O	TTL/DIG	External Memory Address/Data 0.
SEG0				O	Analog	SEG0 output for LCD.
RP20				I/O	ST/DIG	Remappable Peripheral Pin 20 input/output.
PSP0				I/O	ST/DIG	Parallel Slave Port data.
RD0				I/O	ST/DIG	General purpose I/O pin.
AD1/SEG1/RP21/PSP1/RD1	86	69	55			
AD1				I/O	TTL/DIG	External Memory Address/Data 1.
SEG1				O	Analog	SEG1 output for LCD.
RP21				I/O	ST/DIG	Remappable Peripheral Pin 21 input/output.
PSP1				I/O	ST/DIG	Parallel Slave Port data.
RD1				I/O	ST/DIG	General purpose I/O pin.
AD2/SEG2/RP22/PSP2/RD2	84	68	54			
AD2				I/O	TTL/DIG	External Memory Address/Data 2.
SEG2				O	Analog	SEG2 output for LCD.
RP22				I/O	ST/DIG	Remappable Peripheral Pin 22 input/output.
PSP2				I/O	ST/DIG	Parallel Slave Port data.
RD2				I/O	ST/DIG	General purpose I/O pin.
AD3/SEG3/RP23/PSP3/RD3	83	67	53			
AD3				I/O	TTL/DIG	External Memory Address/Data 3.
SEG3				O	Analog	SEG3 output for LCD.
RP23				I/O	ST/DIG	Remappable Peripheral Pin 3 input/output.
PSP3				I/O	ST/DIG	Parallel Slave Port data.
RD3				I/O	ST/DIG	General purpose I/O pin.
AD4/SEG4/RP24/PSP4/RD4	82	66	52			
AD4				I/O	TTL/DIG	External Memory Address/Data 4.
SEG4				O	Analog	SEG4 output for LCD.
RP24				I/O	ST/DIG	Remappable Peripheral Pin 24 input/output.
PSP4				I/O	ST/DIG	Parallel Slave Port data.
RD4				I/O	ST/DIG	General purpose I/O pin.
AD5/SEG5/SDA2/RP25/PSP5/RD5	81	65	51			
AD5				I/O	TTL/DIG	External Memory Address/Data 5.
SEG5				O	Analog	SEG5 output for LCD.
SDA2				I/O	I^2C	I^2C data input/output.
RP25				I/O	ST/DIG	Remappable Peripheral Pin 25 input/output.
PSP5				I/O	ST/DIG	Parallel Slave Port data.
RD5				I/O	ST/DIG	General purpose I/O pin.
AD6/SEG6/SCL2/RP26/PSP6/RD6	79	64	50			
AD6				I/O	TTL/DIG	External Memory Address/Data 6.
SEG6				O	Analog	SEG6 output for LCD.
SCL2				I/O	I^2C	I^2C clock input/output.
RP26				I/O	ST/DIG	Remappable Peripheral Pin 26 input/output.
PSP6				I/O	ST/DIG	Parallel Slave Port data.
RD6				I/O	ST/DIG	General purpose I/O pin.
AD7/SEG7/RP27/REFO2/ PSP7/RD7	78	63	49			
AD7				I/O	TTL/DIG	External Memory Address/Data 7.
SEG7				O	Analog	SEG7 output for LCD.
RP27				I/O	ST/DIG	Remappable Peripheral Pin 27 input/output.
REFO2				O	DIG	Reference output clock.
PSP7				I/O	ST/DIG	Parallel Slave Port data
RD7				I/O	ST/DIG	General purpose I/O pin.

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
I^2C = I^2C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to V_{DD})

3.5.1 SELECTING A PRIMARY OSCILLATOR MODE

The main difference between the MS and HS modes is the gain of the internal inverter of the oscillator circuit, which allows the different frequency ranges. The MS mode is a medium power, medium frequency mode. HS mode provides the highest oscillator frequencies with a crystal. OSC2 provides crystal feedback in both HS and MS Oscillator modes.

The EC and HS modes that use the PLL circuit provide the highest device operating frequencies. The oscillator circuit will consume the most current in these modes because the PLL is enabled to multiply the frequency of the oscillator.

In general, users should select the oscillator option with the lowest possible gain that still meets their specifications. This will result in lower dynamic currents (I_{DD}). The frequency range of each oscillator mode is the recommended frequency cutoff, but the selection of a different gain mode is acceptable as long as a thorough validation is performed (voltage, temperature and component variations, such as resistor, capacitor and internal oscillator circuitry).

The oscillator feedback circuit is disabled in all EC modes. The OSC1 pin is a high-impedance input and can be driven by a CMOS driver.

If the Primary Oscillator is configured for an external clock input, the OSC2 pin is not required to support the oscillator function. For these modes, the OSC2 pin can be used as an additional device I/O pin or a clock output pin. When the OSC2 pin is used as a clock output pin, the output frequency is $F_{OSC}/4$.

3.6 Crystal Oscillators and Ceramic Resonators

In MS and HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 3-3). The PIC18F oscillator design requires the use of a parallel cut crystal. Using a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

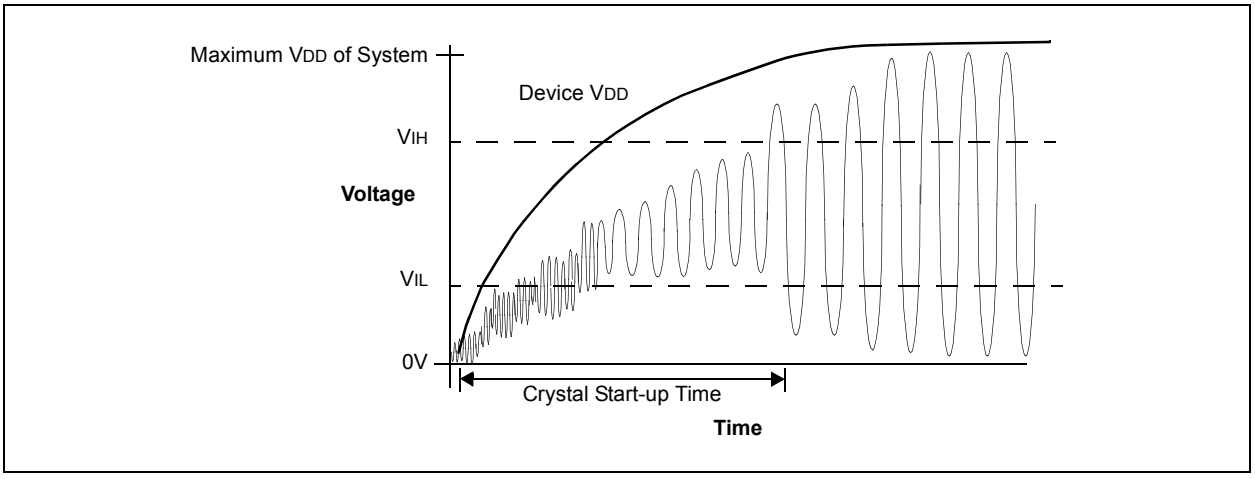
3.6.1 OSCILLATOR/RESONATOR START-UP

As the device voltage increases from V_{SS}, the oscillator will start its oscillations. The time required for the oscillator to start oscillating depends on many factors, including:

- Crystal/resonator frequency
- Capacitor values used
- Series resistor, if used, and its value and type
- Device V_{DD} rise time
- System temperature
- Oscillator mode selection of device (selects the gain of the internal oscillator inverter)
- Crystal quality
- Oscillator circuit layout
- System noise

The course of a typical crystal or resonator start-up is shown in Figure 3-4. Notice that the time to achieve stable oscillation is not instantaneous.

FIGURE 3-4: EXAMPLE OSCILLATOR/RESONATOR START-UP CHARACTERISTICS



3.15.3 CLOCK SYNCHRONIZATION

The Reference Clock Output is enabled only once (ON = 1). Note that the source of the clock and the divider values should be chosen prior to the bit being set to avoid glitches on the REFO output.

Once the ON bit is set, its value is synchronized to the reference clock domain to enable the output. This ensures that no glitches will be seen on the output. Similarly, when the ON bit is cleared, the output and the associated output enable signals will be synchronized, and disabled on the falling edge of the reference clock. Note that with large divider values, this will cause the REFO to be enabled for some period after ON is cleared.

3.15.4 OPERATION IN SLEEP MODE

If any clock source, other than the peripheral clock, is used as a base reference (i.e., ROSEL<3:0> ≠ 0001), the user has the option to configure the behavior of the oscillator in Sleep mode. The RSLP Configuration bit determines if the oscillator will continue to run in Sleep. If RSLP = 0, the oscillator will be shut down in Sleep (assuming no other consumers are requesting it). If RSLP = 1, the oscillator will continue to run in Sleep.

The Reference Clock Output is synchronized with the Sleep signal to avoid any glitches on its output.

3.15.5 MODULE ENABLE SIGNAL

The REFOx module may be enabled or disabled using the REFOxMD register bit (PMD3, bit 1 or 0). The module also needs to be turned on using the ON bit (REFO1CON<7>).

3.15.5.1 Registers and Bits

This module provides the following device registers and/or bits:

- REFOxCON – Reference Clock Output Control Register
- REFOxCON1 – Reference Clock Output Control 1 Register
- REFOxCON2 – Reference Clock Output Control 2 Register
- REFOxCON3 – Reference Clock Output Control 3 Register

TABLE 5-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices			Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
RPINR14_15	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
RPINR12_13	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
RPINR10_11	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
RPINR8_9	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
RPINR6_7	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
RPINR4_5	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
RPINR2_3	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
RPINR0_1	64-pin	80-pin	100-pin	1111 1111	1111 1111	uuuu uuuu
RPOR46	64-pin	80-pin	100-pin	---- 0000	---- 0000	---- uuuu
RPOR44_45	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR42_43	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR40_41	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR38_39	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR36_37	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR34_35	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR32_33	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR30_31	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR28_29	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR26_27	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR24_25	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR22_23	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR20_21	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR18_19	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR16_17	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR14_15	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR12_13	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR10_11	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR8_9	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR6_7	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR4_5	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR2_3	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
RPOR0_1	64-pin	80-pin	100-pin	0000 0000	0000 0000	uuuu uuuu
UCFG	64-pin	80-pin	100-pin	00-0 -000	00-0 -000	uu-u -uuu

Legend: u = unchanged; x = unknown; - = unimplemented bit, read as '0'; q = value depends on condition. Shaded cells indicate that conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-2 for Reset value for specific condition.

5: Bits 7,6 are unimplemented on 64 and 80-pin devices.

6: If the V_{BAT} is always powered, the DSGPx register values will remain unchanged after the first POR.

TABLE 6-2: REGISTER FILE SUMMARY (CONTINUED)

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FCFh	TMR1H	Timer1 Register High Byte							
FCEh	TMR1L	Timer1 Register Low Byte							
FCDh	T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	SOSCEN	$\overline{\text{T1SYNC}}$	RD16	TMR1ON
FCCh	TMR2	Timer2 Register							
FCBh	PR2	Timer2 Period Register							
FCAh	T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
FC9h	SSP1BUF	MSSP1 Receive Buffer/Transmit Register							
FC8h	SSP1ADD	MSSP1 Address Register in I^2C Slave Mode. MSSP1 Baud Rate Reload Register in I^2C Master Mode.							
FC7h	SSP1STAT	SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF
FC6h	SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
FC5h	SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
FC4h	CMSTAT	—	—	—	—	—	C3OUT	C2OUT	C1OUT
FC3h	ADCBUF0H	A/D Result Register 0 High Byte							
FC2h	ADCBUF0L	A/D Result Register 0 Low Byte							
FC1h	ADCON1H	ADON	—	—	—	—	MODE12	FORM1	FORM0
FC0h	ADCON1L	SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE
FBFh	CVRCONH	—	—	—	CVR4	CVR3	CVR2	CVR1	CVR0
FBEh	CVRCONL	CVREN	CVROE	CVRPSS1	CVRPSS0	—	—	—	CVRNSS
FBDh	ECCP1AS	ECCP1ASE	ECCP1AS2	ECCP1AS1	ECCP1AS0	PSS1AC1	PSS1AC0	PSS1BD1	PSS1BD0
FBCh	ECCP1DEL	P1RSEN	P1DC6	P1DC5	P1DC4	P1DC3	P1DC2	P1DC1	P1DC0
FBBh	CCPR1H	Capture/Compare/PWM Register1 High Byte							
FBAh	CCPR1L	Capture/Compare/PWM Register1 Low Byte							
FB9h	CCP1CON	P1M1	P1M0	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
FB8h	PIR5	—	ACTORSIF	ACTLOCKIF	TMR8IF	—	TMR6IF	TMR5IF	TMR4IF
FB7h	PIE5	—	ACTORSIE	ACTLOCKIE	TMR8IE	—	TMR6IE	TMR5IE	TMR4IE
FB6h	IPR4	CCP10IP	CCP9IP	CCP8IP	CCP7IP	CCP6IP	CCP5IP	CCP4IP	ECCP3IP
FB5h	PIR4	CCP10IF	CCP9IF	CCP8IF	CCP7IF	CCP6IF	CCP5IF	CCP4IF	ECCP3IF
FB4h	PIE4	CCP10IE	CCP9IE	CCP8IE	CCP7IE	CCP6IE	CCP5IE	CCP4IE	ECCP3IE
FB3h	TMR3H	Timer3 Register High Byte							
FB2h	TMR3L	Timer3 Register Low Byte							
FB1h	T3CON	TMR3CS1	TMR3CS0	T3CKPS1	T3CKPS0	SOSCEN	$\overline{\text{T3SYNC}}$	RD16	TMR3ON
FB0h	T3GCON	TMR3GE	T3GPOL	T3GTM	T3GSPM	T3GGO/$\overline{\text{T3DONE}}$	T3GVAL	T3GSS1	T3GSS0
FAFh	SPBRG1	EUSART1 Baud Rate Generator							
FAEh	RCREG1	EUSART1 Receive Register							
FADh	TXREG1	EUSART1 Transmit Register							
FACh	TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
FABh	RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
FAAh	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{T1DONE}}$	T1GVAL	T1GSS1	T1GSS0
FA9h	IPR6	RC4IP	TX4IP	RC3IP	TX3IP	—	CMP3IP	CMP2IP	CMP1IP
FA8h	HLVDCON	VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0
FA7h	PSPCON	IBF	OBF	IBOV	PSPMODE	—	—	—	—
FA6h	PIR6	RC4IF	TX4IF	RC3IF	TX3IF	—	CMP3IF	CMP2IF	CMP1IF
FA5h	IPR3	TMR5GIP	LCDIP	RC2IP	TX2IP	CTMUIP	CCP2IP	CCP1IP	RTCCIP
FA4h	PIR3	TMR5GIF	LCDIF	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	RTCCIF
FA3h	PIE3	TMR5GIE	LCDIE	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE
FA2h	IPR2	OSCFIP	SSP2IP	BCL2IP	USBIP	BCL1IP	HLVDIP	TMR3IP	TMR3GIP
FA1h	PIR2	OSCFIF	SSP2IF	BCL2IF	USBIF	BCL1IF	HLVDIF	TMR3IF	TMR3GIF
FA0h	PIE2	OSCFIE	SSP2IE	BCL2IE	USBIE	BCL1IE	HLVDIE	TMR3IE	TMR3GIE
F9Fh	IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	TMR1GIP	TMR2IP	TMR1IP
F9Eh	PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	TMR1GIF	TMR2IF	TMR1IF
F9Dh	PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	TMR1GIE	TMR2IE	TMR1IE

Legend: — = unimplemented, read as '0'.

11.0 I/O PORTS

Depending on the device selected and features enabled, there are up to eleven ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has three memory mapped registers for its operation:

- TRIS register (Data Direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (Output Latch register)

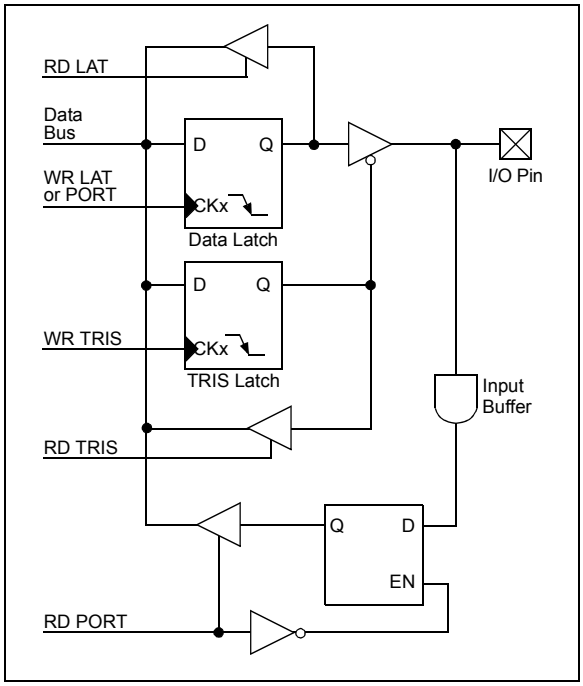
Reading the PORT register reads the current status of the pins, whereas writing to the PORT register, writes to the Output Latch (LAT) register.

Setting a TRIS bit (= 1) makes the corresponding PORT pin an input (putting the corresponding output driver in a High-Impedance mode). Clearing a TRIS bit (= 0) makes the corresponding port pin an output (i.e., driving the contents of the corresponding LAT bit on the selected pin).

The Output Latch (LAT register) is useful for read-modify-write operations on the value that the I/O pins are driving. Read-modify-write operations on the LAT register read and write the latched output value for the PORT register.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 11-1.

FIGURE 11-1: GENERIC I/O PORT OPERATION



11.1 I/O Port Pin Capabilities

When developing an application, the capabilities of the port pins must be considered.

The Absolute Maximum Ratings of the I/O pins are as follows:

- RA2, RA3 = -300mV to (V_{DD} + 300 mV)
- RA6, RA7, RC0, RC1 = -300 mV to (V_{DD} +300 mV)**(1)**
- RF3/RF4 (the USB D+/D- pins) = supports “USB specific levels” (e.g.: -1.0V to +4.6V, but only when the external source impedance is >/= 28 ohms, and the VUSB3V3 pin voltage is >/= 3.0V, otherwise: -500 mV to (VUSB3V3 +500 mV)
- All other general purpose I/O pins (including $\overline{MCLR}$), when V_{DD} is < 2.0V: -300 mV to +4.0V.
- All other general purpose I/O pins (including $\overline{MCLR}$), when V_{DD} is >= 2.0V: -300 mV to +6.0V**(2)**.

Note 1: When the pins are used to drive a crystal or ceramic resonator, natural oscillation waveforms slightly exceeding the -300 mV to (V_{DD} +300 mV) range may sometimes occur, and if present, such waveforms are allowed. If these pins are instead used as general purpose inputs, the external driving source should adhere to the -300 mV to (V_{DD} +300 mV) specification.

2: In addition to the above absolute maximums, any I/O pin voltage that is actively selected at runtime by the ADC channel select MUX must also meet the V_{AIN} requirements (parameter A25 in Table 30-40).

11.2 PORTA, LATA and TRISA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding Data Direction and Output Latch registers are TRISA and LATA.

All PORTA pins have Schmitt Trigger input levels and full CMOS output drivers.

RA<5:0> are multiplexed with analog inputs for the A/D Converter.

The operation of the analog inputs as A/D Converter inputs is selected by clearing or setting the ANSELx control bits in the ANCON1 register. The corresponding TRISA bits control the direction of these pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

Note: RA<5:0> are configured as analog inputs on any Reset and are read as '0'.

OSC2/CLKO/RA6 and OSC1/CLKI/RA7 normally serve as the external circuit connections for the External (Primary) Oscillator circuit (HS Oscillator modes), or the external clock input and output (EC Oscillator modes). In these cases, RA6 and RA7 are not available as digital I/O, and their corresponding TRIS and LAT bits are read as '0'. When the device is configured to use either the FRC or LPRC Internal Oscillators as the default oscillator mode, RA6 and RA7 are automatically configured as digital I/O; the oscillator and clock in/clock out functions are disabled.

EXAMPLE 11-1: INITIALIZING PORTA

```
CLRF     PORTA    ;  Initialize PORTA by
                  ; clearing output latches
CLRF     LATA     ; Alternate method to
                  ; clear output data latches
BANKSEL  ANCON1   ; Select bank with ANCON1 register
MOVLW    00h      ; Configure A/D
MOVWF    ANCON1   ; for digital inputs
BANKSEL  TRISA    ; Select bank with TRISA register
MOVLW    0BFh     ; Value used to initialize
                  ; data direction
MOVWF    TRISA    ; Set RA<7, 5:0> as inputs,
                  ; RA<6> as output
```

TABLE 11-1: PORTA FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0/AN1-/RP0/SEG19	RA0	0	O	DIG	LATA<0> data output; not affected by analog input.
		1	I	ST	PORTA<0> data input; disabled when analog input is enabled.
	AN0	1	I	ANA	A/D Input Channel 0. Default input configuration on POR; does not affect digital output.
	AN1-	1	I	ANA	Quasi-differential A/D negative input channel.
	RP0	x	x	DIG	Reconfigurable Pin 0 for PPS-Lite; TRIS must be set to match input/output of the module.
	SEG19	0	O	ANA	LCD Segment 19 output; disables all other pin functions.
RA1/AN1/RP1/SEG18	RA1	0	O	DIG	LATA<1> data output; not affected by analog input.
		1	I	ST	PORTA<1> data input; disabled when analog input is enabled.
	AN1	1	I	ANA	A/D Input Channel 1. Default input configuration on POR; does not affect digital output.
	RP1	x	x	DIG	Reconfigurable Pin 1 for PPS-Lite; TRIS must be set to match input/output of module.
	SEG18	0	O	ANA	LCD Segment 18 output; disables all other pin functions.
RA2/AN2/VREF-/RP2/SEG21	RA2	0	O	DIG	LATA<2> data output; not affected by analog input.
		1	I	ST	PORTA<2> data input; disabled when analog input enabled.
	AN2	1	I	ANA	A/D Input Channel 2. Default input configuration on POR; does not affect digital output.
	VREF-	1	I	ANA	A/D and Comparator Low Reference Voltage input.
	RP2	x	x	DIG	Reconfigurable Pin 2 for PPS-Lite; TRIS must be set to match input/output of module.
	SEG21	0	O	ANA	LCD Segment 21 output; disables all other pin functions.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

13.4 LCD Bias Types

The LCD module can be configured in one of three bias types:

- Static bias (two voltage levels: VSS and VDD)
- 1/2 bias (three voltage levels: VSS, 1/2 VDD and VDD)
- 1/3 bias (four voltage levels: VSS, 1/3 VDD, 2/3 VDD and VDD)

LCD bias voltages can be generated with internal resistor ladders, internal bias generator or external resistor ladder.

13.5 Internal Resistor Biasing

This mode does not use external resistors, but rather internal resistor ladders that are configured to generate the bias voltage.

The internal reference ladder actually consists of three separate ladders. Disabling the internal reference ladder disconnects all of the ladders, allowing external voltages to be supplied.

Depending on the total resistance of the resistor ladders, the biasing can be classified as low, medium or high power.

Table 13-3 shows the total resistance of each of the ladders. Table 13-3 shows the internal resister ladder connections. When the internal resistor ladder is selected, the bias voltage can either be from VDD or from VDDCORE, depending on the LCDIRS setting. It can also provide software contrast control (using LCDCST<2:0>)

.

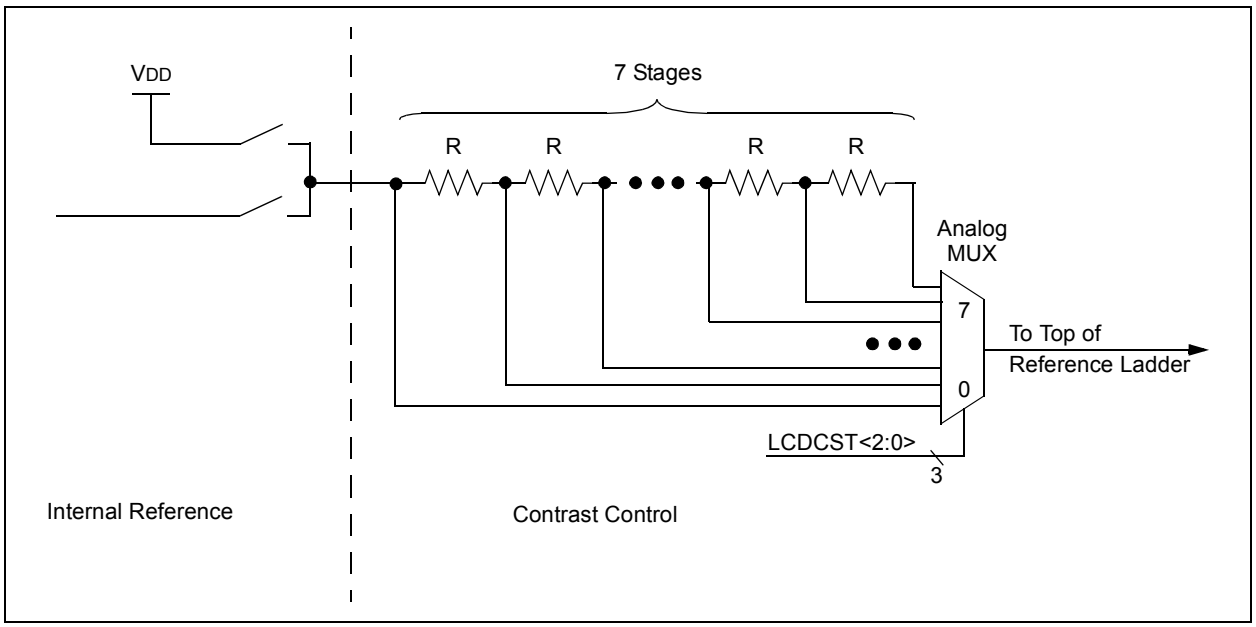
TABLE 13-3: INTERNAL RESISTANCE LADDER POWER MODES

Power Mode	Nominal Resistance of Entire Ladder	IDD
Low	3 MΩ	1 µA
Medium	300 kΩ	10 µA
High	30 kΩ	100 µA

13.5.2 CONTRAST CONTROL

The LCD contrast control circuit consists of a 7-tap resistor ladder, controlled by the LCDCSTx bits (see Figure 13-5)

FIGURE 13-5: INTERNAL REFERENCE AND CONTRAST CONTROL BLOCK DIAGRAM



13.5.3 INTERNAL REFERENCE

Under firmware control, an internal reference for the LCD bias voltages can be enabled. When enabled, the source of this voltage can be VDD.

When no internal reference is selected, the LCD contrast control circuit is disabled and LCD bias must be provided externally. Whenever the LCD module is inactive (LCDA = 0), the internal reference will be turned off.

13.5.4 VLCDxPE PINS

The VLCD3PE, VLCD2PE and VLCD1PE pins provide the ability for an external LCD bias network to be used instead of the internal ladder. Use of the VLCDxPE pins does not prevent use of the internal ladder.

Each VLCDxPE pin has an independent control in the LCDREF register, allowing access to any or all of the LCD bias signals.

This architecture allows for maximum flexibility in different applications. The VLCDxPE pins could be used to add capacitors to the internal reference ladder for increasing the drive capacity. For applications where the internal contrast control is insufficient, the firmware can choose to enable only the VLCD3PE pin, allowing an external contrast control circuit to use the internal reference divider.

In addition to the expanded range of modes available through the CCPxCON, the ECCP modules have three additional registers associated with Enhanced PWM operation, Pulse Steering Control and auto-shutdown features. They are:

- ECCPxDEL – Enhanced PWM x Control
- PSTRxCON – Pulse Steering x Control
- ECCPxAS – Auto-Shutdown x Control

18.1 ECCP Outputs and Configuration

The Enhanced CCP module may have up to four PWM outputs, depending on the selected operating mode.

These outputs, designated as PxA through PxD, are routed through the PPS-Lite module. Therefore, individual functions can be mapped to any of the remappable I/O pins (RPn). The outputs that are active depend on the ECCP operating mode selected. The pin assignments are summarized in Table 18-3.

To configure the I/O pins as PWM outputs, the proper PWM mode must be selected by setting the PxM<1:0> and CCPxM<3:0> bits. The appropriate TRIS direction bits for the port pins must also be set as outputs Table 18-3.

18.1.1 ECCP MODULE AND TIMER RESOURCES

The ECCP modules use Timers, 1, 2, 3, 4, 6 or 8, depending on the mode selected. These timers are available to CCP modules in Capture, Compare or PWM modes, as shown in Table 18-1.

TABLE 18-1: ECCP MODE – TIMER RESOURCE

ECCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2, Timer4, Timer6 or Timer8

The assignment of a particular timer to a module is determined by the timer to ECCP enable bits in the CCPTMRS0 register (Register 18-2). The interactions between the two modules are depicted in Figure 18-1. Capture operations are designed to be used when the timer is configured for Synchronous Counter mode. Capture operations may not work as expected if the associated timer is configured for Asynchronous Counter mode.

20.5.9.1 I²C Master Mode Operation

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDAx while SCLx outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/$\overline{W}$) bit. In this case, the R/$\overline{W}$ bit will be logic '0'. Serial data is transmitted, 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/$\overline{W}$ bit. In this case, the R/$\overline{W}$ bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address, followed by a '1' to indicate the receive bit. Serial data is received via SDAx, while SCLx outputs the serial clock. Serial data is received, 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

The Baud Rate Generator, used for the SPI mode operation, is used to set the SCLx clock frequency for either 100 kHz, 400 kHz or 1 MHz I²C operation. See **Section 20.5.10 "Baud Rate"** for more details.

A typical transmit sequence would go as follows:

1. The user generates a Start condition by setting the Start Enable bit, SEN (SSPxCON2<0>).
2. SSPxIF is set. The MSSPx module will wait the required start time before any other operation takes place.
3. The user loads the SSPxBUF with the slave address to transmit.
4. Address is shifted out the SDAx pin until all 8 bits are transmitted.
5. The MSSPx module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the SSPxCON2 register (SSPxCON2<6>).
6. The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
7. The user loads the SSPxBUF with eight bits of data.
8. Data is shifted out the SDAx pin until all 8 bits are transmitted.
9. The MSSPx module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the SSPxCON2 register (SSPxCON2<6>).
10. The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
11. The user generates a Stop condition by setting the Stop Enable bit, PEN (SSPxCON2<2>).
12. Interrupt is generated once the Stop condition is complete.

REGISTER 22-3: ANCON3: ANALOG SELECT CONTROL REGISTER 3 (FOR ANSEL23-ANSEL16)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSEL23	ANSEL22	ANSEL21	ANSEL20	ANSEL19	ANSEL18	ANSEL17	ANSEL16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ANSEL23:** Pin RH7 Analog Enable
1 = Pin configured as an analog channel – digital input disabled and reads '0'
0 = Pin configured as a digital port

bit 6 **ANSEL22:** Pin RH6 Analog Enable
1 = Pin configured as an analog channel – digital input disabled and reads '0'
0 = Pin configured as a digital port

bit 5 **ANSEL21:** Pin RH5 Analog Enable
1 = Pin configured as an analog channel – digital input disabled and reads '0'
0 = Pin configured as a digital port

bit 4 **ANSEL20:** Pin RH4 Analog Enable
1 = Pin configured as an analog channel – digital input disabled and reads '0'
0 = Pin configured as a digital port

bit 3 **ANSEL19:** Pin RH3 Analog Enable
1 = Pin configured as an analog channel – digital input disabled and reads '0'
0 = Pin configured as a digital port

bit 2 **ANSEL18:** Pin RH2 Analog Enable
1 = Pin configured as an analog channel – digital input disabled and reads '0'
0 = Pin configured as a digital port

bit 1 **ANSEL17:** Pin RH1 Analog Enable
1 = Pin configured as an analog channel – digital input disabled and reads '0'
0 = Pin configured as a digital port

bit 0 **ANSEL16:** Pin RH0 Analog Enable
1 = Pin configured as an analog channel – digital input disabled and reads '0'
0 = Pin configured as a digital port

REGISTER 22-5: ADCON1L: A/D CONTROL REGISTER 1 LOW

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **SSRC<3:0>:** Sample Clock Source Select bits

1111-1110 = Reserved, do not use
1101 = CMP1
1100 = Reserved, do not use
1011 = CCP4
1010 = ECCP3
1001 = ECCP2
1000 = ECCP1
0111 = The SAMP bit is cleared after SAMC<4:0> number of TAD clocks following the SAMP bit being set (Auto-Convert mode); no extended sample time is present
0110 = Unimplemented
0101 = TMR1
0100 = CTMU
0011 = TMR5
0010 = TMR3
0001 = INT0
0000 = The SAMP bit must be cleared by software to start conversion

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** A/D Sample Auto-Start bit

1 = Sampling begins immediately after last conversion; SAMP bit is auto-set
0 = Sampling begins when SAMP bit is manually set

bit 1 **SAMP:** A/D Sample Enable bit

1 = A/D Sample-and-Hold amplifiers are sampling
0 = A/D Sample-and-Hold amplifiers are holding

bit 0 **DONE:** A/D Conversion Status bit

1 = A/D conversion cycle has completed
0 = A/D conversion has not started or is in progress

22.5.2 CLOCKED CONVERSION TRIGGER

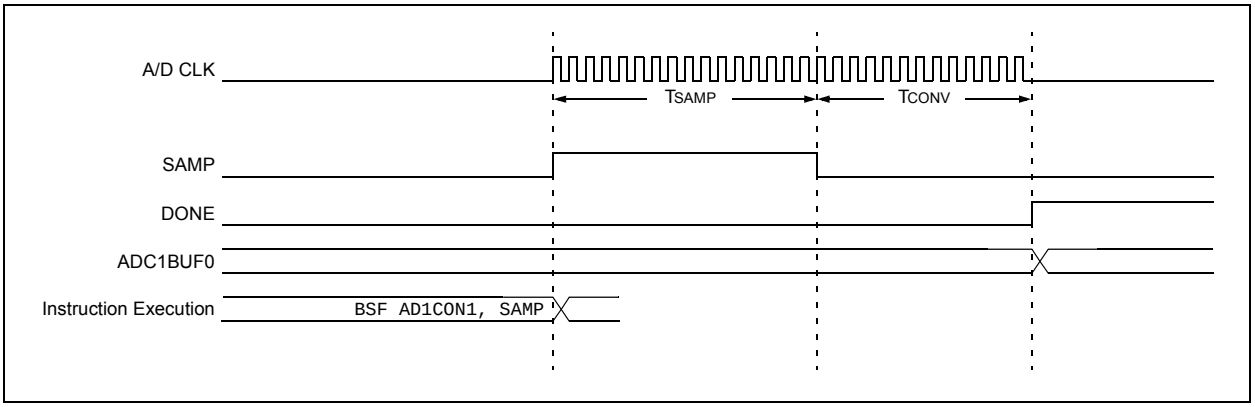
When ADRC = 1, the conversion trigger is under A/D clock control. The SAMCx bits (ADCON3H<4:0>) select the number of TAD clock cycles between the start of sampling and the start of conversion. After the start of sampling, the module will count a number of TAD clocks specified by the SAMCx bits. The SAMCx bits must always be programmed for at least one clock cycle to ensure sampling requirements are met.

EQUATION 22-2: CLOCKED CONVERSION TRIGGER TIME

$$T_{SMP} = SAMC<4:0> * T_{AD}$$

Figure 22-6 shows how to use the clocked conversion trigger with the sampling started by the user software.

FIGURE 22-6: CONVERTING ONE CHANNEL, MANUAL SAMPLE START, TAD-BASED CONVERSION START



EXAMPLE 22-2: CONVERTING ONE CHANNEL, MANUAL SAMPLE START, TAD-BASED CONVERSION START CODE

```
int ADCValue;

ANCON2  = 0x10;                     // all PORTB = Digital; RB12 = analog
ADCON1L = 0x70;                     // SSRC<2:0> = 111 implies internal counter ends sampling
                                    // and starts converting.
ADCHS0L = 0x0C;                     // Connect AN12 as S/H input.
                                    // in this example AN12 is the input
ADCSS0H = 0;
ADCON3H = 1F;                       // Sample time = 31Tad, Tad = 3Tcy
ADCON3L=02;
ADCON2L = 0;
ADCON1Hbits.ADON = 1;               // turn ADC ON
while (1)                           // repeat continuously
{
    ADCON1Lbits.SAMP = 1;           // start sampling, then after 31Tad go to conversion
    while (!ADCON1Lbits.DONE){};    // conversion done?
    ADCValue = ADCBUF0;             // yes then get ADC value
}                                   // repeat
```

EXAMPLE 22-6: CONVERTING A SINGLE CHANNEL, ONCE PER INTERRUPT, DUAL BUFFER MODE

A/D Configuration:

- Select AN3 for S/H+ Input (CH0SA<4:0> = 00011)
- Select VR- for S/H- Input (CH0NA<2:0> = 000)
- Configure for No Input Scan (CSCNA = 0)
- Use Only MUX A for Sampling (ALTS = 0)
- Set AD1IF on Every Sample (SMPI<4:0> = 00000)
- Configure Buffer as Dual, 8-Word Segments (BUFM = 1)

Operational Sequence:

1. Sample MUX A Input, AN3; Convert and Write to Buffer 0h.
2. Set AD1IF Flag (and generate interrupt, if enabled); Write Access Automatically Switches to Alternate Buffer.
3. Sample MUX A Input, AN3; Convert and Write to Buffer 8h.
4. Set AD1IF Flag (and generate interrupt, if enabled); Write Access Automatically Switches to Alternate Buffer.
5. Repeat (1-4).

Results Stored in Buffer (after 2 cycles):

Buffer Address	Buffer Contents at 1st AD1IF Event	Buffer Contents at 2nd AD1IF Event
ADC1BUF0	Sample 1 (AN3, Sample 1)	(undefined)
ADC1BUF1	(undefined)	(undefined)
ADC1BUF2	(undefined)	(undefined)
ADC1BUF3	(undefined)	(undefined)
ADC1BUF4	(undefined)	(undefined)
ADC1BUF5	(undefined)	(undefined)
ADC1BUF6	(undefined)	(undefined)
ADC1BUF7	(undefined)	(undefined)
ADC1BUF8	(undefined)	Sample 2 (AN3, Sample 2)
ADC1BUF9	(undefined)	(undefined)
ADC1BUFA	(undefined)	(undefined)
ADC1BUFB	(undefined)	(undefined)
ADC1BUFC	(undefined)	(undefined)
ADC1BUFD	(undefined)	(undefined)
ADC1BUFE	(undefined)	(undefined)
ADC1BUFF	(undefined)	(undefined)

22.8.3.1 Using Alternating MUX A and MUX B Input Selections

Figure 22-19 and Example 22-7 demonstrate alternate sampling of the inputs assigned to MUX A and MUX B. Setting the ALTS bit enables alternating input selections. The first sample uses the MUX A inputs specified by the CH0SAx and CH0NAx bits. The next sample uses the MUX B inputs, specified by the CH0SBx and CH0NBx bits.

This example also demonstrates use of the dual, 8-word buffers. An interrupt occurs after every 8th sample, resulting in filling eight words into the buffer on each interrupt.

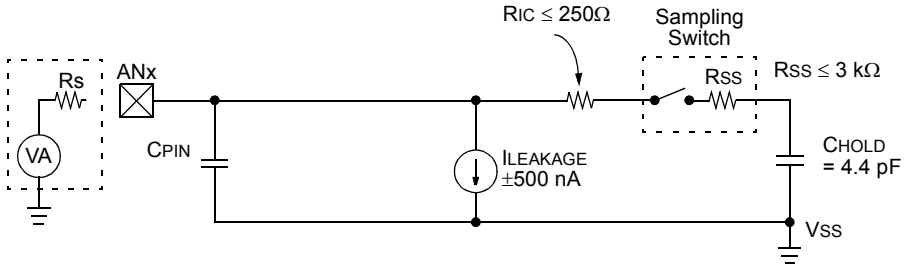
22.9 A/D Sampling Requirements

The Analog Input model of the 12-bit A/D Converter is shown in Figure 22-20. The total sampling time for the A/D is a function of the holding capacitor charge time.

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the voltage level on the analog input pin. The source impedance (RS), the interconnect impedance (RIC) and the internal sampling switch (RSS) impedance combine to directly affect the time required to charge CHOLD. The combined impedance of the analog sources must, therefore, be small enough to fully charge the holding capacitor within the chosen sample time. To minimize the effects of pin leakage currents on the accuracy of the A/D Converter, the maximum recommended source impedance, RS, is 2.5 k. After the analog input channel is selected (changed), this sampling function must be completed prior to starting the conversion. The internal holding capacitor will be in a discharged state prior to each sample operation.

At least 1 TAD time period should be allowed between conversions for the sample time. For more details, see **Section 30.0 "Electrical Specifications"**.

FIGURE 22-20: 12-BIT A/D CONVERTER ANALOG INPUT MODEL



Legend:		
	CPIN	= Input Capacitance
	VT	= Threshold Voltage
	ILEAKAGE	= Leakage Current at the Pin due to Various Junctions
	RIC	= Interconnect Resistance
	RSS	= Sampling Switch Resistance
	CHOLD	= Sample/Hold Capacitance (from DAC)

Note: CPIN value depends on device package and is not tested. The effect of the CPIN is negligible if Rs ≤ 5 kΩ.

22.10 Transfer Functions

The transfer functions of the A/D Converter, in 12-bit and 10-bit resolution, are shown in Figure 22-21 and Figure 22-22, respectively. In both cases, the difference of the input voltages, (VINH - VINL), is compared to the reference, ((VR+) - (VR-)).

For the 12-bit transfer function:

- The first code transition occurs when the input voltage is ((VR+) - (VR-))/4096 or 1.0 LSb.
- The '0000 0000 0001' code is centered at VR- + (1.5 * ((VR+) - (VR-)) / 4096).
- The '0010 0000 0000' code is centered at VREFL + (2048.5 * ((VR+) - (VR-)) /4096).
- An input voltage less than VR- + (((VR-) - (VR-)) / 4096) converts as '0000 0000 0000'.
- An input voltage greater than (VR-) + (4096 ((VR+) - (VR-))/4096) converts as '1111 1111 1111'.

24.0 COMPARATOR VOLTAGE REFERENCE MODULE

The comparator voltage reference is a 32-tap resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it may also be used independently of them.

A block diagram of the module is shown in Figure 24-1. The resistor ladder is segmented to provide a range of CV_{REF} values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device V_{DD}/V_{SS} or an external voltage reference.

24.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRCONH register (Register 24-1). The comparator voltage reference provides a range of output voltage with 32 levels.

The CVR<4:0> selection bits (CVRCONH<4:0>) offer a range of output voltages. Equation 24-1 shows how the comparator voltage reference is computed.

EQUATION 24-1:

If CVRSS = 1:

$$CV_{REF} = (V_{REF-} + \frac{CVR<4:0>}{32}) \bullet (V_{REF+} - V_{REF-})$$

If CVRSS = 0:

$$CV_{REF} = (AV_{SS} + \frac{CVR<4:0>}{32}) \bullet (AV_{DD} - AV_{SS})$$

The comparator voltage reference supply can come from either V_{DD} and V_{SS}, or the external V_{REF+} and V_{REF-} that are multiplexed with RA3 and RA2. The voltage source is selected by the CVRPSS<1:0> bits (CVRCONL<5:4>).

The settling time of the comparator voltage reference must be considered when changing the CV_{REF} output (see Table 30-13 in **Section 30.0 "Electrical Specifications"**).

REGISTER 24-1: CVRCONH: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER HIGH

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **CVR<4:0>:** Comparator V_{REF} Value Selection $0 \le CVR<4:0> \le 31$ bits

$CV_{REF} = V_{NEGSRC} + (CVR<4:0>/32) \bullet (V_{POSSRC} - V_{NEGSRC})$

XORWF	Exclusive OR W with f
Syntax:	XORWF f {,d {,a}}
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ dest
Status Affected:	N, Z

Encoding:

0001	10da	ffff	ffff

Description: Exclusive OR the contents of W with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in the register 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

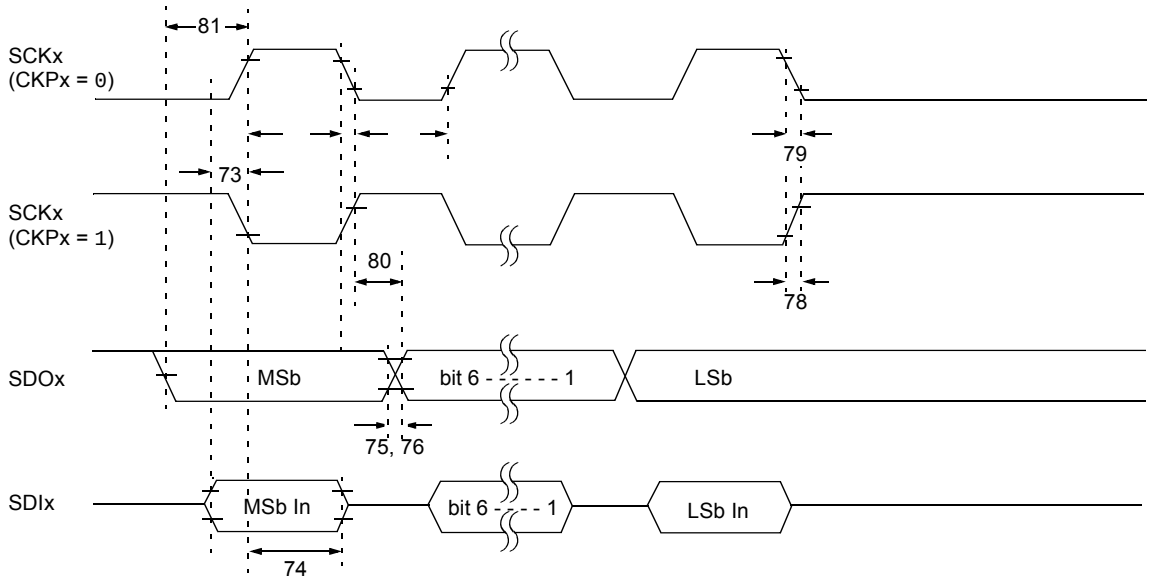
Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example:

```
XORWF   REG, 1, 0
```

Before Instruction
REG = AFh
W = B5h
After Instruction
REG = 1Ah
W = B5h

FIGURE 30-13: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)



Note: Refer to Figure 30-2 for load conditions.

TABLE 30-31: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
73	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	20	—	ns	
73A	TB2B	Last Clock Edge of Byte 1 to the 1st Clock Edge of Byte 2	1.5 TCY + 40	—	ns	
74	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	40	—	ns	
75	TDOR	SDOx Data Output Rise Time	—	25	ns	
76	TDOF	SDOx Data Output Fall Time	—	25	ns	
78	TSCR	SCKx Output Rise Time (Master mode)	—	25	ns	
79	TSCF	SCKx Output Fall Time (Master mode)	—	25	ns	
80	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid after SCKx Edge	—	50	ns	
81	TDOV2SCH, TDOV2SCL	SDOx Data Output Setup to SCKx Edge	TCY	—	ns	