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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	3MHz
Connectivity	USB
Peripherals	LVD, POR, PWM
Number of I/O	21
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908jb8adw

Section 11. Timer Interface Module (TIM)

Section 1. General Description

1.1 Contents

1.2 Introduction

The MC68HC908JB8 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

When the USB module is disabled, the PTE4 and PTE3 pins are general-purpose bidirectional I/O port pins with 10mA sink capability. Each pin is open-drain when configured as an output; and each pin contains a software configurable 5kΩ pullup to V_{DD} when configured as an input. The PTE4 pin can also be enabled to trigger the IRQ interrupt.

When the USB module is enabled, the PTE4/D– and PTE3/D+ pins become the USB module D– and D+ pins. The D– pin contains a software configurable 1.5kΩ pullup to V_{REG}. (See **Section 11. Timer Interface Module (TIM)**, **Section 9. Universal Serial Bus Module (USB)** and **Section 12. Input/Output Ports (I/O)**.)

Summary of the pin functions are provided in **Table 1-1**.

Table 1-1. Summary of Pin Functions

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
V_{DD}	Power supply.	IN	4.0 to 5.5V
V_{SS}	Power supply ground.	OUT	0V
V_{REG}	Regulated 3.3V output from MCU.	OUT	V_{REG} (3.3V)
$\overline{RST}$	Reset input; active low. With internal pullup to V_{DD} and schmitt trigger input.	IN/OUT	V_{DD}
$\overline{IRQ}$	External IRQ pin; with programmable internal pullup to V_{DD} and schmitt trigger input.	IN	V_{DD}
	Used for mode entry selection.	IN	V_{REG} to $V_{DD}+V_{HI}$
OSC1	Crystal oscillator input.	IN	V_{REG}
OSC2	Crystal oscillator output; inverting of OSC1 signal.	OUT	V_{REG}
PTA0/$\overline{KBA0}$: PTA7/$\overline{KBA7}$	8-bit general-purpose I/O port.	IN/OUT	V_{REG}
	Pins as keyboard interrupts, $\overline{KBA0}$–$\overline{KBA7}$.	IN	V_{REG}
	Each pin has programmable internal pullup to V_{REG} when configured as input.	IN	V_{REG}
PTB0–PTB7	8-bit general-purpose I/O port.	IN/OUT	V_{REG}
	Each pin has programmable internal pullup to V_{REG} when configured as input.	IN	V_{REG}

Section 2. Memory Map

2.1 Contents

2.2 Introduction

The CPU08 can address 64 Kbytes of memory space. The memory map, shown in **Figure 2-1**, includes:

- 8,192 bytes of user FLASH memory
- 256 bytes of RAM
- 16 bytes of user-defined vectors
- 976 bytes of monitor ROM

Section 5. Configuration Register (CONFIG)

5.1 Contents

5.2 Introduction

This section describes the configuration register (CONFIG). This write-once-after-reset register controls the following options:

- USB reset
- Low voltage inhibit
- Stop mode recovery time (2048 or 4096 OSCXCLK cycles)
- COP timeout period ($2^{18} – 2^4$ or $2^{13} – 2^4$ OSCXCLK cycles)
- STOP instruction
- Computer operating properly module (COP)

7.3 Oscillator External Connections

In its typical configuration, the oscillator requires five external components. The crystal oscillator is normally connected in a Pierce oscillator configuration, as shown in **Figure 7-1**. This figure shows only the logical representation of the internal components and may not represent actual circuitry. The oscillator configuration uses five components:

- Crystal, X_1
- Fixed capacitor, C_1
- Tuning capacitor, C_2 (can also be a fixed capacitor)
- Feedback resistor, R_B
- Series resistor, R_S (optional)

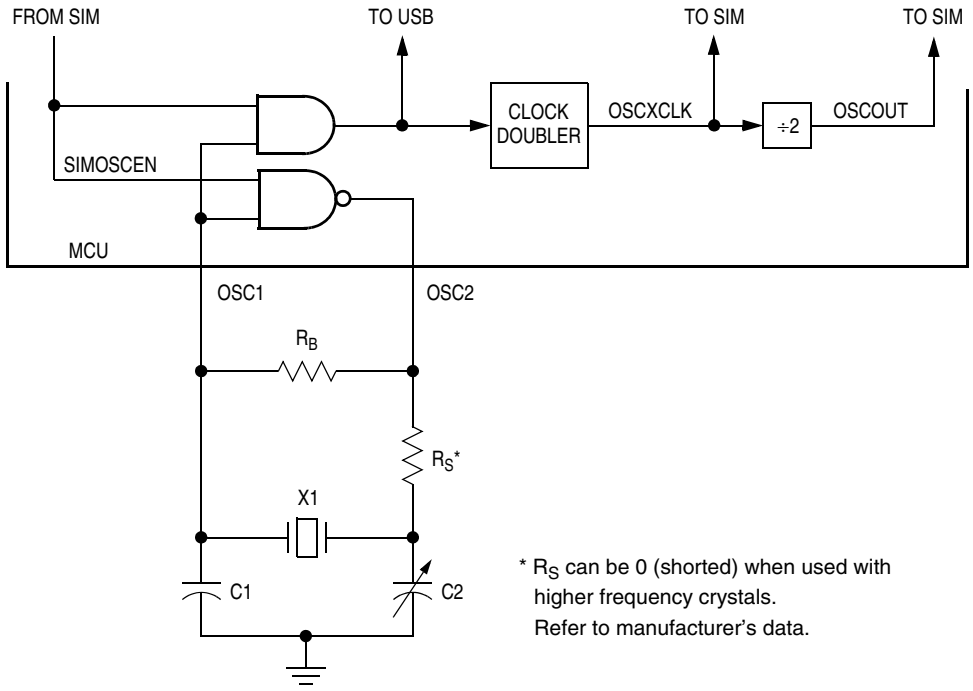

Figure 7-1. Oscillator External Connections

9.8.3 USB Interrupt Register 1

Address: $003A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	EOPF	RSTF	TXD2F	RXD2F	TXD1F	RESUMF	TXD0F	RXD0F
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-17. USB Interrupt Register 1 (UIR1)

EOPF — End-of-Packet Detect Flag

This read-only bit is set when a valid end-of-packet sequence is detected on the D+ and D– lines. Software must clear this flag by writing a logic 1 to the EOPFR bit.

Reset clears this bit. Writing to EOPF has no effect.

1 = End-of-packet sequence has been detected
0 = End-of-packet sequence has not been detected

RSTF — USB Reset Flag

This read-only bit is set when a valid reset signal state is detected on the D+ and D– lines. If the URSTD bit of the configuration register (CONFIG) is clear, this reset detection will generate an internal reset signal to reset the CPU and other peripherals including the USB module. If the URSTD bit is set, this reset detection will generate an USB interrupt. This bit is cleared by writing a logic 1 to the RSTFR bit. This bit also is cleared by a POR reset.

NOTE: *The USB bit in the RSR register (see* **8.8.2 Reset Status Register**) *is also a USB reset indicator.*

TXD2F — Endpoint 2 Data Transmit Flag

This read-only bit is set after the data stored in endpoint 2 transmit buffers has been sent and an ACK handshake packet from the host is received. Once the next set of data is ready in the transmit buffers, software must clear this flag by writing a logic 1 to the TXD2FR bit.

9.8.4 USB Interrupt Register 2

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:	EOPFR	RSTFR	TXD2FR	RXD2FR	TXD1FR	RESUMFR	TXD0FR	RXD0FR
Reset:	0	0	0	0	0	0	0	0

Figure 9-18. USB Interrupt Register 2 (UIR2)

EOPFR — End-of-Packet Flag Reset

Writing a logic 1 to this write-only bit will clear the EOPF bit if it is set. Writing a logic 0 to the EOPFR has no effect. Reset clears this bit.

RSTFR — Clear Reset Indicator Bit

Writing a logic 1 to this write-only bit will clear the RSTF bit if it is set. Writing a logic 0 to the RSTFR has no effect. Reset clears this bit.

TXD2FR — Endpoint 2 Transmit Flag Reset

Writing a logic 1 to this write-only bit will clear the TXD2F bit if it is set. Writing a logic 0 to TXD2FR has no effect. Reset clears this bit.

RXD2FR — Endpoint 2 Receive Flag Reset

Writing a logic 1 to this write-only bit will clear the RXD2F bit if it is set. Writing a logic 0 to RXD2FR has no effect. Reset clears this bit.

TXD1FR — Endpoint 1 Transmit Flag Reset

Writing a logic 1 to this write-only bit will clear the TXD1F bit if it is set. Writing a logic 0 to TXD1FR has no effect. Reset clears this bit.

RESUMFR — Resume Flag Reset

Writing a logic 1 to this write-only bit will clear the RESUMF bit if it is set. Writing to RESUMFR has no effect. Reset clears this bit.

TXD0FR — Endpoint 0 Transmit Flag Reset

Writing a logic 1 to this write-only bit will clear the TXD0F bit if it is set. Writing a logic 0 to TXD0FR has no effect. Reset clears this bit.

RXD0FR — Endpoint 0 Receive Flag Reset

Writing a logic 1 to this write-only bit will clear the RXD0F bit if it is set. Writing a logic 0 to RXD0FR has no effect. Reset clears this bit.

9.9 USB Interrupts

The USB module is capable of generating interrupts and causing the CPU to execute the USB interrupt service routine. There are three types of USB interrupts:

- End-of-transaction interrupts signify either a completed transaction receive or transmit transaction.
- Resume interrupts signify that the USB bus is reactivated after having been suspended.
- End-of-packet interrupts signify that a low-speed end-of-packet signal was detected.

All USB interrupts share the same interrupt vector. Firmware is responsible for determining which interrupt is active.

9.9.1 USB End-of-Transaction Interrupt

There are five possible end-of-transaction interrupts:

- Endpoint 0 or 2 receive
- Endpoint 0, 1 or 2 transmit

End-of-transaction interrupts occur as detailed in the following sections.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000A	TIM Status and Control Register (TSC)	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
$000C	TIM Counter Register High (TCNTH)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000D	TIM Counter Register Low (TCNTL)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000E	TIM Counter Modulo Register High (TMODH)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$000F	TIM Counter Modulo Register Low (TMODL)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0010	TIM Channel 0 Status and Control Register (TSC0)	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0011	TIM Channel 0 Register High (TCH0H)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	Indeterminate after reset							
$0012	TIM Channel 0 Register Low (TCH0L)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	Indeterminate after reset							
$0013	TIM Channel 1 Status and Control Register (TSC1)	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-2. TIM I/O Register Summary

Section 13. External Interrupt (IRQ)

13.1 Contents

13.2 Introduction

The IRQ module provides two external interrupt inputs: one dedicated $\overline{\text{IRQ}}$ pin and one shared port pin, PTE4/D–.

13.3 Features

Features of the IRQ module include:

- Two external interrupt pins, $\overline{\text{IRQ}}$ (5V) and PTE4/D– (5V)
- $\overline{\text{IRQ}}$ interrupt control bits
- Hysteresis buffer
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Low leakage $\overline{\text{IRQ}}$ pin for external RC wake up input
- Selectable internal pullup resistor

14.5 Functional Description

Writing to the KBIE7–KBIE0 bits in the keyboard interrupt enable register independently enables or disables each port A pin as a keyboard interrupt pin. Enabling a keyboard interrupt pin also enables its internal pullup device. A logic 0 applied to an enabled keyboard interrupt pin latches a keyboard interrupt request.

A keyboard interrupt is latched when one or more keyboard pins goes low after all were high. The MODEK bit in the keyboard status and control register controls the triggering mode of the keyboard interrupt.

- If the keyboard interrupt is edge-sensitive only, a falling edge on a keyboard pin does not latch an interrupt request if another keyboard pin is already low.
- If the keyboard interrupt is falling edge- and low level-sensitive, an interrupt request is present as long as any keyboard pin is low.

NOTE: *To prevent losing an interrupt request on one pin because another pin is still low, software can disable the latter pin while it is low.*

If the MODEK bit is set, the keyboard interrupt pins are both falling edge- and low level-sensitive, and both of the following actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a logic 1 to the ACKK bit in the keyboard status and control register (KBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt pins and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine also can prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt pins. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the CPU loads the program counter with the vector address at locations $FFF0 and $FFF1.

3. Write to the ACKK bit in the keyboard status and control register to clear any false interrupts.
4. Clear the IMASKK bit.

An interrupt signal on an edge-triggered pin can be acknowledged immediately after enabling the pin. An interrupt signal on an edge- and level-triggered interrupt pin must be acknowledged after a delay that depends on the external load.

Another way to avoid a false interrupt:

1. Configure the keyboard pins as outputs by setting the appropriate DDRA bits in data direction register A.
2. Write logic 1s to the appropriate port A data register bits.
3. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.

14.7 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power consumption standby modes.

14.7.1 Wait Mode

The keyboard module remains active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

14.7.2 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

Section 20. Ordering Information

20.1 Contents

20.2 Introduction

This section contains ordering numbers for the MC68HC908JB8.

20.3 MC Order Numbers

Table 20-1. MC Order Numbers

MC Order Number	Package	Operating Temperature Range	Compliance
MC68HC908JB8JP	20-pin PDIP	0 to +70 °C	—
MC68HC908JB8JDW	20-pin SOIC	0 to +70 °C	
MC68HC908JB8ADW	28-pin SOIC	0 to +70 °C	
MC68HC908JB8FB	44-pin QFP	0 to +70 °C	
MC68HC908JB8JPE	20-pin PDIP	0 to +70 °C	Pb-Free and RoHS compliant.
MC908JB8JDWE	20-pin SOIC	0 to +70 °C	
MC908JB8ADWE	28-pin SOIC	0 to +70 °C	
MC908JB8FBE	44-pin QFP	0 to +70 °C	

NOTES:
1. V_{DD} = 4.0 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source (f_{XCLK} = 6 MHz). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
4. Wait I_{DD} measured using external square wave clock source (f_{XCLK} = 6 MHz); all inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. C_L = 20 pF on OSC2; 15 kΩ ± 5% termination resistors on D+ and D– pins; all ports configured as inputs; OSC2 capacitance linearly affects wait I_{DD}
5. STOP I_{DD} measured with USB in suspend mode; OSC1 grounded; transceiver pullup resistor of 1.5 kΩ ± 5% between V_{REG} and D– pins and 15 kΩ ± 5% termination resistor on D+ pin; no port pins sourcing current.
6. Maximum is highest voltage that POR is guaranteed.
7. If minimum V_{REG} is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum V_{REG} is reached.

A.7.2 Memory Characteristics

Characteristic	Symbol	Min	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	V

Notes:
Since MC68HC08JB8 is a ROM device, FLASH memory electrical characteristics do not apply.

A.8 MC68HC08JB8 Order Numbers

These part numbers are generic numbers only. To place an order, ROM code must be submitted to the ROM Processing Center (RPC).

Table A-2. MC68HC08JB8 Order Numbers

MC Order Number	Package	Operating Temperature Range
MC68HC08JB8JP	20-pin PDIP	0 to +70 °C
MC68HC08JB8JDW	20-pin SOIC	0 to +70 °C
MC68HC08JB8ADW	28-pin SOIC	0 to +70 °C
MC68HC08JB8FB	44-pin QFP	0 to +70 °C

Appendix B. MC68HC08JT8

B.1 Contents

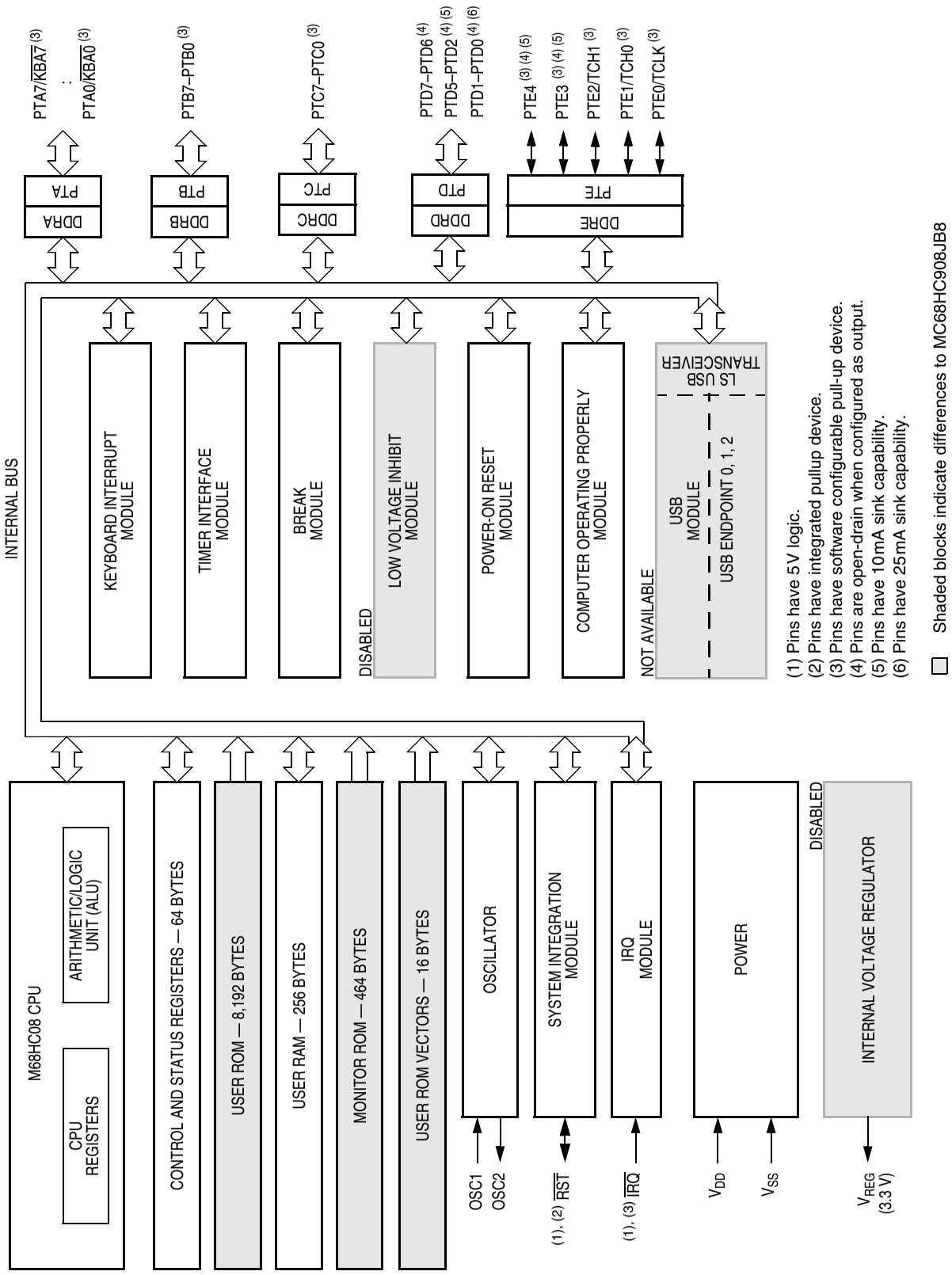

Figure B-1. MC68HC08JT8 Block Diagram

B.8 Monitor ROM

The monitor program (monitor ROM: $FE10–$FFDF) on the MC68HC08JT8 is for device testing only. $FC00–$FDFF are unused.

B.9 Universal Serial Bus Module

The USB module is designed for operation with V_{DD} = 4V to 5.5V, therefore, it should not be used on the MC68HC08JT8 device. To further reduce current consumption in stop mode, set the SUSPND bit in the USB interrupt register 0 (UIR0) to logic 1. Other USB registers should be left in their default state.

B.10 Low-Voltage Inhibit Module

The LVI module is disabled on the MC68HC08JT8.

B.11 Electrical Specifications

Electrical specifications for the MC68HC908JB8 apply to the MC68HC08JT8, except for the parameters indicated below.

B.11.1 Absolute Maximum Ratings

Characteristic[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.9	V
Input voltage	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum current per pin excluding V_{DD} and V_{SS}	I	± 25	mA
Storage temperature	T_{STG}	–55 to +150	°C
Maximum current of PTD0/1 (20-pin package)	I_{OL}	–15 to +30	mA
Maximum current out of V_{SS}	I_{MVSS}	100	mA
Maximum current into V_{DD}	I_{MVDD}	100	mA

NOTES:
1. Voltages referenced to V_{SS}.

NOTES:
1. V_{DD} = 2.0 to 3.6 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at 3V, 25 °C only.
3. In LDD mode, the specified I_{OL} is achieved when the external pullup voltage is equal to or higher than the voltage: V_{OL} + voltage dropped across LED.
4. Run (operating) I_{DD} measured using external square wave clock source (f_{XCLK} = 6 MHz). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
5. Wait I_{DD} measured using external square wave clock source (f_{XCLK} = 6 MHz). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects wait I_{DD}.
6. Stop I_{DD} measured with OSC1 grounded; no port pins sourcing current.
7. Maximum is highest voltage that POR is guaranteed.

B.11.4 Control Timing

Characteristic	Symbol	Min	Max	Unit
Internal operating frequency V_{DD} = 2.0V V_{DD} = 3.0V	f_{OP}	 — —	 2.5 3.0	 MHz MHz

B.11.5 Memory Characteristics

Characteristic	Symbol	Min	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	V

NOTES: Since MC68HC08JT8 is a ROM device, FLASH memory electrical characteristics do not apply.

B.12 MC68HC08JT8 Order Numbers

These part numbers are generic numbers only. To place an order, ROM code must be submitted to the ROM Processing Center (RPC).

Table B-2. MC68HC08JT8 Order Numbers

MC Order Number	Package	Operating Temperature Range	Compliance
MC68HC08JT8ADW	28-pin SOIC	0 to +70 °C	—
MC68HC08JT8FB	44-pin QFP	0 to +70 °C	
MC68HC08JT8FBE	44-pin QFP	0 to +70 °C	Pb-Free and RoHS compliant.