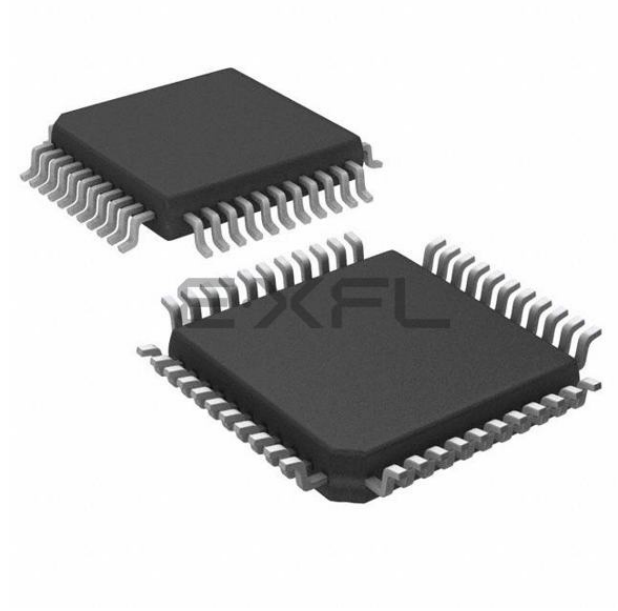

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	3MHz
Connectivity	USB
Peripherals	LVD, POR, PWM
Number of I/O	37
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908jb8fb

Revision History

Date	Revision Level	Description	Page Number(s)
September 2005	2.3	Added Pb-free parts.	267, 284
August 2005	2.2	Updated to meet Freescale identity guidelines.	Throughout
December 2003	2.1	**4.9 ROM-Resident Routines** — Removed block erase references for ROM-resident routines.	61
		9.8.8 USB Control Register 3 — Clarified bit descriptions for OSTALL0 and ISTALL0.	149, 150
		9.8.11 USB Status Register 1 — Clarified bit descriptions for TXACK, TXNAK, and TXSTL.	153
		Section 19. Mechanical Specifications — Replaced incorrect 44-pin QFP drawing, case 824E to case 824A.	263
February 2002	2	Corrected PTD6 and PTD7: not direct LED drive pins.	28, 210, 217
		Removed incorrect RX1E text from USB control register 1.	146
		Corrected **Figure 9-30** for USB module.	159
		Corrected timer discrepancies throughout **Section 11. Timer Interface Module (TIM)**.	177
		Added **Table 12-1 . Port Control Register Bits Summary**.	201
		Changed pullup resistor limits for D– and I/O ports in **18.6 DC Electrical Characteristics**.	256
		Added mechanical drawing for 20-pin SOIC package.	266
		Added **Appendix A. MC68HC08JB8** — ROM part.	269
		Added **Appendix B. MC68HC08JT8** — low-voltage ROM part.	277

Figure	Title	Page

1.3 Features

Features of the MC68HC908JB8 include:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 3-MHz internal bus frequency
- 8,192 bytes of on-chip FLASH memory
- 256 bytes of on-chip random-access memory (RAM)
- FLASH program memory security[1]
- On-chip programming firmware for use with host PC computer
- Up to 37 general-purpose 3.3V input/output (I/O) pins, including:
  - 13 or 10 shared-function I/O pins, depending on package
  - 24, 8, or 2 dedicated I/O pins, depending on package
  - 8 keyboard interrupts on port A, on all packages
  - 10mA sink capability for normal LED on 4 pins
  - 25mA sink capability for infrared LED on 2 pins
  - 10mA sink capability for PS/2 connection on 2 pins (with USB module disabled)
- 16-bit, 2-channel timer interface module (TIM) with selectable input capture, output compare, PWM capability on each channel, and external clock input option (TCLK)
- Full Universal Serial Bus Specification 1.1 low-speed functions:
  - 1.5 Mbps data rate
  - On-chip 3.3V regulator
  - Endpoint 0 with 8-byte transmit buffer and 8-byte receive buffer
  - Endpoint 1 with 8-byte transmit buffer
  - Endpoint 2 with 8-byte transmit buffer and 8-byte receive buffer

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

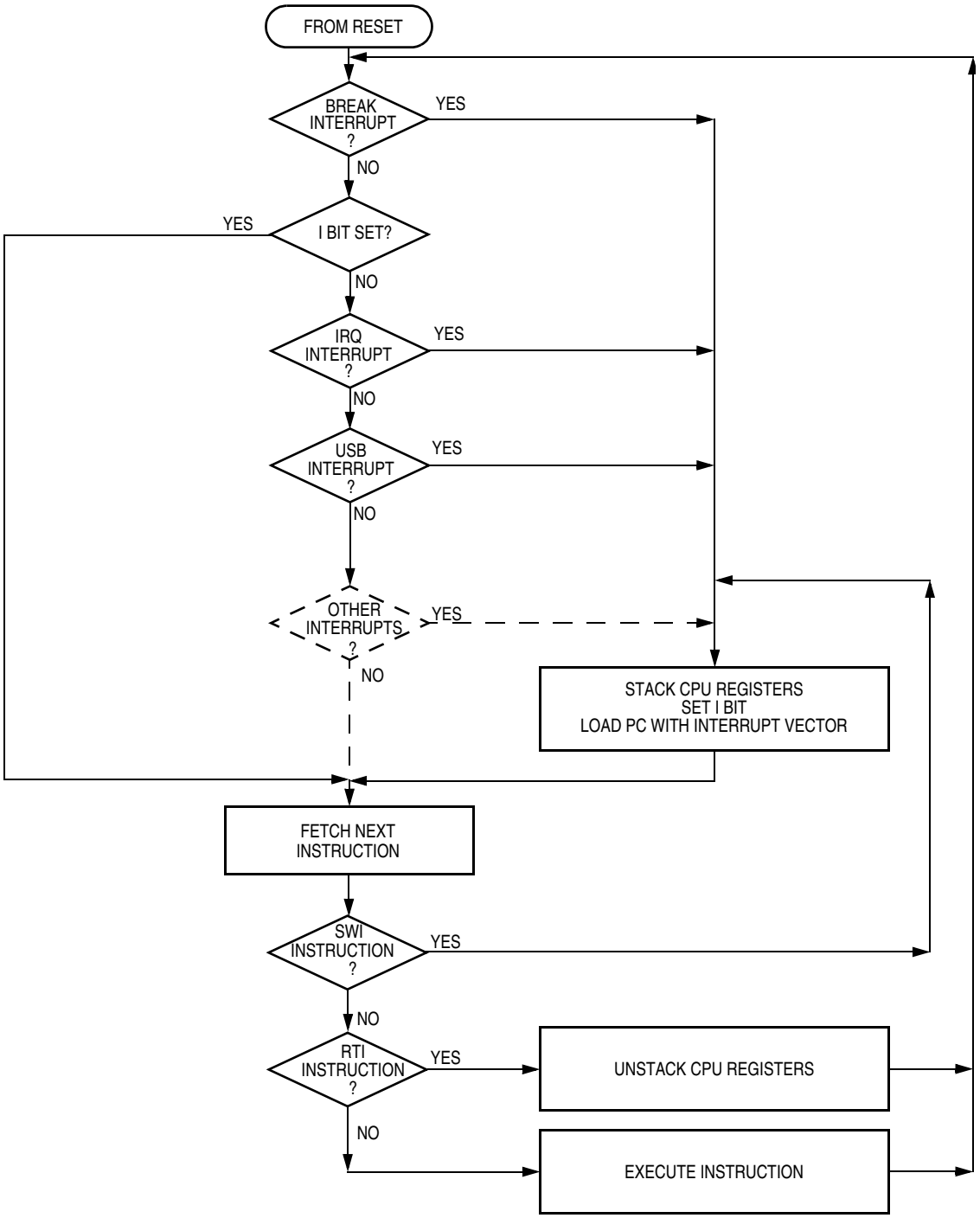


Figure 8-8. Interrupt Processing

8.7.2 Stop Mode

In stop mode, the SIM counter is reset and the system clocks are disabled. An interrupt request from a module can cause an exit from stop mode. Stacking for interrupts begins after the selected stop recovery time has elapsed. Reset or break also causes an exit from stop mode.

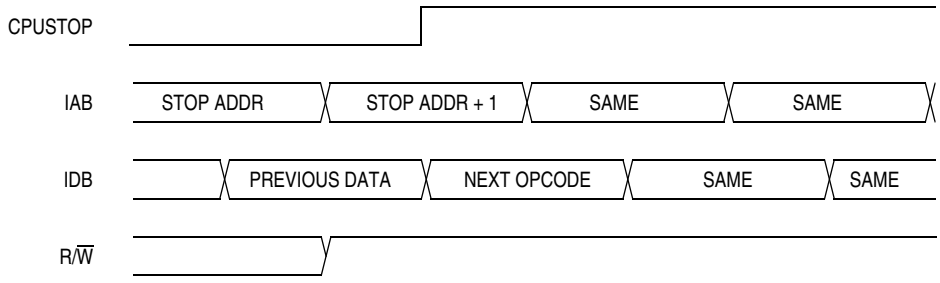
The SIM disables the oscillator signals (OSCOUT and OSCXCLK) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the configuration register (CONFIG). If SSREC is set, stop recovery is reduced from the normal delay of 4096 OSCXCLK cycles down to 2048. This is ideal for applications using canned oscillators that do not require long startup times from stop mode.

NOTE: *External crystal applications should use the full stop recovery time by clearing the SSREC bit.*

A break interrupt during stop mode sets the SIM break stop/wait bit (SBSW) in the break status register (BSR).

The SIM counter is held in reset from the execution of the STOP instruction until the beginning of stop recovery. It is then used to time the recovery period. **Figure 8-16** shows stop mode entry timing.

NOTE: *To minimize stop current, all pins configured as inputs should be driven to a logic 1 or logic 0.*



NOTE: Previous data can be operand data or the STOP opcode, depending on the last instruction.

Figure 8-16. Stop Mode Entry Timing

The start of a packet (SOP) is signaled by the originating port by driving the D+ and D– lines from the idle state (also referred to as the J state) to the opposite logic level (also referred to as the K state). This switch in levels represents the first bit of the sync field. **Figure 9-6** shows the data signaling and voltage levels for the start of packet and the sync pattern.

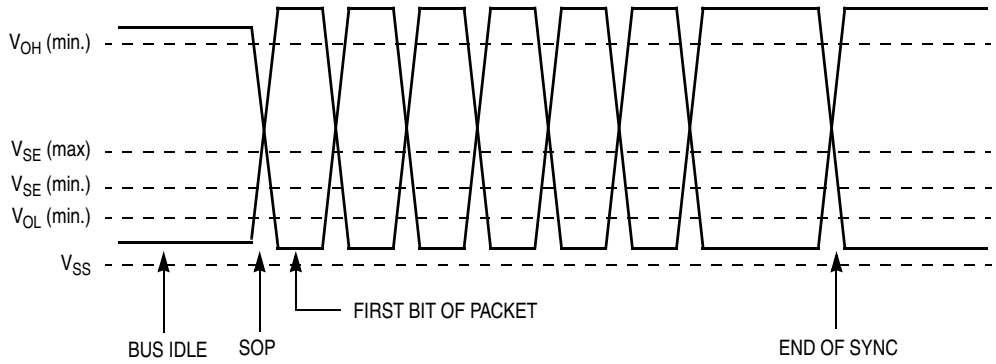


Figure 9-6. SOP, Sync Signaling, and Voltage Levels

9.5.1.2 Packet Identifier Field

The packet identifier field is an 8-bit number comprised of the 4-bit packet identification and its complement. The field follows the sync pattern and determines the direction and type of transaction on the bus. **Table 9-2** shows the packet identifier values for the supported packet types.

Table 9-2. Supported Packet Identifiers

Packet Identifier Value	Packet Identifier Type
%1001	IN Token
%0001	OUT Token
%1101	SETUP Token
%0011	DATA0 Packet
%1011	DATA1 Packet
%0010	ACK Handshake
%1010	NAK Handshake
%1110	STALL Handshake

9.5.5 Low-Speed Device

Low-speed devices are configured by the position of a pull-up resistor on the USB D– pin of the MCU. Low-speed devices are terminated as shown in **Figure 9-9** with the pull-up on the D– line.

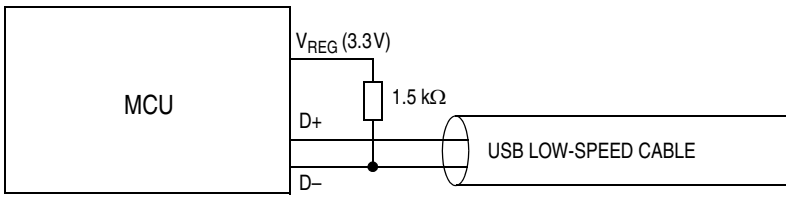


Figure 9-9. External Low-Speed Device Configuration

For low-speed transmissions, the transmitter's EOP width must be between 1.25 µs and 1.50 µs. These ranges include timing variations due to differential buffer delay and rise/fall time mismatches and to noise and other random effects. A low-speed receiver must accept a 670 ns SE0 followed by a J transition as a valid EOP. An SE0 shorter than 330 ns or an SE0 not followed by a J transition are rejected as an EOP. Any SE0 that is 8 µs or longer is automatically a reset.

9.6 Clock Requirements

The low-speed data rate is nominally 1.5 Mbps. The OSCXCLK signal driven by the oscillator circuits is the clock source for the USB module and requires that a 6-MHz oscillator circuit be connected to the OSC1 and OSC2 pins. The permitted frequency tolerance for low-speed functions is approximately ±1.5% (15,000 ppm). This tolerance includes inaccuracies from all sources: initial frequency accuracy, crystal capacitive loading, supply voltage on the oscillator, temperature, and aging. The jitter in the low-speed data rate must be less than 10 ns.

9.8.5 USB Control Register 0

Address: $003B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	T0SEQ	0	TX0E	RX0E	TP0SIZ3	TP0SIZ2	TP0SIZ1	TP0SIZ0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 9-19. USB Control Register 0 (UCR0)

T0SEQ — Endpoint 0 Transmit Sequence Bit

This read/write bit determines which type of data packet (DATA0 or DATA1) will be sent during the next IN transaction directed at endpoint 0. Toggling of this bit must be controlled by software. Reset clears this bit.

1 = DATA1 token active for next endpoint 0 transmit
0 = DATA0 token active for next endpoint 0 transmit

TX0E — Endpoint 0 Transmit Enable

This read/write bit enables a transmit to occur when the USB host controller sends an IN token to endpoint 0. Software should set this bit when data is ready to be transmitted. It must be cleared by software when no more endpoint 0 data needs to be transmitted.

If this bit is 0 or the TXD0F is set, the USB will respond with a NAK handshake to any endpoint 0 IN tokens. Reset clears this bit.

1 = Data is ready to be sent
0 = Data is not ready. Respond with NAK

RX0E — Endpoint 0 Receive Enable

This read/write bit enables a receive to occur when the USB host controller sends an OUT token to endpoint 0. Software should set this bit when data is ready to be received. It must be cleared by software when data cannot be received.

If this bit is 0 or the RXD0F is set, the USB will respond with a NAK handshake to any endpoint 0 OUT tokens; but does not respond to a SETUP token. Reset clears this bit.

1 = Data is ready to be received
0 = Not ready for data. Respond with NAK

9.8.8 USB Control Register 3

Address: $001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TX1ST	0	OSTALL0	ISTALL0	0	PULLEN	ENABLE2	ENABLE1
Write:		TX1STR						
Reset:	0	0	0	0	0	0*	0	0

= Unimplemented

* PULLEN bit is reset by POR or LVI reset only.

Figure 9-22. USB Control Register 3 (UCR3)

TX1ST — Endpoint 0 Transmit First Flag

This read-only bit is set if the endpoint 0 data transmit flag (TXD0F) is set when the USB control logic is setting the endpoint 0 data receive flag (RXD0F). In other words, if an unserviced endpoint 0 transmit flag is still set at the end of an endpoint 0 reception, then this bit will be set. This bit lets the firmware know that the endpoint 0 transmission happened before the endpoint 0 reception.

Reset clears this bit.

1 = IN transaction occurred before SETUP/OUT
0 = IN transaction occurred after SETUP/OUT

TX1STR — Clear Endpoint 0 Transmit First Flag

Writing a logic 1 to this write-only bit will clear the TX1ST bit if it is set. Writing a logic 0 to the TX1STR has no effect. Reset clears this bit.

OSTALL0 — Endpoint 0 Force STALL Bit for OUT token

This read/write bit causes endpoint 0 to return a STALL handshake when polled by an OUT token by the USB host controller. Reset clears this bit.

1 = Send STALL handshake
0 = Default

SETUP transactions cannot be stalled by the USB function. A SETUP received by a control endpoint will clear the ISTALL0 and OSTALL0 bits. The conditions for receiving a SETUP interrupt are shown in **Figure 9-30**.

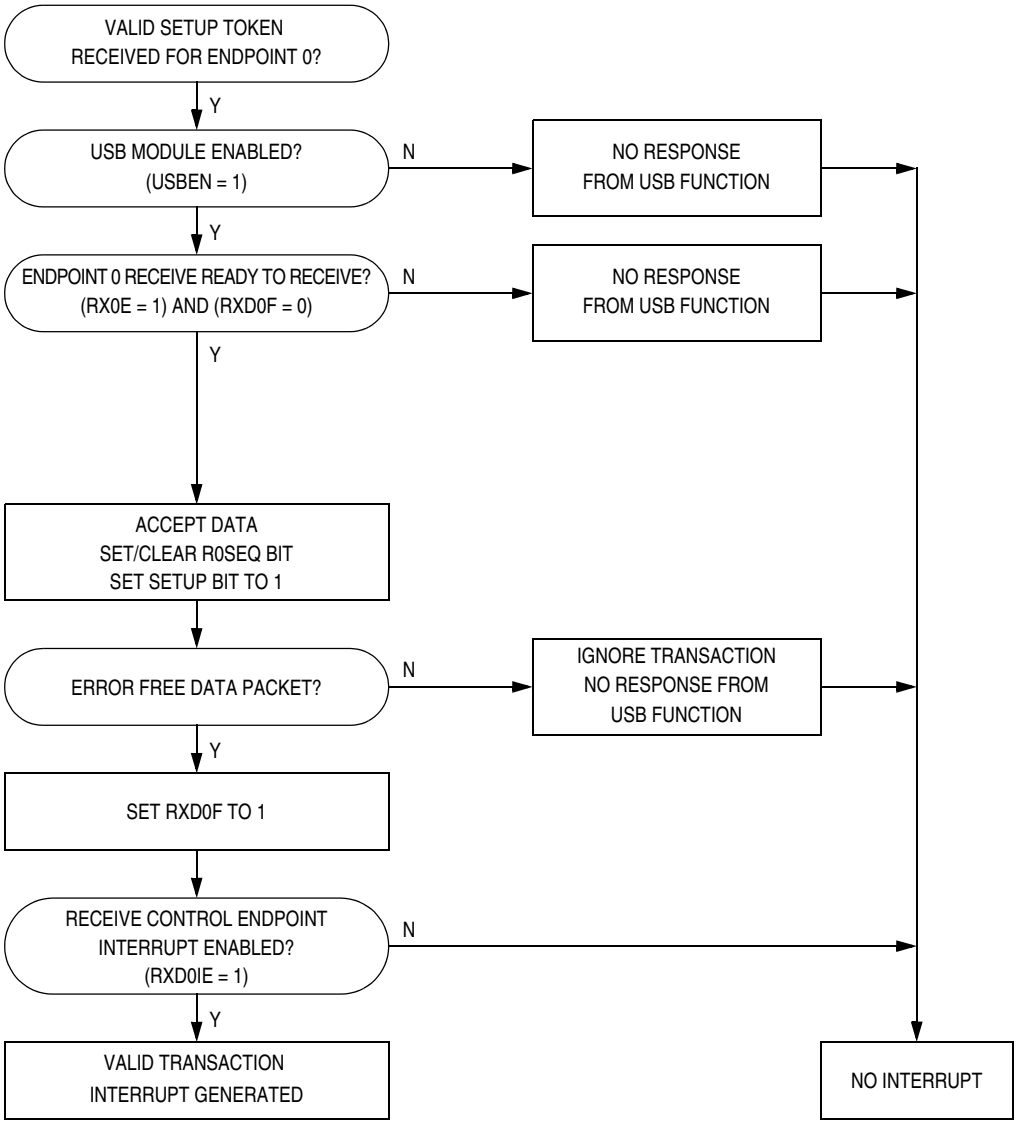


Figure 9-30. SETUP Token Data Flow for Receive Endpoint 0

9.9.1.2 Transmit Control Endpoint 0

For a control IN transaction directed at endpoint 0, the USB module will generate an interrupt by setting the TXD0F flag in the UIR1 register. The conditions necessary for the interrupt to occur are shown in the flowchart in **Figure 9-31**.

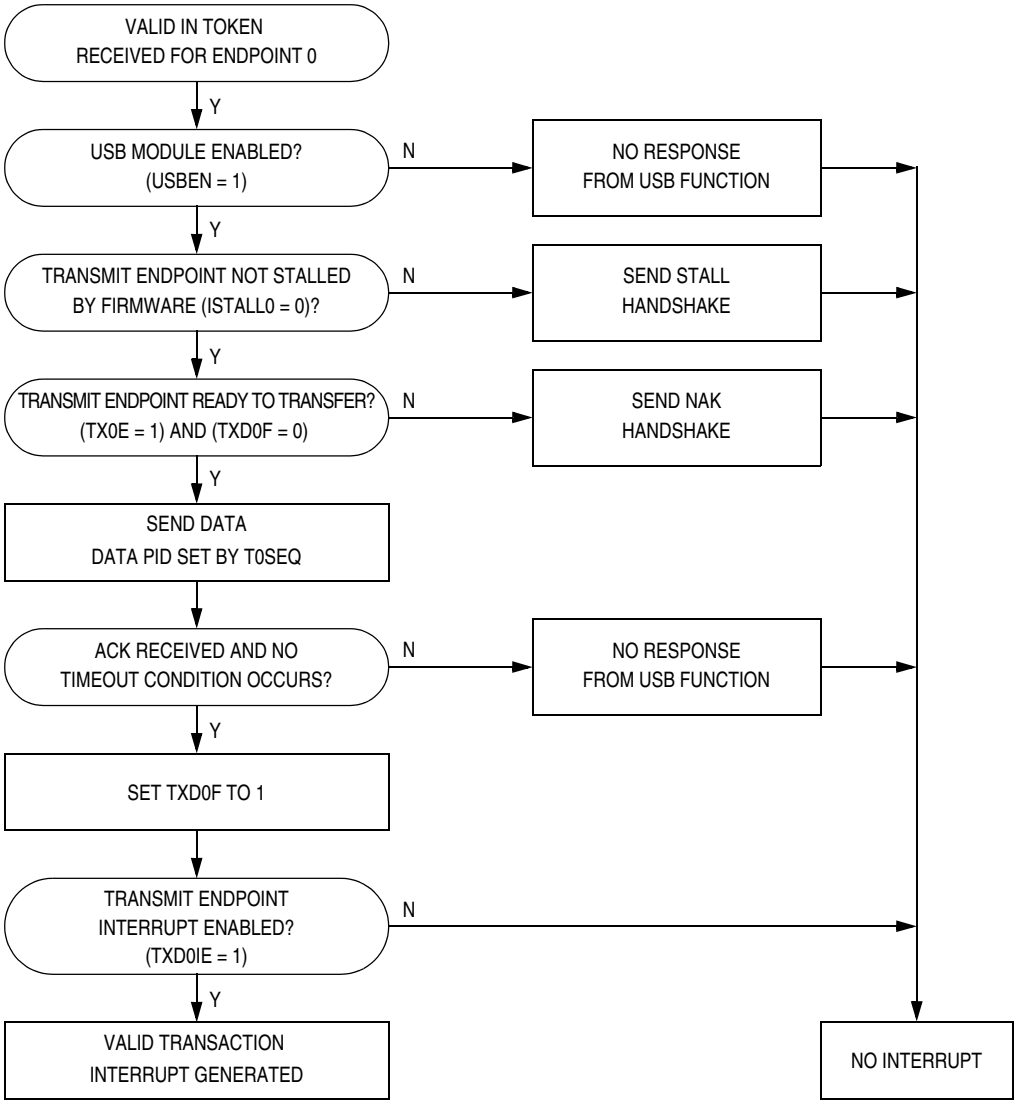


Figure 9-31. IN Token Data Flow for Transmit Endpoint 0

Table 10-8. READSP (Read Stack Pointer) Command

Description	Reads stack pointer
Operand	None
Data Returned	Returns stack pointer in high byte:low byte order
Opcode	$0C
Command Sequence	

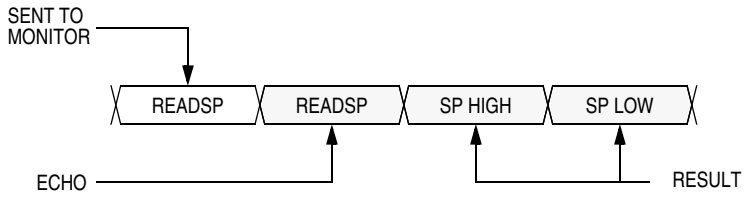
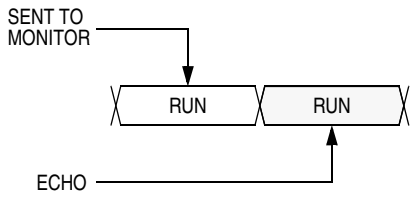


Table 10-9. RUN (Run User Program) Command

Description	Executes RTI instruction
Operand	None
Data Returned	None
Opcode	$28
Command Sequence	



12.6.1 Port D Data Register

The port D data register contains a data latch for each of the eight port D pins.

NOTE: *PTD7–PTD2 are not available in the 20-pin PDIP and 20-pin SOIC packages. PTD7 is not available in the 28-pin SOIC package.*

Address: $0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
Reset:	Unaffected by reset							
Additional Function:	Open-drain	Open-drain	Open-drain	Open-drain	Open-drain	Open-drain	Open-drain	Open-drain
			10mA sink	10mA sink	10mA sink	10mA sink	25mA sink	25mA sink

Figure 12-11. Port D Data Register (PTD)

PTD[7:0] — Port D Data Bits

These read/write bits are software programmable. Data direction of each port D pin is under control of the corresponding bit in data direction register D. Reset has no effect on port D data.

The LED direct drive bit, PTDLDD, in the port option control register (POCR) controls the drive options for the PTD5–PTD2 pins. The infrared LED drive bit, PTDILDD, in the POCR controls the drive options for the PTD1–PTD0 pins. (See **12.8 Port Options**.)

NOTE: *In 20-pin package, PTD1 and PTD0 are bonded together to PTD0/1 pin, forming a 50mA high current sink pin. When both PTD1 and PTD0 are configured as output, the values of PTD0 and PTD1 should be written the same.*

Section 14. Keyboard Interrupt Module (KBI)

14.1 Contents

14.2 Introduction

The keyboard interrupt module (KBI) provides eight independently maskable external interrupts which are accessible via PTA0–PTA7 pins.

14.8 Keyboard Module During Break Interrupts

The system integration module (SIM) controls whether the keyboard interrupt latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state.

To allow software to clear the keyboard interrupt latch during a break interrupt, write a logic 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latch during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), writing to the keyboard acknowledge bit (ACKK) in the keyboard status and control register during the break state has no effect. (See **14.9.1 Keyboard Status and Control Register**.)

14.9 I/O Registers

These registers control and monitor operation of the keyboard module:

- Keyboard status and control register (KBSCR)
- Keyboard interrupt enable register (KBIER)

14.9.1 Keyboard Status and Control Register

The keyboard status and control register:

- Flags keyboard interrupt requests
- Acknowledges keyboard interrupt requests
- Masks keyboard interrupt requests
- Controls keyboard interrupt triggering sensitivity

COPRS — COP Rate Select Bit

COPRS selects the COP timeout period. Reset clears COPRS.

1 = COP timeout period is $(2^{13} – 2^4) \times$ OSCXOUT cycles
0 = COP timeout period is $(2^{18} – 2^4) \times$ OSCXOUT cycles

COPD — COP Disable Bit

COPD disables the COP module.

1 = COP module disabled
0 = COP module enabled

15.5 COP Control Register

The COP control register is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Low byte of reset vector							
Write:	Clear COP counter							
Reset:	Unaffected by reset							

Figure 15-3. COP Control Register (COPCTL)

15.6 Interrupts

The COP does not generate CPU interrupt requests.

15.7 Monitor Mode

The COP is disabled in monitor mode when $V_{DD} + V_{HI}$ is present on the $\overline{IRQ}$ pin or on the $\overline{RST}$ pin.

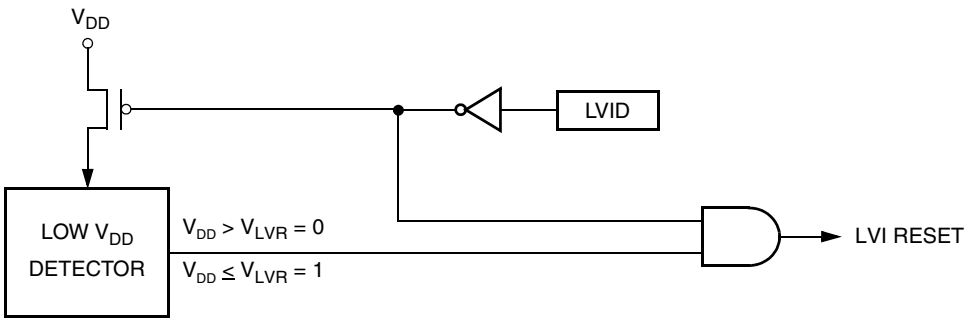


Figure 16-1. LVI Module Block Diagram

16.4 LVI Control Register (CONFIG)

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	URSTD	LVID	SSREC	COPRS	STOP	COPD
Write:								
Reset:	0	0	0	0	0	0	0	0

One-time writable register after each reset. URSTD and LVID bits are reset by POR or LVI reset only.

= Unimplemented

Figure 16-2. Configuration Register (CONFIG)

LVID —þLow Voltage Inhibit Disable Bit
1 = Low voltage inhibit disabled
0 = Low voltage inhibit enabled

16.5 Low-Power Modes

The STOP and WAIT instructions put the MCU in low-power consumption standby modes.

16.5.1 Wait Mode

The LVI module, when enabled, will continue to operate in WAIT Mode.

16.5.2 Stop Mode

The LVI module, when enabled, will continue to operate in STOP Mode.

Section 20. Ordering Information

20.1 Contents

20.2 Introduction

This section contains ordering numbers for the MC68HC908JB8.

20.3 MC Order Numbers

Table 20-1. MC Order Numbers

MC Order Number	Package	Operating Temperature Range	Compliance
MC68HC908JB8JP	20-pin PDIP	0 to +70 °C	—
MC68HC908JB8JDW	20-pin SOIC	0 to +70 °C	
MC68HC908JB8ADW	28-pin SOIC	0 to +70 °C	
MC68HC908JB8FB	44-pin QFP	0 to +70 °C	
MC68HC908JB8JPE	20-pin PDIP	0 to +70 °C	Pb-Free and RoHS compliant.
MC908JB8JDWE	20-pin SOIC	0 to +70 °C	
MC908JB8ADWE	28-pin SOIC	0 to +70 °C	
MC908JB8FBE	44-pin QFP	0 to +70 °C	

A.5 Reserved Registers

The two registers at $FE08 and $FE09 are reserved locations on the MC68HC08JB8.

On the MC68HC908JB8, these two locations are the FLASH control register and the FLASH block protect register respectively.

A.6 Monitor ROM

The monitor program (monitor ROM: $FE10–$FFDF) on the MC68HC08JB8 is for device testing only. $FC00–$FDFF are unused.

A.7 Electrical Specifications

Electrical specifications for the MC68HC908JB8 apply to the MC68HC08JB8, except for the parameters indicated below.

NOTES:
1. V_{DD} = 4.0 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source (f_{XCLK} = 6 MHz). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
4. Wait I_{DD} measured using external square wave clock source (f_{XCLK} = 6 MHz); all inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. C_L = 20 pF on OSC2; 15 kΩ ± 5% termination resistors on D+ and D– pins; all ports configured as inputs; OSC2 capacitance linearly affects wait I_{DD}
5. STOP I_{DD} measured with USB in suspend mode; OSC1 grounded; transceiver pullup resistor of 1.5 kΩ ± 5% between V_{REG} and D– pins and 15 kΩ ± 5% termination resistor on D+ pin; no port pins sourcing current.
6. Maximum is highest voltage that POR is guaranteed.
7. If minimum V_{REG} is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum V_{REG} is reached.

A.7.2 Memory Characteristics

Characteristic	Symbol	Min	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	V

Notes:
Since MC68HC08JB8 is a ROM device, FLASH memory electrical characteristics do not apply.

A.8 MC68HC08JB8 Order Numbers

These part numbers are generic numbers only. To place an order, ROM code must be submitted to the ROM Processing Center (RPC).

Table A-2. MC68HC08JB8 Order Numbers

MC Order Number	Package	Operating Temperature Range
MC68HC08JB8JP	20-pin PDIP	0 to +70 °C
MC68HC08JB8JDW	20-pin SOIC	0 to +70 °C
MC68HC08JB8ADW	28-pin SOIC	0 to +70 °C
MC68HC08JB8FB	44-pin QFP	0 to +70 °C