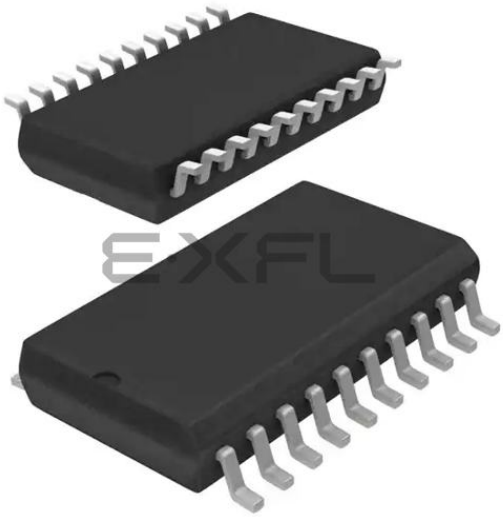

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	3MHz
Connectivity	USB
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908jb8jdw

List of Sections

Section 1. General Description

1.1 Contents

1.2 Introduction

The MC68HC908JB8 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

1.3 Features

Features of the MC68HC908JB8 include:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 3-MHz internal bus frequency
- 8,192 bytes of on-chip FLASH memory
- 256 bytes of on-chip random-access memory (RAM)
- FLASH program memory security[1]
- On-chip programming firmware for use with host PC computer
- Up to 37 general-purpose 3.3V input/output (I/O) pins, including:
  - 13 or 10 shared-function I/O pins, depending on package
  - 24, 8, or 2 dedicated I/O pins, depending on package
  - 8 keyboard interrupts on port A, on all packages
  - 10mA sink capability for normal LED on 4 pins
  - 25mA sink capability for infrared LED on 2 pins
  - 10mA sink capability for PS/2 connection on 2 pins (with USB module disabled)
- 16-bit, 2-channel timer interface module (TIM) with selectable input capture, output compare, PWM capability on each channel, and external clock input option (TCLK)
- Full Universal Serial Bus Specification 1.1 low-speed functions:
  - 1.5 Mbps data rate
  - On-chip 3.3V regulator
  - Endpoint 0 with 8-byte transmit buffer and 8-byte receive buffer
  - Endpoint 1 with 8-byte transmit buffer
  - Endpoint 2 with 8-byte transmit buffer and 8-byte receive buffer

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

When the USB module is disabled, the PTE4 and PTE3 pins are general-purpose bidirectional I/O port pins with 10mA sink capability. Each pin is open-drain when configured as an output; and each pin contains a software configurable 5kΩ pullup to V_{DD} when configured as an input. The PTE4 pin can also be enabled to trigger the IRQ interrupt.

When the USB module is enabled, the PTE4/D– and PTE3/D+ pins become the USB module D– and D+ pins. The D– pin contains a software configurable 1.5kΩ pullup to V_{REG}. (See **Section 11. Timer Interface Module (TIM)**, **Section 9. Universal Serial Bus Module (USB)** and **Section 12. Input/Output Ports (I/O)**.)

Summary of the pin functions are provided in **Table 1-1**.

Table 1-1. Summary of Pin Functions

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
V_{DD}	Power supply.	IN	4.0 to 5.5V
V_{SS}	Power supply ground.	OUT	0V
V_{REG}	Regulated 3.3V output from MCU.	OUT	V_{REG} (3.3V)
$\overline{RST}$	Reset input; active low. With internal pullup to V_{DD} and schmitt trigger input.	IN/OUT	V_{DD}
$\overline{IRQ}$	External IRQ pin; with programmable internal pullup to V_{DD} and schmitt trigger input.	IN	V_{DD}
	Used for mode entry selection.	IN	V_{REG} to $V_{DD}+V_{HI}$
OSC1	Crystal oscillator input.	IN	V_{REG}
OSC2	Crystal oscillator output; inverting of OSC1 signal.	OUT	V_{REG}
PTA0/$\overline{KBA0}$: PTA7/$\overline{KBA7}$	8-bit general-purpose I/O port.	IN/OUT	V_{REG}
	Pins as keyboard interrupts, $\overline{KBA0}$–$\overline{KBA7}$.	IN	V_{REG}
	Each pin has programmable internal pullup to V_{REG} when configured as input.	IN	V_{REG}
PTB0–PTB7	8-bit general-purpose I/O port.	IN/OUT	V_{REG}
	Each pin has programmable internal pullup to V_{REG} when configured as input.	IN	V_{REG}

4.8 FLASH Protection

Due to the ability of the on-board charge pump to erase and program the FLASH memory in the target application, provision is made to protect blocks of memory from unintentional erase or program operations due to system malfunction. This protection is done by use of a FLASH block protect register (FLBPR). The FLBPR determines the range of the FLASH memory which is to be protected. The range of the protected area starts from a location defined by FLBPR and ends to the bottom of the FLASH memory ($FFFF). When the memory is protected, the HVEN bit cannot be set in either ERASE or PROGRAM operations.

NOTE: *When the FLBPR is cleared (all 0's), the entire FLASH memory is protected from being programmed and erased. When all the bits are set, the entire FLASH memory is accessible for program and erase.*

4.8.1 FLASH Block Protect Register

The FLASH block protect register is implemented as an 8-bit I/O register. The content of this register determine the starting location of the protected range within the FLASH memory.

Address: $FE09

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
Reset:	0	0	0	0	0	0	0	0

Figure 4-4. FLASH Block Protect Register (FLBPR)

BPR[7:0] — FLASH Block Protect Register Bit 7 to Bit 0

BPR[7:1] represent bits [15:9] of a 16-bit memory address; bits [8:0] are logic 0's.

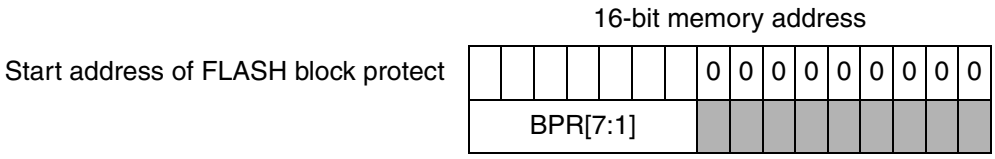

Figure 4-5. FLASH Block Protect Start Address

6.4.2 Index Register

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

The index register can serve also as a temporary data storage location.

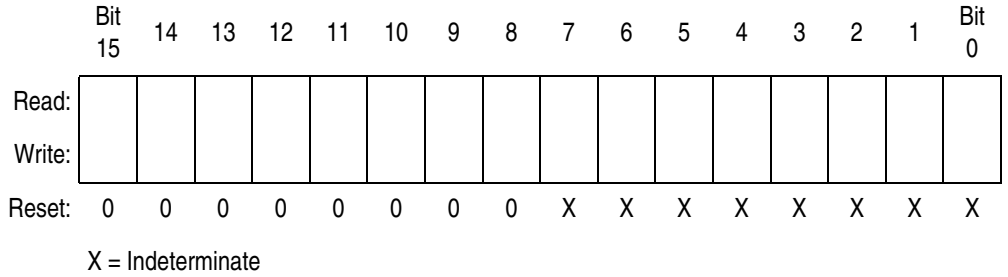

Figure 6-3. Index Register (H:X)

6.4.3 Stack Pointer

The stack pointer is a 16-bit register that contains the address of the next location on the stack. During a reset, the stack pointer is preset to $00FF. The reset stack pointer (RSP) instruction sets the least significant byte to $FF and does not affect the most significant byte. The stack pointer decrements as data is pushed onto the stack and increments as data is pulled from the stack.

In the stack pointer 8-bit offset and 16-bit offset addressing modes, the stack pointer can function as an index register to access data on the stack. The CPU uses the contents of the stack pointer to determine the conditional address of the operand.

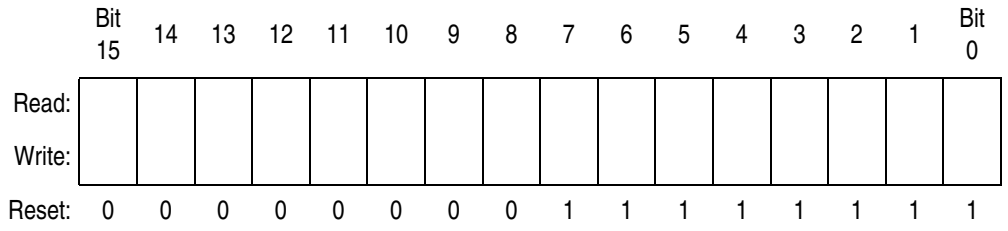

Figure 6-4. Stack Pointer (SP)

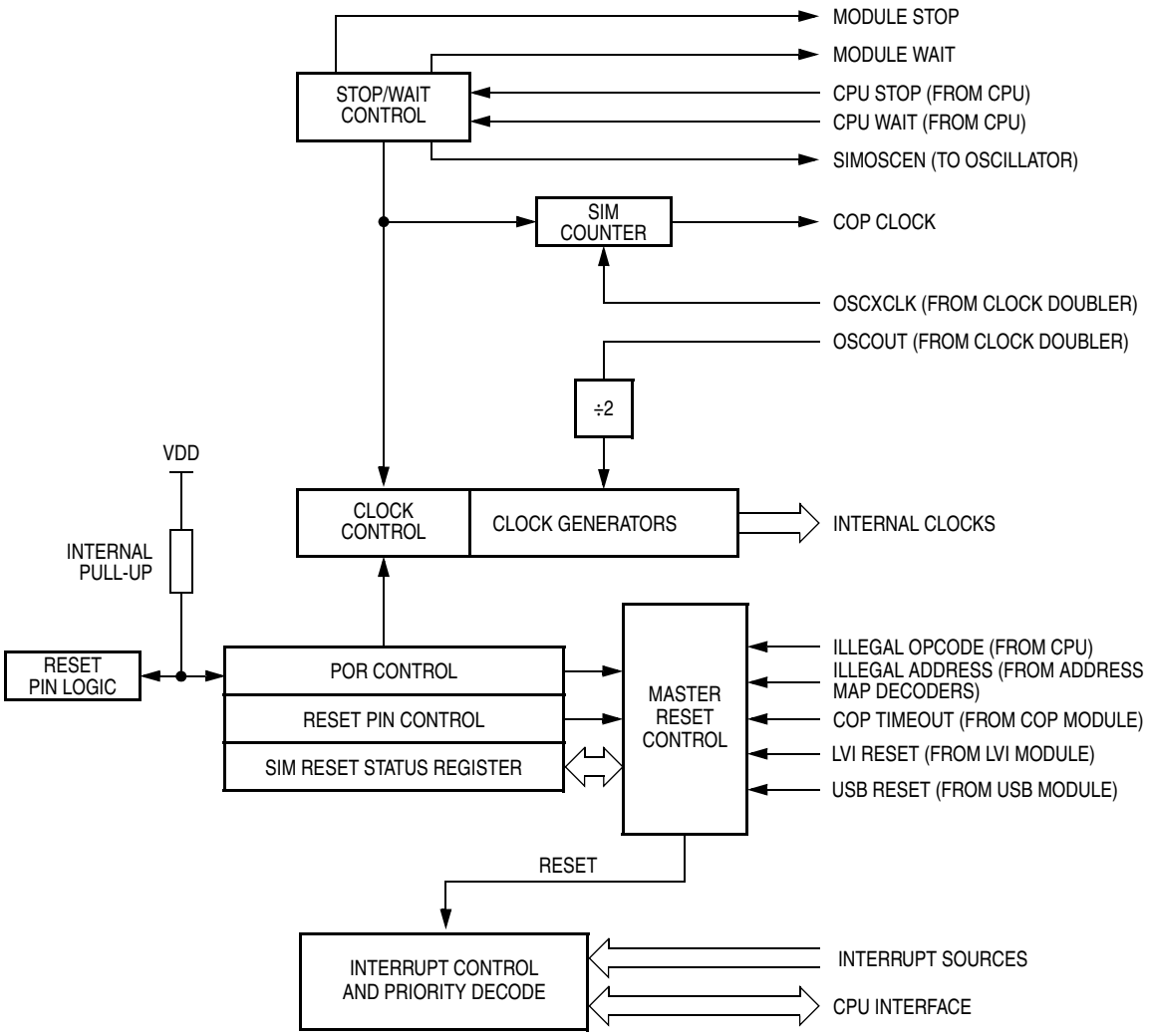

Figure 8-1. SIM Block Diagram

Table 8-1. SIM Module Signal Name Conventions

Signal Name	Description
OSCXCLK	Clock doubler output which has twice the frequency of OSC1 from the oscillator
OSCOUT	The OSCXCLK frequency divided by two. This signal is again divided by two in the SIM to generate the internal bus clocks. (Bus clock = OSCXCLK ÷ 4 = f_{OSC} ÷ 2)
IAB	Internal address bus
IDB	Internal data bus
PORRST	Signal from the power-on reset module to the SIM
IRST	Internal reset signal
R/$\overline{W}$	Read/write signal

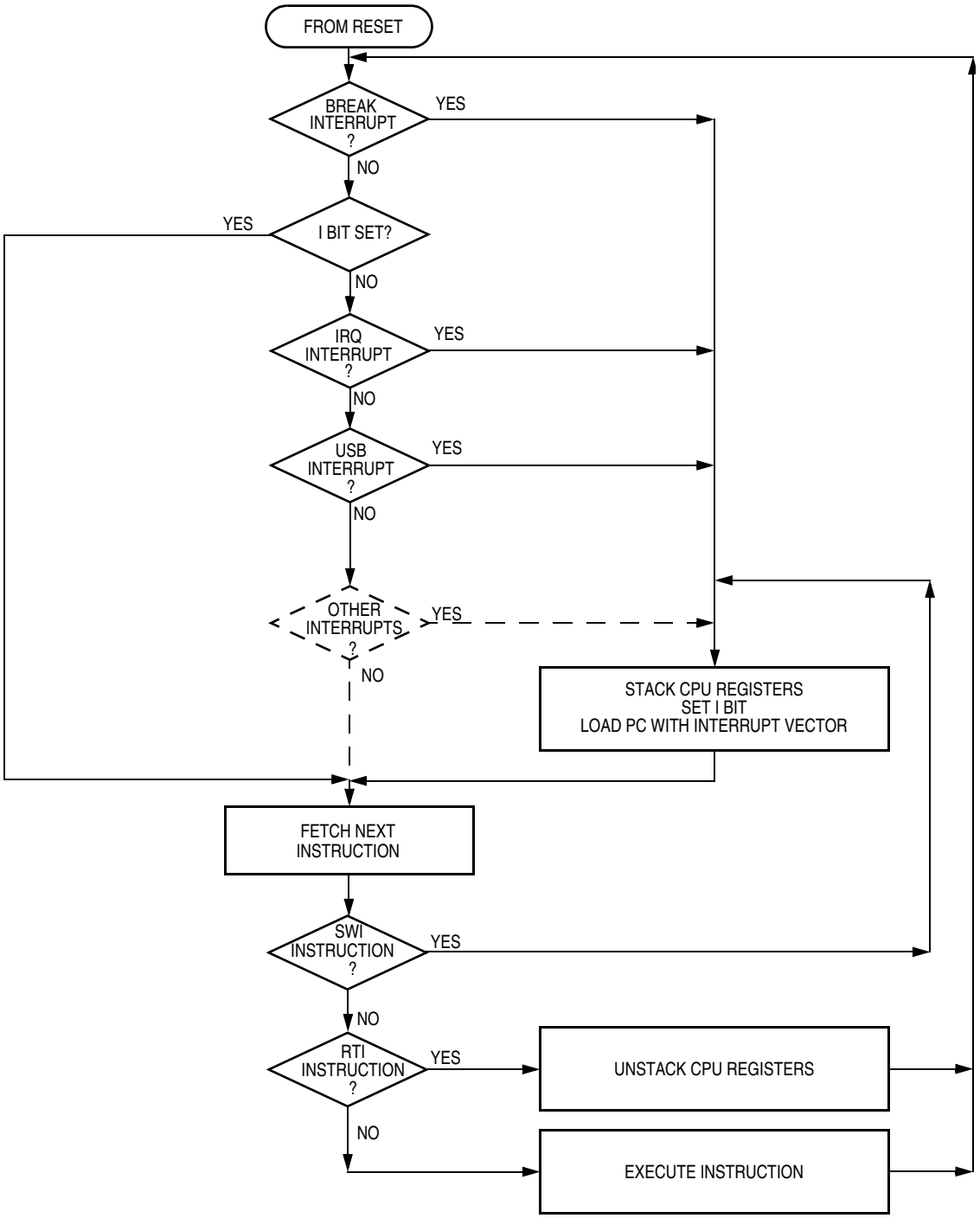

Figure 8-8. Interrupt Processing

Section 9. Universal Serial Bus Module (USB)

9.1 Contents

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0036	USB Endpoint 2 Data Register 6 (UE2D6)	Read:	UE2R67	UE2R66	UE2R65	UE2R64	UE2R63	UE2R62	UE2R61	UE2R60
		Write:	UE2T67	UE2T66	UE2T65	UE2T64	UE2T63	UE2T62	UE2T61	UE2T60
		Reset:	Unaffected by reset							
$0037	USB Endpoint 2 Data Register 7 (UE2D7)	Read:	UE2R77	UE2R76	UE2R75	UE2R74	UE2R73	UE2R72	UE2R71	UE2R70
		Write:	UE2T77	UE2T76	UE2T75	UE2T74	UE2T73	UE2T72	UE2T71	UE2T70
		Reset:	Unaffected by reset							
$0038	USB Address Register (UADDR)	Read:	USBEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0
		Write:								
		Reset:	0*	0	0	0	0	0	0	0

* USBEN bit is reset by POR or LVI reset only.

$0039	USB Interrupt Register 0 (UIR0)	Read:	EOPIE	SUSPND	TXD2IE	RXD2IE	TXD1IE	0	TXD0IE	RXD0IE
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$003A	USB Interrupt Register 1 (UIR1)	Read:	EOPF	RSTF	TXD2F	RXD2F	TXD1F	RESUMF	TXD0F	RXD0F
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$003B	USB Control Register 0 (UCR0)	Read:	T0SEQ	0	TX0E	RX0E	TP0SIZ3	TP0SIZ2	TP0SIZ1	TP0SIZ0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$003C	USB Control Register 1 (UCR1)	Read:	T1SEQ	STALL1	TX1E	FRESUM	TP1SIZ3	TP1SIZ2	TP1SIZ1	TP1SIZ0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$003D	USB Status Register 0 (USR0)	Read:	R0SEQ	SETUP	0	0	RP0SIZ3	RP0SIZ2	RP0SIZ1	RP0SIZ0
		Write:								
		Reset:	Unaffected by reset							
$003E	USB Status Register 1 (USR1)	Read:	R2SEQ	TXACK	TXNAK	TXSTL	RP2SIZ3	RP2SIZ2	RP2SIZ1	RP2SIZ0
		Write:								
		Reset:	U	0	0	0	U	U	U	U

= Unimplemented U = Unaffected by reset

Figure 9-1. USB I/O Register Summary (Sheet 4 of 4)

9.8.3 USB Interrupt Register 1

Address: $003A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	EOPF	RSTF	TXD2F	RXD2F	TXD1F	RESUMF	TXD0F	RXD0F
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-17. USB Interrupt Register 1 (UIR1)

EOPF — End-of-Packet Detect Flag

This read-only bit is set when a valid end-of-packet sequence is detected on the D+ and D– lines. Software must clear this flag by writing a logic 1 to the EOPFR bit.

Reset clears this bit. Writing to EOPF has no effect.

1 = End-of-packet sequence has been detected
0 = End-of-packet sequence has not been detected

RSTF — USB Reset Flag

This read-only bit is set when a valid reset signal state is detected on the D+ and D– lines. If the URSTD bit of the configuration register (CONFIG) is clear, this reset detection will generate an internal reset signal to reset the CPU and other peripherals including the USB module. If the URSTD bit is set, this reset detection will generate an USB interrupt. This bit is cleared by writing a logic 1 to the RSTFR bit. This bit also is cleared by a POR reset.

NOTE: *The USB bit in the RSR register (see* **8.8.2 Reset Status Register**) *is also a USB reset indicator.*

TXD2F — Endpoint 2 Data Transmit Flag

This read-only bit is set after the data stored in endpoint 2 transmit buffers has been sent and an ACK handshake packet from the host is received. Once the next set of data is ready in the transmit buffers, software must clear this flag by writing a logic 1 to the TXD2FR bit.

9.8.4 USB Interrupt Register 2

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:	EOPFR	RSTFR	TXD2FR	RXD2FR	TXD1FR	RESUMFR	TXD0FR	RXD0FR
Reset:	0	0	0	0	0	0	0	0

Figure 9-18. USB Interrupt Register 2 (UIR2)

EOPFR — End-of-Packet Flag Reset

Writing a logic 1 to this write-only bit will clear the EOPF bit if it is set. Writing a logic 0 to the EOPFR has no effect. Reset clears this bit.

RSTFR — Clear Reset Indicator Bit

Writing a logic 1 to this write-only bit will clear the RSTF bit if it is set. Writing a logic 0 to the RSTFR has no effect. Reset clears this bit.

TXD2FR — Endpoint 2 Transmit Flag Reset

Writing a logic 1 to this write-only bit will clear the TXD2F bit if it is set. Writing a logic 0 to TXD2FR has no effect. Reset clears this bit.

RXD2FR — Endpoint 2 Receive Flag Reset

Writing a logic 1 to this write-only bit will clear the RXD2F bit if it is set. Writing a logic 0 to RXD2FR has no effect. Reset clears this bit.

TXD1FR — Endpoint 1 Transmit Flag Reset

Writing a logic 1 to this write-only bit will clear the TXD1F bit if it is set. Writing a logic 0 to TXD1FR has no effect. Reset clears this bit.

RESUMFR — Resume Flag Reset

Writing a logic 1 to this write-only bit will clear the RESUMF bit if it is set. Writing to RESUMFR has no effect. Reset clears this bit.

TXD0FR — Endpoint 0 Transmit Flag Reset

Writing a logic 1 to this write-only bit will clear the TXD0F bit if it is set. Writing a logic 0 to TXD0FR has no effect. Reset clears this bit.

RXD0FR — Endpoint 0 Receive Flag Reset

Writing a logic 1 to this write-only bit will clear the RXD0F bit if it is set. Writing a logic 0 to RXD0FR has no effect. Reset clears this bit.

STALL2 — Endpoint 2 Force Stall Bit

This read/write bit causes endpoint 2 to return a STALL handshake when polled by either an IN or OUT token by the USB host controller. Reset clears this bit.

1 = Send STALL handshake
0 = Default

TX2E — Endpoint 2 Transmit Enable

This read/write bit enables a transmit to occur when the USB host controller sends an IN token to endpoint 2. The appropriate endpoint enable bit, ENABLE2 bit in the UCR3 register, also should be set. Software should set the TX2E bit when data is ready to be transmitted. It must be cleared by software when no more data needs to be transmitted.

If this bit is 0 or the TXD2F is set, the USB will respond with a NAK handshake to any endpoint 2 directed IN tokens. Reset clears this bit.

1 = Data is ready to be sent
0 = Data is not ready. Respond with NAK

RX2E — Endpoint 2 Receive Enable

This read/write bit enables a receive to occur when the USB host controller sends an OUT token to endpoint 2. Software should set this bit when data is ready to be received. It must be cleared by software when data cannot be received.

If this bit is 0 or the RXD2F is set, the USB will respond with a NAK handshake to any endpoint 2 OUT tokens. Reset clears this bit.

1 = Data is ready to be received
0 = Not ready for data. Respond with NAK

TP2SIZ3–TP2SIZ0 — Endpoint 2 Transmit Data Packet Size

These read/write bits store the number of transmit data bytes for the next IN token request for endpoint 2. These bits are cleared by reset.

SETUP transactions cannot be stalled by the USB function. A SETUP received by a control endpoint will clear the ISTALL0 and OSTALL0 bits. The conditions for receiving a SETUP interrupt are shown in **Figure 9-30**.

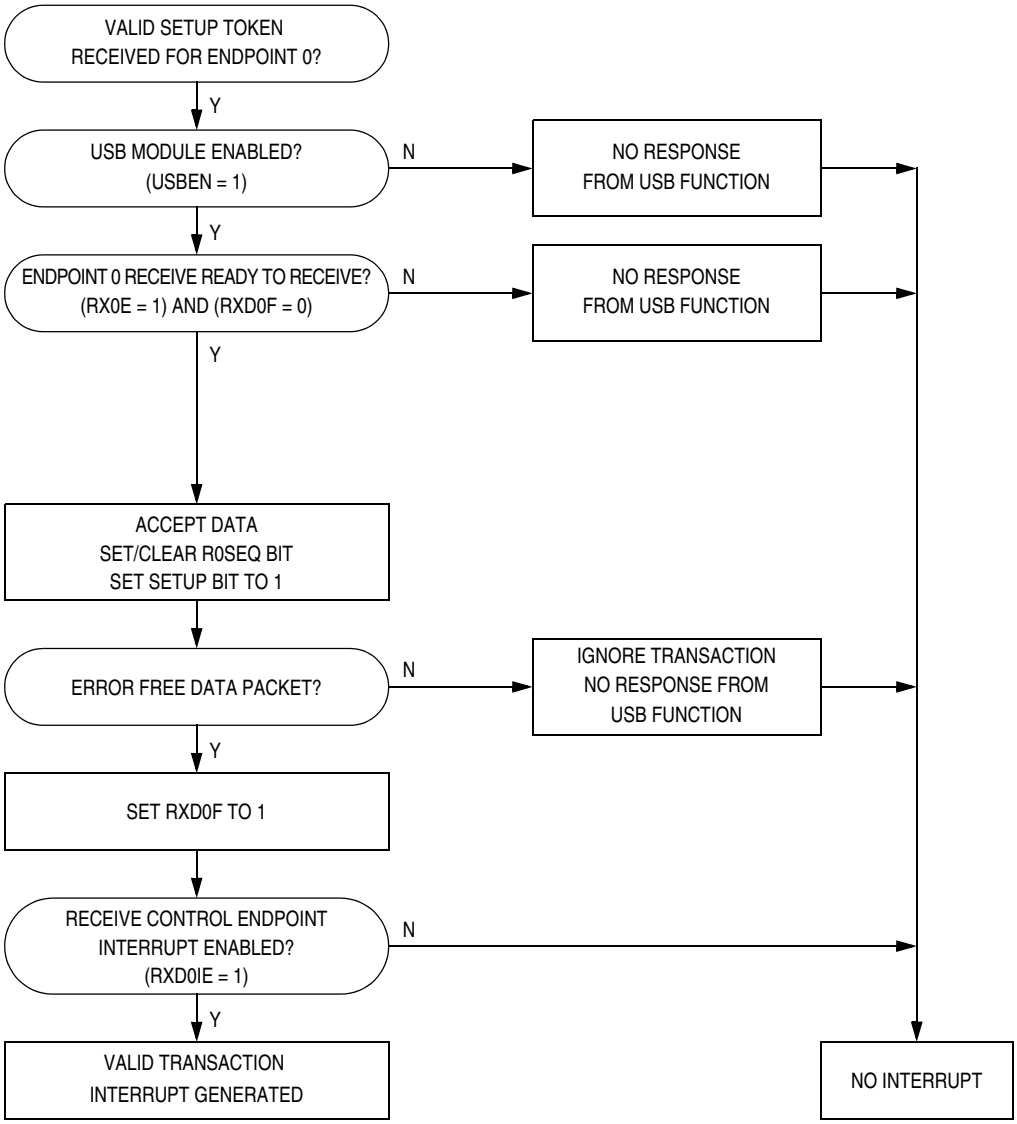

Figure 9-30. SETUP Token Data Flow for Receive Endpoint 0

PTE4P — Pin PTE4 Pullup Enable

This read/write bit controls the pullup option for the PTE4 pin when the pin is configured as an input and the USB module is disabled.

1 = Configure PTE4 to have internal pullup to V_{DD}

0 = Disconnect PTE4 internal pullup

NOTE: *When the USB module is enabled, the pullup controlled by PTE4P is disconnected; PTE4/D– pin functions as D– which has a 1.5kΩ programmable pullup resistor. (See* **9.8.8 USB Control Register 3**.)

PTE3P — Pin PTE3 Pullup Enable

This read/write bit controls the pullup option for the PTE3 pin when the pin is configured as an input and the USB module is disabled.

1 = Configure PTE3 to have internal pullup to V_{DD}

0 = Disconnect PTE3 internal pullup

PCP — Port C Pullup Enable

This read/write bit controls the pullup option for the PTC7–PTC0 pins. When set, a pullup device is connected when a pin is configured as an input.

1 = Configure port C to have internal pullups to V_{REG}

0 = Disconnect port C internal pullups

PBP — Port B Pullup Enable

This read/write bit controls the pullup option for the PTB7–PTB0 pins. When set, a pullup device is connected when a pin is configured as an input.

1 = Configure port B to have internal pullups to V_{REG}

0 = Disconnect port B internal pullups

PAP — Port A Pullup Enable

This read/write bit controls the pullup option for the PTA7–PTA0 pins. When set, a pullup device is connected when a pin is configured as an input.

1 = Configure port A to have internal pullups to V_{REG}

0 = Disconnect port A internal pullups

14.5 Functional Description

Writing to the KBIE7–KBIE0 bits in the keyboard interrupt enable register independently enables or disables each port A pin as a keyboard interrupt pin. Enabling a keyboard interrupt pin also enables its internal pullup device. A logic 0 applied to an enabled keyboard interrupt pin latches a keyboard interrupt request.

A keyboard interrupt is latched when one or more keyboard pins goes low after all were high. The MODEK bit in the keyboard status and control register controls the triggering mode of the keyboard interrupt.

- If the keyboard interrupt is edge-sensitive only, a falling edge on a keyboard pin does not latch an interrupt request if another keyboard pin is already low.
- If the keyboard interrupt is falling edge- and low level-sensitive, an interrupt request is present as long as any keyboard pin is low.

NOTE: *To prevent losing an interrupt request on one pin because another pin is still low, software can disable the latter pin while it is low.*

If the MODEK bit is set, the keyboard interrupt pins are both falling edge- and low level-sensitive, and both of the following actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a logic 1 to the ACKK bit in the keyboard status and control register (KBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt pins and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine also can prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt pins. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the CPU loads the program counter with the vector address at locations $FFF0 and $FFF1.

Section 19. Mechanical Specifications

19.1 Contents

19.2 Introduction

This section gives the dimensions for:

- 44-pin plastic quad flat pack (case 824A)
- 28-pin small outline integrated circuit package (case 751F)
- 20-pin plastic dual in-line package (case 738)
- 20-pin small outline integrated circuit package (case 751D)

Appendix A. MC68HC08JB8

A.1 Contents

B.5 Power Supply Pins

The MC68HC08JT8 is design for low voltage operation. Connect V_{DD} and V_{REG} for normal operation.

The V_{REG} voltage regulator is disabled on the MC68HC08JT8.

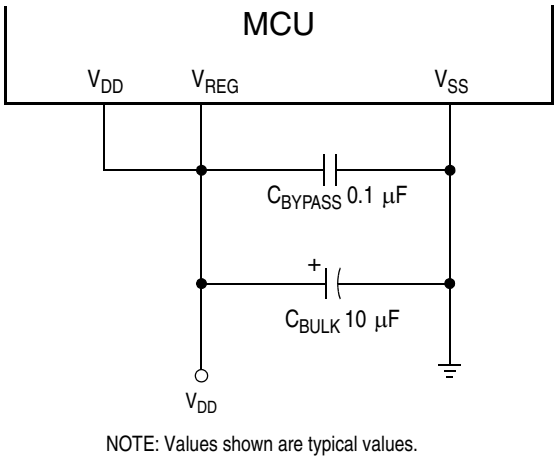

Figure B-3. Power Supply Bypassing

B.6 Reserved Register Bit

Bit 4 of the configuration register ($001F) is a reserved bit on the MC68HC08JT8. The bit will always read as zero.

On the MC68HC908JB8, bit 4 of the configuration register is the low-voltage inhibit disable bit, LVID.

B.7 Reserved Registers

The two registers at $FE08 and $FE09 are reserved locations on the MC68HC08JT8.

On the MC68HC908JB8, these two locations are the FLASH control register and the FLASH block protect register respectively.

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