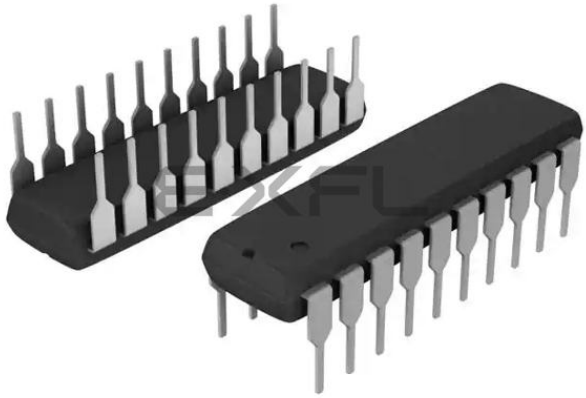

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Details	
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Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908jb8jp

List of Sections

1.5.6 Port A Input/Output (I/O) Pins (PTA7/$\overline{\text{KBA7}}$–PTA0/$\overline{\text{KBA0}}$)

PTA7/$\overline{\text{KBA7}}$–PTA0/$\overline{\text{KBA0}}$ are general-purpose bidirectional I/O port pins. (See **Section 12. Input/Output Ports (I/O)**.) Each pin contains a software configurable pullup device to V_{REG} when the pin is configured as an input. (See **12.8 Port Options**.) Each pin can also be programmed as an external keyboard interrupt pin. (See **Section 14. Keyboard Interrupt Module (KBI)**.)

1.5.7 Port B (I/O) Pins (PTB7–PTB0)

PTB7–PTB0 are general-purpose bidirectional I/O port pins. Each pin contains a software configurable pullup device to V_{REG} when the pin is configured as an input. (See **12.8 Port Options**.)

1.5.8 Port C I/O Pins (PTC7–PTC0)

PTC7–PTC0 are general-purpose bidirectional I/O port pins. (See **Section 12. Input/Output Ports (I/O)**.) Each pin contains a software configurable pullup device to V_{REG} when the pin is configured as an input. (See **12.8 Port Options**.)

1.5.9 Port D I/O Pins (PTD7–PTD0)

PTD7–PTD0 are general-purpose bidirectional I/O port pins; open-drain when configured as output. (See **Section 12. Input/Output Ports (I/O)**.) PTD5–PTD2 are software configurable to be 10mA sink pins for direct LED connections. PTD1–PTD0 are software configurable to be 25mA sink pins for direct infrared LED connections. (See **12.8 Port Options**.)

1.5.10 Port E I/O Pins (PTE4/D–, PTE3/D+, PTE2/TCH1, PTE1/TCH0, PTE0/TCLK)

Port E is a 5-bit special function port that shares two of its pins with the USB module and three of its pins with the timer interface module.

Each PTE2–PTE0 pin contains a software configurable pullup device to V_{REG} when the pin is configured as an input or output.

Table 1-1. Summary of Pin Functions

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
PTC0–PTC7	8-bit general-purpose I/O port.	IN/OUT	V_{REG}
	Each pin has programmable internal pullup to V_{REG} when configured as input.	IN	V_{REG}
PTD0–PTD7	8-bit general-purpose I/O port; open-drain when configured as output.	IN OUT	V_{REG} V_{REG} or V_{DD}
	PTD0–PTD1 have configurable 25mA sink for infrared LED.	OUT	V_{REG} or V_{DD}
	PTD2–PTD5 have configurable 10mA sink for LED.	OUT	V_{REG} or V_{DD}
PTE0/TCLK PTE1/TCH0 PTE2/TCH1	PTE0–PTE2 are general-purpose I/O pins.	IN/OUT	V_{REG}
	PTE0–PTE2 have programmable internal pullup to V_{REG} when configured as input or output.	IN/OUT	V_{REG}
	PTE0 as TCLK of timer interface module.	IN	V_{REG}
	PTE1 as TCH0 of timer interface module.	IN/OUT	V_{REG}
	PTE2 as TCH1 of timer interface module.	IN/OUT	V_{REG}
PTE3/D+ PTE4/D–	PTE3–PTE4 are general-purpose I/O pins; open-drain when configured as output.	IN OUT	V_{DD} V_{REG} or V_{DD}
	PTE3–PTE4 have programmable internal pullup to V_{DD} when configured as input.	IN	V_{DD}
	PTE3 as D+ of USB module.	IN/OUT	V_{REG}
	PTE4 as D– of USB module.	IN/OUT	V_{REG}
	PTE4 as additional IRQ interrupt.	IN	V_{DD}

2.3 I/O Section

Addresses $0000–$003F, shown in **Figure 2-2,** contain most of the control, status, and data registers. Additional I/O registers have these addresses:

- $FE00; break status register, BSR
- $FE01; reset status register, RSR
- $FE02; reserved
- $FE03; break flag control register, BFCR
- $FE04; interrupt status register 1, INT1
- $FE05; reserved
- $FE06; reserved
- $FE07; reserved
- $FE08; FLASH control register, FLCR
- $FE09; FLASH block protect register, FLBPR
- $FE0A; reserved
- $FE0B; reserved
- $FE0C; break Address Register High, BRKH
- $FE0D; break Address Register Low, BRKL
- $FE0E; break status and control register, BRKSCR
- $FFFF; COP control register, COPCTL

2.4 Monitor ROM

The 512 bytes at addresses $FC00–$FDFF and 464 bytes at addresses $FE10–$FFDF are reserved ROM addresses that contain the instructions for the monitor functions. (See **Section 10. Monitor ROM (MON)**.)

Table 6-1. Instruction Set Summary (Sheet 5 of 9)

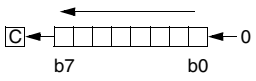
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X EOR *opr*,SP EOR *opr*,SP	Exclusive OR M with A	A ← (A ⊕ M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A8 B8 C8 D8 E8 F8 9EE8 9ED8	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
INC *opr* INCA INCX INC *opr*,X INC ,X INC *opr*,SP	Increment	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1 M ← (M) + 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd ff ff	4 1 1 4 3 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Jump	PC ← Jump Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff 	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + *n* (*n* = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Unconditional Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff 	4 5 6 5 4
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X LDA *opr*,SP LDA *opr*,SP	Load A from M	A ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
LDHX #*opr* LDHX *opr*	Load H:X from M	H:X ← (M:M + 1)	0	–	–	↕	↕	–	IMM DIR	45 55	ii jj dd	3 4
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X LDX *opr*,SP LDX *opr*,SP	Load X from M	X ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
LSL *opr* LSLA LSLX LSL *opr*,X (Same as ASL) LSL ,X LSL *opr*,SP	Logical Shift Left  		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5

Table 6-1. Instruction Set Summary (Sheet 9 of 9)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				

A	Accumulator	*n*	Any bit
C	Carry/borrow bit	*opr*	Operand (one or two bytes)
CCR	Condition code register	PC	Program counter
dd	Direct address of operand	PCH	Program counter high byte
dd rr	Direct address of operand and relative offset of branch instruction	PCL	Program counter low byte
DD	Direct to direct addressing mode	REL	Relative addressing mode
DIR	Direct addressing mode	*rel*	Relative program counter offset byte
DIX+	Direct to indexed with post increment addressing mode	rr	Relative program counter offset byte
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing	SP1	Stack pointer, 8-bit offset addressing mode
EXT	Extended addressing mode	SP2	Stack pointer 16-bit offset addressing mode
ff	Offset byte in indexed, 8-bit offset addressing	SP	Stack pointer
H	Half-carry bit	U	Undefined
H	Index register high byte	V	Overflow bit
hh ll	High and low bytes of operand address in extended addressing	X	Index register low byte
I	Interrupt mask	Z	Zero bit
ii	Immediate operand byte	&	Logical AND
IMD	Immediate source to direct destination addressing mode	|	Logical OR
IMM	Immediate addressing mode	⊕	Logical EXCLUSIVE OR
INH	Inherent addressing mode	( )	Contents of
IX	Indexed, no offset addressing mode	–( )	Negation (two's complement)
IX+	Indexed, no offset, post increment addressing mode	#	Immediate value
IX+D	Indexed with post increment to direct addressing mode	«	Sign extend
IX1	Indexed, 8-bit offset addressing mode	←	Loaded with
IX1+	Indexed, 8-bit offset, post increment addressing mode	?	If
IX2	Indexed, 16-bit offset addressing mode	:	Concatenated with
M	Memory location	↕	Set or cleared
N	Negative bit	—	Not affected

6.9 Opcode Map

See **Table 6-2**.

7.3 Oscillator External Connections

In its typical configuration, the oscillator requires five external components. The crystal oscillator is normally connected in a Pierce oscillator configuration, as shown in **Figure 7-1**. This figure shows only the logical representation of the internal components and may not represent actual circuitry. The oscillator configuration uses five components:

- Crystal, X_1
- Fixed capacitor, C_1
- Tuning capacitor, C_2 (can also be a fixed capacitor)
- Feedback resistor, R_B
- Series resistor, R_S (optional)

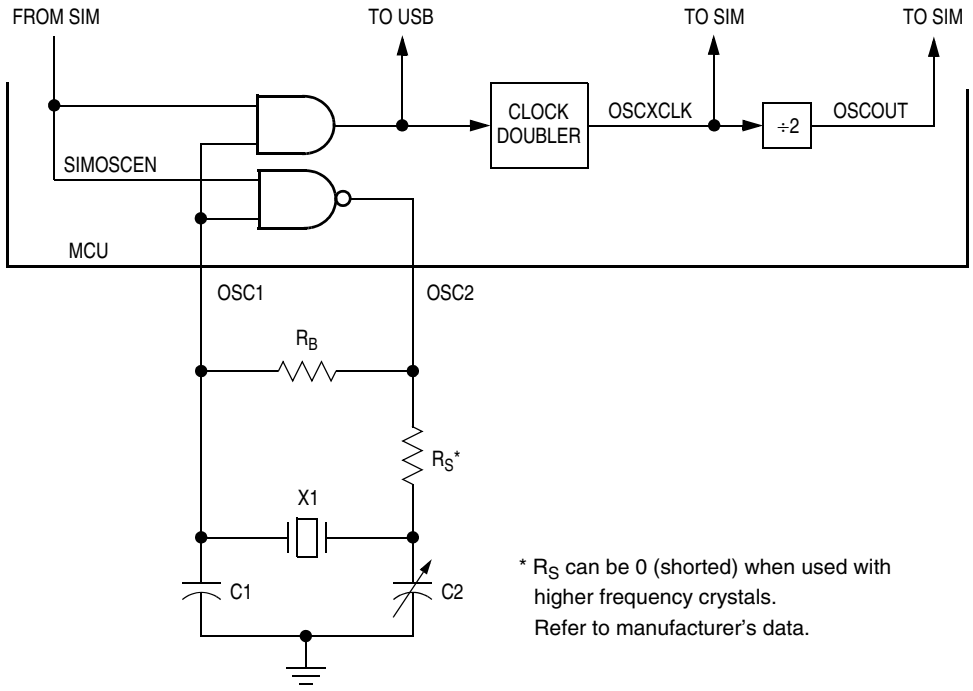


Figure 7-1. Oscillator External Connections

8.6.1.2 SWI Instruction

The SWI instruction is a non-maskable instruction that causes an interrupt regardless of the state of the interrupt mask (I bit) in the condition code register.

NOTE: *A software interrupt pushes PC onto the stack. A software interrupt does* ***not*** *push PC–1, as a hardware interrupt does.*

8.6.2 Interrupt Status Registers

The flags in the interrupt status registers identify maskable interrupt sources. **Table 8-4** summarizes the interrupt sources and the interrupt status register flags that they set. The interrupt status registers can be useful for debugging.

Table 8-4. Interrupt Sources

Source	Flags	Mask[1]	INT Register Flag	Priority[2]	Vector Address
SWI Instruction			—	0	$FFFC–$FFFD
USB Reset Interrupt	RSTF	URSTD	IF2	1	$FFFA–$FFFB
USB Endpoint 0 Transmit	TXD0F	TXD0IE			
USB Endpoint 0 Receive	RXD0F	RXD0IE			
USB Endpoint 1 Transmit	TXD1F	TXD1IE			
USB Endpoint 2 Transmit	TXD2F	TXD2IE			
USB Endpoint 2 Receive	RXD2F	RXD2IE			
USB End of Packet	EOPF	EOPIE			
USB Resume Interrupt	RESUMF	—			
IRQ Interrupt ($\overline{\text{IRQ}}$, PTE4)	IRQF PTE4IF	IMASK	IF1	2	$FFF8–$FFF9
TIM Channel 0	CH0F	CH0IE	IF3	3	$FFF6–$FFF7
TIM Channel 1	CH1F	CH1IE	IF4	4	$FFF4–$FFF5
TIM Overflow	TOF	TOIE	IF5	5	$FFF2–$FFF3
Keyboard Interrupt	KEYF	IMASKK	IF6	6	$FFF0–$FFF1

1. The I bit in the condition code register is a global mask for all interrupt sources except the SWI instruction.
2. 0 = highest priority

8.6.5 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are protected from being cleared by properly initializing the break clear flag enable bit (BCFE) in the break flag control register (BFCR).

Protecting flags in break mode ensures that set flags will not be cleared while in break mode. This protection allows registers to be freely read and written during break mode without losing status flag information.

Setting the BCFE bit enables the clearing mechanisms. Once cleared in break mode, a flag remains cleared even when break mode is exited. Status flags with a 2-step clearing mechanism — for example, a read of one register followed by the read or write of another — are protected, even when the first step is accomplished prior to entering break mode. Upon leaving break mode, execution of the second step will clear the flag as normal.

8.7 Low-Power Modes

Executing the WAIT or STOP instruction puts the MCU in a low-power-consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described here. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

8.7.1 Wait Mode

In wait mode, the CPU clocks are inactive while the peripheral clocks continue to run. **Figure 8-13** shows the timing for wait mode entry.

A module that is active during wait mode can wake up the CPU with an interrupt if the interrupt is enabled. Stacking for the interrupt begins one cycle after the WAIT instruction during which the interrupt occurred. In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

9.8.9 USB Control Register 4

USB control register 4 directly controls the USB data pins D+ and D–. If the FUSBO bit, and the USBEN bit of the USB address register (UADDR) are set, the output buffers of the USB modules are enabled and the corresponding levels of the USB data pins D+ and D– are equal to the values set by the FDP and the FDM bits.

Address: $001B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	FUSBO	FDP	FDM
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-23. USB Control Register 4 (UCR4)

FUSBO — Force USB Output

This read/write bit enables the USB output buffers.

1 = Enables USB output buffers
0 = USB module in normal operation

FDP — Force D+

This read/write bit determinates the output level of D+.

1 = D+ at output high level
0 = D+ at output low level

FDM — Force D–

This read/write bit determinates the output level of D–.

1 = D– at output high level
0 = D– at output low level

NOTE: *Customers must be very careful when setting the UCR4 register. When the FUSBO and the USBEN bits are set, the USB module is in output mode and it will not recognize any USB signals including the USB reset signal. The UCR4 register is used for some special applications. Customers are not normally expected to use this register.*

10.4.3 Data Format

Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. (See **Figure 10-3** and **Figure 10-4**.)

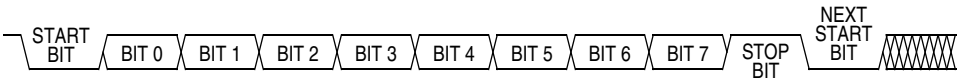


Figure 10-3. Monitor Data Format

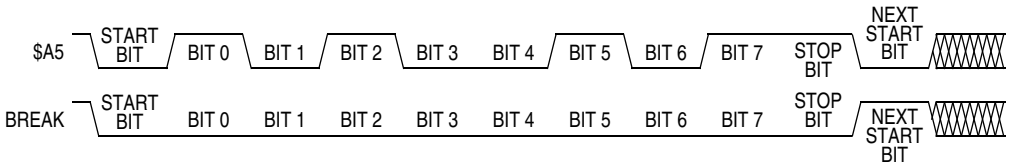


Figure 10-4. Sample Monitor Waveforms

The data transmit and receive rate can be anywhere from 4800 baud to 28.8k-baud. Transmit and receive baud rates must be identical.

10.4.4 Echoing

As shown in **Figure 10-5**, the monitor ROM immediately echoes each received byte back to the PTA0 pin for error checking.

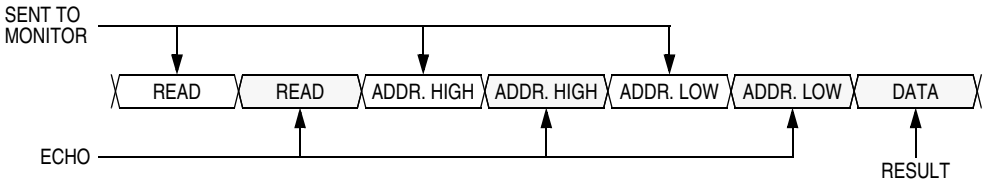


Figure 10-5. Read Transaction

Any result of a command appears after the echo of the last byte of the command.

Section 11. Timer Interface Module (TIM)

11.1 Contents

11.10.1 TIM Status and Control Register

The TIM status and control register:

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

= Unimplemented

Figure 11-4. TIM Status and Control Register (TSC)

TOF — TIM Overflow Flag Bit

This read/write flag is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TIM status and control register when TOF is set and then writing a logic 0 to TOF. If another TIM overflow occurs before the clearing sequence is complete, then writing logic 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a logic 1 to TOF has no effect.

1 = TIM counter has reached modulo value
0 = TIM counter has not reached modulo value

TOIE — TIM Overflow Interrupt Enable Bit

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM overflow interrupts enabled
0 = TIM overflow interrupts disabled

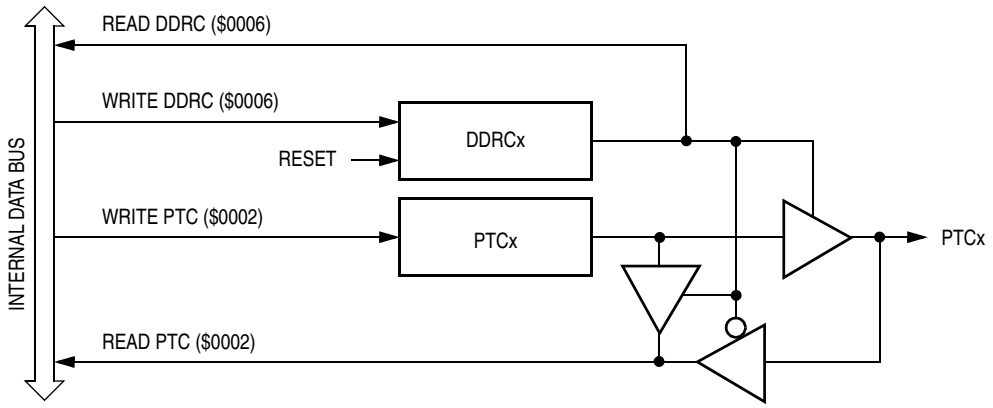


Figure 12-10. Port C I/O Circuit

When bit DDRCx is a logic 1, reading address $0002 reads the PTCx data latch. When bit DDRCx is a logic 0, reading address $0002 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. **Table 12-4** summarizes the operation of the port C pins.

Table 12-4. Port C Pin Functions

DDRC Bit	PTC Bit	I/O Pin Mode	Accesses to DDRC	Accesses to PTC	
			Read/Write	Read	Write
0	X(1)	Input, Hi-Z(2)	DDRC[7:0]	Pin	PTC[7:0](3)
1	X	Output	DDRC[7:0]	PTC[7:0]	PTC[7:0]

NOTES:
1. X = don't care.
2. Hi-Z = high impedance.
3. Writing affects data register, but does not affect input.

12.6 Port D

Port D is an 8-bit general-purpose bidirectional I/O port. In 20-pin package, PTD1 and PTD0 internal pads are bonded together to PTD0/1 pin. Port D pins are open-drain when configured as output, and can interface with 5V logic.

12.6.2 Data Direction Register D

Data direction register D determines whether each port D pin is an input or an output. Writing a logic 1 to a DDRD bit enables the output buffer for the corresponding port D pin; a logic 0 disables the output buffer.

Address: $0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Reset:	0	0	0	0	0	0	0	0

Figure 12-12. Data Direction Register D (DDRD)

DDRD[7:0] — Data Direction Register D Bits

These read/write bits control port D data direction. Reset clears DDRD[7:0], configuring all port D pins as inputs.

1 = Corresponding port D pin configured as output
0 = Corresponding port D pin configured as input

Port D pins are open-drain when configured as output.

NOTE: *Avoid glitches on port D pins by writing to the port D data register before changing data direction register D bits from 0 to 1.*

NOTE: *For those devices packaged in a 20-pin PDIP and 20-pin SOIC package, PTD7–PTD2 are not connected. DDRD7–DDRD2 should be set to a 1 to configure PTD7–PTD2 as outputs.*
For those devices packaged in a 28-pin SOIC package, PTD7 is not connected. DDRD7 should be set to a 1 to configure PTD7 as output.

Figure 12-13 shows the port D I/O circuit logic.

12.7.1 Port E Data Register

The port E data register contains a data latch for each of the five port E pins.

NOTE: *PTE2 and PTE0 are not available in the 20-pin PDIP and 20-pin SOIC packages.*

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	PTE4	PTE3	PTE2	PTE1	PTE0
Write:								
Reset:	Unaffected by reset							
Alternative Function:				D–	D+	TCH1	TCH0	TCLK
Additional Function:				Optional pullup	Optional pullup	Optional pullup	Optional pullup	Optional pullup
Additional Function:				External interrupt				
				Open-drain	Open-drain			

= Unimplemented

Figure 12-14. Port E Data Register (PTE)

PTE[4:0] — Port E Data Bits

PTE[4:0] are read/write, software-programmable bits. Data direction of each port E pin is under the control of the corresponding bit in data direction register E.

The PTE4 and PTE3 pullup enable bits, PTE4P and PTE3P, in the port option control register (POCR) enable 5kΩ pullups on PTE4 and PTE3 if the respective pin is configured as an input and the USB module is disabled. (See **12.8 Port Options**.)

The PTE[2:0] pullup enable bit, PTE20P, in the port option control register (POCR) enables pullups on PTE2–PTE0, regardless of the pin is configured as an input or an output. (See **12.8 Port Options**.)

12.8.1 Port Option Control Register

The port option control register controls the pullup options for port A, B, C, and E pins. It also controls the drive configuration on port D.

Address: $001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTE20P	PTDLDD	PTDILDD	PTE4P	PTE3P	PCP	PBP	PAP
Reset:	0	0	0	0	0	0	0	0

Figure 12-17. Port Option Control Register (POCR)

PTE20P — Port PTE2–PTE0 Pullup Enable

This read/write bit controls the pullup option for the PTE2–PTE0 pins, regardless whether the pins are input or output.

1 = Configure PTE2–PTE0 to have internal pullups to V_{REG}

0 = Disconnect PTE2–PTE0 internal pullups

PTDLDD — LED Direct Drive Control

This read/write bit controls the output current capability of PTD5–PTD2 pins. When set, each port pin has 10mA current sink limit. An LED can be connected directly between the port pin and V_{DD} without the need of a series resistor.

1 = PTD5–PTD2 configured for direct LED drive capability; when a pin is set as an output, the pin is an open-drain pin with 10mA current sink limit

0 = PTD5–PTD2 configured as standard open-drain I/O port pin

PTDILDD — Infrared LED Drive Control

This read/write bit controls the output current capability of PTD1 and PTD0 pins. When set, each port pin has 25mA current sink capability. An infrared LED can be connected directly between the port pin and V_{DD}.

1 = PTD1 and PTD0 configured for infrared LED drive capability; when a pin is set as an output, the pin is an open-drain pin with 25mA current sink capability

0 = PTD1 and PTD0 configured as standard open-drain I/O port pins

Use the BIH or BIL instruction to read the logic level on the $\overline{IRQ}$ pin.

NOTE: *When using the level-sensitive interrupt trigger, avoid false interrupts by masking interrupt requests in the interrupt routine.*

NOTE: *An internal pullup resistor to V_{DD} is connected to $\overline{IRQ}$ pin; this can be disabled by setting the IRQPD bit in the IRQ option control register ($001C).*

13.6 PTE4/D– Pin

The PTE4 pin is configured as an interrupt input to trigger the IRQ interrupt when the following conditions are satisfied:

- The USB module is disabled (USBEN = 0)
- PTE4 pin configured for external interrupt input (PTE4IE = 1)

Setting PTE4IE configures the PTE4 pin to an input pin with an internal pullup device. The PTE4 interrupt is "ORed" with the $\overline{IRQ}$ input to trigger the IRQ interrupt (see **Figure 13-1 . IRQ Module Block Diagram**). Therefore, the IRQ status and control register affects both the $\overline{IRQ}$ pin and the PTE pin. An interrupt on PTE4 also sets the PTE4 interrupt flag, PTE4IF, in the IRQ option control register (IOCR).

13.7 IRQ Module During Break Interrupts

The system integration module (SIM) controls whether the IRQ latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear the latches during the break state. (See **Section 8. System Integration Module (SIM)**.)

To allow software to clear the IRQ latch during a break interrupt, write a logic 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latches during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), writing to the ACK bit in the IRQ status and control register during the break state has no effect on the IRQ latch.

- Return of all enabled keyboard interrupt pins to logic 1 — As long as any enabled keyboard interrupt pin is at logic 0, the keyboard interrupt remains set.

The vector fetch or software clear and the return of all enabled keyboard interrupt pins to logic 1 may occur in any order.

If the MODEK bit is clear, the keyboard interrupt pin is falling-edge-sensitive only. With MODEK clear, a vector fetch or software clear immediately clears the keyboard interrupt request.

Reset clears the keyboard interrupt request and the MODEK bit, clearing the interrupt request even if a keyboard interrupt pin stays at logic 0.

The keyboard flag bit (KEYF) in the keyboard status and control register can be used to see if a pending interrupt exists. The KEYF bit is not affected by the keyboard interrupt mask bit (IMASKK) which makes it useful in applications where polling is preferred.

To determine the logic level on a keyboard interrupt pin, use the data direction register to configure the pin as an input and read the data register.

NOTE: *Setting a keyboard interrupt enable bit (KBIEx) forces the corresponding keyboard interrupt pin to be an input, overriding the data direction register. However, the data direction register bit must be a logic 0 for software to read the pin.*

14.6 Keyboard Initialization

When a keyboard interrupt pin is enabled, it takes time for the pullup device to reach a logic 1. Therefore, a false interrupt can occur as soon as the pin is enabled.

To prevent a false interrupt on keyboard initialization:

1. Mask keyboard interrupts by setting the IMASKK bit in the keyboard status and control register.
2. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.

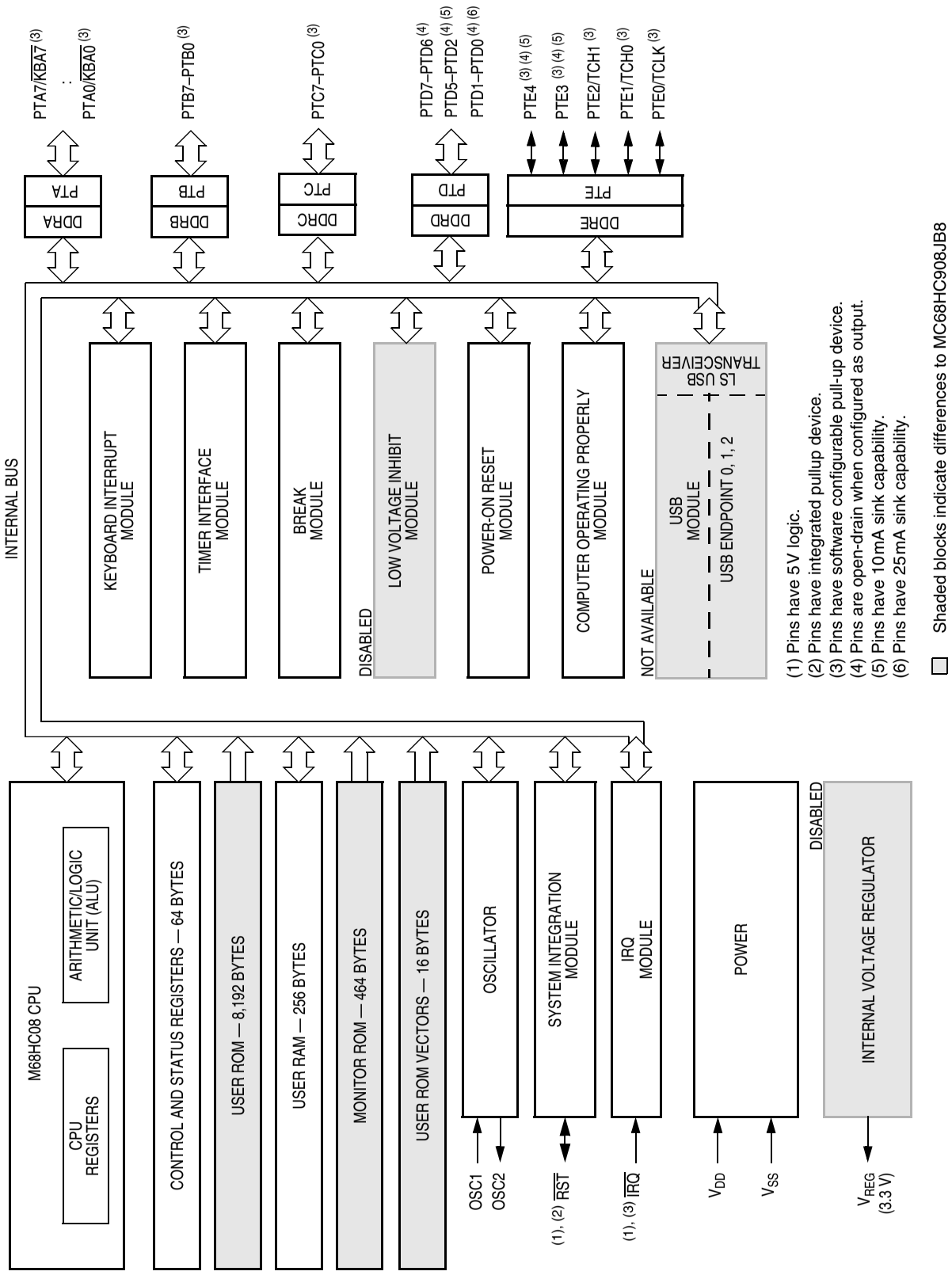


Figure B-1. MC68HC08JT8 Block Diagram