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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f914-i-ml

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	- • ·										
I/O	Pin	A/D	LCD	Comparators	Timers	ССР	AUSART	SSP	Interrupt	Pull-Up	Basic
RF3	14		SEG35	_					_	_	
RF4	45		SEG28	_					_	_	
RF5	46		SEG29	_					_	_	
RF6	47	_	SEG30	_	_	_	_	_	_	_	_
RF7	48	_	SEG31	_	_		_	_	_	_	_
RG0	3	_	SEG36	_	_	_	_	_	_	_	_
RG1	4	_	SEG37	_	_	_	_	_	—	_	_
RG2	5	_	SEG38	_	_	_	_	_	—	_	_
RG3	6	_	SEG39	_	_	_	_	_	—	_	_
RG4	7	_	SEG40	_	—	_		_	—	—	_
RG5	8	_	SEG41	_	_	_	_	_	—	_	_
_	26	—	—	_	—	_	_	_	—	—	AVDD
_	25	_	_	_	_	_	_	_	—	_	AVss
_	10	_	_	_	_	_	_	_	_	_	Vdd
_	19	_	_	_	_		_	_	_	_	Vdd
_	38	_	_	_	_	_	_	_	_	_	Vdd
_	57	_	_	_	_		_	_	_	_	Vdd
_	9	_	_	_	_	_	_	_	_	_	Vss
_	20		_	_	—				_	_	Vss
_	41	_	_	_	_	_	_	_	_	_	Vss
_	56	_	_	_	_	_	_	_	_	_	Vss

TABLE 6: PIC16F946 64-PIN (TQFP) SUMMARY (CONTINUED)

Note 1: Pull-up enabled only with external MCLR configuration.

1.0 DEVICE OVERVIEW

The PIC16F91X/946 devices are covered by this data sheet. They are available in 28/40/44/64-pin packages. Figure 1-1 shows a block diagram of the PIC16F913/916 device, Figure 1-2 shows a block diagram of the PIC16F914/917 device, and Figure 1-3 shows a block diagram of the PIC16F946 device. Table 1-1 shows the pinout descriptions.





	File		File		File		File
	Address		Address		Address		Addres
ndirect addr. ⁽¹⁾	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. ⁽¹⁾	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	LCDCON	107h		187h
	08h		88h	LCDPS	108h		188h
PORTE	09h	TRISE	89h	LVDCON	109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATL	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADRL	10Dh	EECON2 ⁽¹⁾	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCTUNE	90h	LCDDATA0	110h		190h
TMR2	11h	ANSEL	91h	LCDDATA1	111h		
T2CON	12h	PR2	92h		112h		
SSPBUF	13h	SSPADD	93h	LCDDATA3	113h		
SSPCON	14h	SSPSTAT	94h	LCDDATA4	114h		
CCPR1L	15h	WPUB	95h		115h		
CCPR1H	16h	IOCB	96h	LCDDATA6	116h		
CCP1CON	17h	CMCON1	97h	LCDDATA7	117h		
RCSTA	18h	TXSTA	98h		118h		
TXREG	19h	SPBRG	99h	LCDDATA9	119h	General	
RCREG	1Ah		9Ah	LCDDATA10	11Ah	Purpose	
	1Bh		9Bh		11Bh	Register ⁽²⁾	
	1Ch	CMCON0	9Ch	LCDSE0	11Ch		
	1Dh	VRCON	9Dh	LCDSE1	11Dh	96 Bytes	
ADRESH	1Eh	ADRESL	9Eh		11Eh		
ADCON0	1Fh	ADCON1	9Fh		11Fh		
	20h		A0h		120h		
		General		General			
General		Purpose		Purpose			
Purpose		Register		Register			
Register							
		80 Bytes		80 Bytes			
96 Bytes			EFh		16Fh		1EFh
		accesses	F0h	accesses	170h	accesses	1F0h
	7Fh	70h-7Fh	FFh	70h-7Fh	17Fh	70h-7Fh	1FFh
Bank 0	-	Bank 1	1	Bank 2		Bank 3	I

Note 1: Not a physical register.

2: On the PIC16F913, unimplemented data memory locations, read as '0'.

3.4.3 PIN DESCRIPTIONS AND DIAGRAMS

Each PORTB pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the LCD or interrupts, refer to the appropriate section in this data sheet.

3.4.3.1 RB0/INT/SEG0

Figure 3-9 shows the diagram for this pin. The RB0 pin is configurable to function as one of the following:

- a general purpose I/O
- · an external edge triggered interrupt
- an analog output for the LCD

3.4.3.2 RB1/SEG1

Figure 3-9 shows the diagram for this pin. The RB1 pin is configurable to function as one of the following:

- a general purpose I/O
- · an analog output for the LCD

3.4.3.3 RB2/SEG2

Figure 3-9 shows the diagram for this pin. The RB2 pin is configurable to function as one of the following:

- a general purpose I/O
- · an analog output for the LCD

3.4.3.4 RB3/SEG3

Figure 3-9 shows the diagram for this pin. The RB3 pin is configurable to function as one of the following:

- a general purpose I/O
- · an analog output for the LCD



FIGURE 3-9: BLOCK DIAGRAM OF RB<3:0>

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP2CON ⁽¹⁾	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
LCDCON	LCDEN	SLPEN	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE2 ⁽¹⁾	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000	uuuu uuuu
PORTD ⁽¹⁾	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	XXXX XXXX	uuuu uuuu
TRISD ⁽¹⁾	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	1111 1111

TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD⁽¹⁾

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

Note 1: PIC16F914/917 and PIC16F946 only.

TABLE 3-5: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	ADFM	VCFG1	VCFG0	CHS2	CHS1	CHS0	GO/DONE	ADON	0000 0000	0000 0000
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
LCDCON	LCDEN	SLPEN	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE2 ^(1,2)	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000	uuuu uuuu
LCDSE3 ^(1, 3)	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	0000 0000	uuuu uuuu
PORTE	RE7 ⁽³⁾	RE6 ⁽³⁾	RE5 ⁽³⁾	RE4 ⁽³⁾	RE3	RE2 ⁽²⁾	RE1 ⁽²⁾	RE0 ⁽²⁾	xxxx xxxx	uuuu uuuu
TRISE	TRISE7 ⁽³⁾	TRISE6 ⁽³⁾	TRISE5 ⁽³⁾	TRISE4 ⁽³⁾	TRISE3 ⁽⁴⁾	TRISE2 ⁽²⁾	TRISE1 ⁽²⁾	TRISE0 ⁽²⁾	1111 1111	1111 1111

x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC. This register is only initialized by a POR or BOR reset and is unchanged by other Resets. PIC16F914/917 and PIC16F946 only. Legend: Note 1:

2:

3: PIC16F946 only.

4: Bit is read-only; TRISE = 1 always.

3.9 PORTG and TRISG Registers

PORTG is an 8-bit port with Schmitt Trigger input buffers. RG<5:0> are individually configured as inputs or outputs, depending on the state of the port direction. The port bits are also multiplexed with LCD segment functions. PORTG is available on the PIC16F946 only.

EXAMPLE 3-7: INITIALIZING PORTG

BANKSEL	PORTG	;
CLRF	PORTG	;Init PORTG
BANKSEL	TRISG	;
MOVLW	3Fh	;Set RG<5:0> as inputs
MOVWF	TRISG	;

REGISTER 3-16: PORTG: PORTG REGISTER⁽¹⁾

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	RG5	RG4	RG3	RG2	RG1	RG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

on perienced. Read as 0

bit 5-0 **RG<5:0>**: PORTG I/O Pin bits 1 = Port pin is >VIH min. 0 = Port pin is <VIL max.

Note 1: PIC16F946 only.

REGISTER 3-17: TRISG: PORTG TRI-STATE REGISTER⁽¹⁾

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TRISG5	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **TRISF<5:0>:** PORTG Tri-State Control bits 1 = PORTG pin configured as an input (tri-stated)

0 = PORTG pin configured as an output

Note 1: PIC16F946 only.

4.4.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 4-5 shows the external RC mode connections.

Vdd PIC[®] MCU REXT OSC1/CLKIN Internal Clock CEXT Vss -Fosc/4 or OSC2/CLKOUT⁽¹⁾ I/O⁽²⁾ Recommended values: 10 k $\Omega \le REXT \le 100 k\Omega$, <3V $3 \text{ k}\Omega \leq \text{REXT} \leq 100 \text{ k}\Omega, 3-5\text{V}$ CEXT > 20 pF, 2-5V Note 1: Alternate pin functions are listed in Section 1.0 "Device Overview". 2: Output depends upon RC or RCIO clock mode.

FIGURE 4-5: EXTERNAL RC MODES

In RCIO mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- · threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

4.5 Internal Clock Modes

The Oscillator module has two independent, internal oscillators that can be configured or selected as the system clock source.

- 1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 8 MHz. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 4-2).
- 2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<2:0> of the OSCCON register.

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit of the OSCCON register. See **Section 4.6 "Clock Switching"** for more information.

4.5.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the Configuration Word register (CONFIG). See **Section 16.0 "Special Features of the CPU"** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCIO** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

4.5.2 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 8 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 4-2).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 4-1). One of seven frequencies can be selected via software using the IRCF<2:0> bits of the OSCCON register. See **Section 4.5.4 "Frequency Select Bits (IRCF)"** for more information.

The HFINTOSC is enabled by selecting any frequency between 8 MHz and 125 kHz by setting the IRCF<2:0> bits of the OSCCON register \neq 000. Then, set the System Clock Source (SCS) bit of the OSCCON register to '1' or enable Two-Speed Start-up by setting the IESO bit in the Configuration Word register (CONFIG) to '1'.

The HF Internal Oscillator (HTS) bit of the OSCCON register indicates whether the HFINTOSC is stable or not.

4.6 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit of the OSCCON register.

4.6.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bit of the OSCCON register = 0, the system clock source is determined by configuration of the FOSC<2:0> bits in the Configuration Word register (CONFIG).
- When the SCS bit of the OSCCON register = 1, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<2:0> bits of the OSCCON register. After a Reset, the SCS bit of the OSCCON register is always cleared.
- Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit of the OSCCON register. The user can monitor the OSTS bit of the OSCCON register to determine the current system clock source.

4.6.2 OSCILLATOR START-UP TIME-OUT STATUS (OSTS) BIT

The Oscillator Start-up Time-out Status (OSTS) bit of the OSCCON register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

4.7 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note: Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCCON register to remain clear. When the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see **Section 4.4.1 "Oscillator Start-up Timer (OST)"**). The OST will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit of the OSCCON register is set, program execution switches to the external oscillator.

4.7.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Word register) = 1; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = 0.
- FOSC<2:0> bits in the Configuration Word register (CONFIG) configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

4.7.2 TWO-SPEED START-UP SEQUENCE

- 1. Wake-up from Power-on Reset or Sleep.
- 2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF<2:0> bits of the OSCCON register.
- 3. OST enabled to count 1024 clock cycles.
- 4. OST timed out, wait for falling edge of the internal oscillator.
- 5. OSTS is set.
- 6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
- 7. System clock is switched to external clock source.

9.4 AUSART Operation During Sleep

The AUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

9.4.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see Section 9.3.2.4 "Synchronous Slave Reception Set-up:").
- If interrupts are desired, set the RCIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE global interrupt enable bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

9.4.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Transmission (see Section 9.3.2.2 "Synchronous Slave Transmission Set-up:").
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE global interrupt enable bit is also set then the Interrupt Service Routine at address 0004h will be called.



FIGURE 10-7: TYPE-A WAVEFORMS IN 1/2 MUX, 1/2 BIAS DRIVE



10.10 Operation During Sleep

The LCD module can operate during Sleep. The selection is controlled by bit SLPEN of the LCDCON register. Setting the SLPEN bit allows the LCD module to go to Sleep. Clearing the SLPEN bit allows the module to continue to operate during Sleep.

If a SLEEP instruction is executed and $\overline{\text{SLPEN}} = 1$, the LCD module will cease all functions and go into a very low-current Consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 10-18 shows this operation.

To ensure that no DC component is introduced on the panel, the SLEEP instruction should be executed immediately after a LCD frame boundary. For Type-B multiplex (non-static), the LCD interrupt can be used to determine the frame boundary. See **Section 10.9 "LCD Interrupts"** for the formulas to calculate the delay. In all other modes, the LCDA bit can be used to determine when the display is active. To use this method, the following sequence should be used when wanting to enter into Sleep mode:

- Clear LCDEN
- Wait for LCDA to clear
- Drive all LCD pins to inactive state using PORT and TRIS registers
- Execute **SLEEP** instruction

Note:	When the LCDEN bit is cleared, the LCD
	module will be disabled at the completion
	of frame. At this time, the PORT pins will
	revert to digital functionality. To minimize
	power consumption due to floating digital
	inputs, the LCD pins should be driven low
	using the PORT and TRIS registers.

If a SLEEP instruction is executed and $\overline{\text{SLPEN}} = 0$, the module will continue to display the current contents of the LCDDATA registers. To allow the module to continue operation while in Sleep, the clock source must be either the LFINTOSC or T1OSC external oscillator. While in Sleep, the LCD data cannot be changed. The LCD module current consumption will not decrease in this mode; however, the overall consumption of the device will be lower due to shut down of the core and other peripheral functions.

Table 10-5 shows the status of the LCD module during a Sleep while using each of the three available clock sources:

TABLE 10-5:	LCD MODULE STATUS
	DURING SLEEP

Clock Source	SLPEN	Operation During Sleep?
T1090	0	Yes
11030	1	No
	0	Yes
LFINTUSC	1	No
Eosc/4	0	No
FUSC/4	1	No

Note:	The	LFINTOSC	or	external	T10SC			
oscillator must be used to operate the LCI								
module during Sleep.								

If LCD interrupts are being generated (Type-B waveform with a multiplex mode not static) and LCDIE = 1, the device will awaken from Sleep on the next frame boundary.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CMCON0	C2OUT	C10UT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
LCDCON	LCDEN	SLPEN	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDDATA0	SEG7 COM0	SEG6 COM0	SEG5 COM0	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0	XXXX XXXX	uuuu uuuu
LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	SEG12 COM0	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0	XXXX XXXX	uuuu uuuu
LCDDATA2 ⁽²⁾	SEG23 COM0	SEG22 COM0	SEG21 COM0	SEG20 COM0	SEG19 COM0	SEG18 COM0	SEG17 COM0	SEG16 COM0	XXXX XXXX	uuuu uuuu
LCDDATA3	SEG7 COM1	SEG6 COM1	SEG5 COM1	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1	XXXX XXXX	uuuu uuuu
LCDDATA4	SEG15 COM1	SEG14 COM1	SEG13 COM1	SEG12 COM1	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1	XXXX XXXX	uuuu uuuu
LCDDATA5 ⁽²⁾	SEG23 COM1	SEG22 COM1	SEG21 COM1	SEG20 COM1	SEG19 COM1	SEG18 COM1	SEG17 COM1	SEG16 COM1	XXXX XXXX	uuuu uuuu
LCDDATA6	SEG7 COM2	SEG6 COM2	SEG5 COM2	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2	XXXX XXXX	uuuu uuuu
LCDDATA7	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2	XXXX XXXX	uuuu uuuu
LCDDATA8 ⁽²⁾	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2	XXXX XXXX	uuuu uuuu
LCDDATA9	SEG7 COM3	SEG6 COM3	SEG5 COM3	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3	XXXX XXXX	uuuu uuuu
LCDDATA10	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3	XXXX XXXX	uuuu uuuu
LCDDATA11 ⁽²⁾	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3	XXXX XXXX	uuuu uuuu
LCDDATA12 ⁽³⁾	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0	XXXX XXXX	uuuu uuuu
LCDDATA13 ⁽³⁾	SEG39 COM0	SEG38 COM0	SEG37 COM0	SEG36 COM0	SEG35 COM0	SEG34 COM0	SE33 COM0	SEG32 COM0	XXXX XXXX	uuuu uuuu
LCDDATA14 ⁽³⁾	—	—	—	-	_	—	SEG41 COM0	SEG40 COM0	xx	uu
LCDDATA15 ⁽³⁾	SEG31 COM1	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1	XXXX XXXX	uuuu uuuu
LCDDATA16 ⁽³⁾	SEG39 COM1	SEG38 COM1	SEG37 COM1	SEG36 COM1	SEG35 COM1	SEG34 COM1	SEG33 COM1	SEG32 COM1	XXXX XXXX	uuuu uuuu
LCDDATA17 ⁽³⁾	_	_	_	_		_	SEG41 COM1	SEG40 COM1	xx	uu
LCDDATA18 ⁽³⁾	SEG31 COM2	SEG30 COM2	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2	XXXX XXXX	uuuu uuuu
LCDDATA19 ⁽³⁾	SEG39 COM2	SEG38 COM2	SEG37 COM2	SEG36 COM2	SEG35 COM2	SEG34 COM2	SEG33 COM2	SEG32 COM2	XXXX XXXX	uuuu uuuu
LCDDATA20 ⁽³⁾		_	_	—		_	SEG41 COM2	SEG40 COM2	xx	uu
LCDDATA21 ⁽³⁾	SEG31 COM3	SEG30 COM3	SEG29 COM3	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3	XXXX XXXX	uuuu uuuu
LCDDATA22 ⁽³⁾	SEG39 COM3	SEG38 COM3	SEG37 COM3	SEG36 COM3	SEG35 COM3	SEG34 COM3	SEG33 COM3	SEG32 COM3	XXXX XXXX	uuuu uuuu
LCDDATA23 ⁽³⁾	-	—	—	—	—	—	SEG41 COM3	SEG40 COM3	xx	uu
LCDPS	WFT	BIASMD	LCDA	WA	LP3	LP2	LP1	LP0	0000 0000	0000 0000
LCDSE0	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	0000 0000	uuuu uuuu
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	uuuu uuuu

x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the LCD module. These pins may be configured as port pins, depending on the oscillator mode selected. PIC16F914/917 and PIC16F946 only. PIC16F946 only. Legend:

Note 1:

2: 3:

NOTES:

TABLE 19-9: PIC16F913/914/916/917/946 A/D CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$									
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions		
AD130*	Tad	A/D Clock Period	1.6	_	9.0	μs	Tosc-based, VREF \geq 3.0V		
			3.0	—	9.0	μs	Tosc-based, VREF full range		
		A/D Internal RC					ADCS<1:0> = 11 (ADRC mode)		
		Oscillator Period	3.0	6.0	9.0	μs	At VDD = 2.5V		
			1.6	4.0	6.0	μs	At VDD = 5.0V		
AD131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	_	11	_	Tad	Set GO/DONE bit to new data in A/D Result register		
AD132*	TACQ	Acquisition Time		11.5	—	μs			
AD133*	TAMP	Amplifier Settling Time	_	_	5	μs			
AD134	Tgo	Q4 to A/D Clock Start	—	Tosc/2		-			
				Tosc/2 + Tcy			If the A/D clock source is selected as RC, a time of TcY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRESH and ADRESL registers may be read on the following TCY cycle.

2: See Section 12.3 "A/D Acquisition Requirements" for minimum conditions.







FIGURE 20-30: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

FIGURE 20-34: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE









FIGURE 20-38: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)





PIC16F917/916/914/913

NOTES: