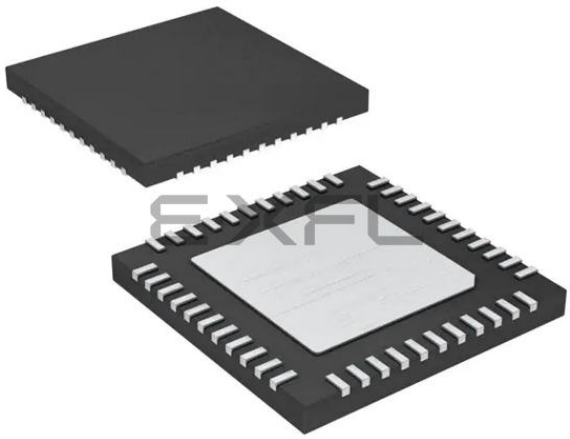

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Number of I/O	35
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f914t-i-ml

TABLE 1: PIC16F914/917 40-PIN SUMMARY

I/O	Pin	A/D	LCD	Comparators	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	2	AN0	SEG12	C1-	—	—	—	—	—	—	—
RA1	3	AN1	SEG7	C2-	—	—	—	—	—	—	—
RA2	4	AN2/VREF-	COM2	C2+	—	—	—	—	—	—	—
RA3	5	AN3/VREF+	SEG15	C1+	—	—	—	—	—	—	—
RA4	6		SEG4	C1OUT	T0CKI	—	—	—	—	—	—
RA5	7	AN4	SEG5	C2OUT	—	—	—	$\overline{SS}$	—	—	—
RA6	14	—	—	—	T1OSO	—	—	—	—	—	OSC2/CLKOUT
RA7	13	—	—	—	T1OSI	—	—	—	—	—	OSC1/CLKIN
RB0	33	—	SEG0	—	—	—	—	—	INT	Y	—
RB1	34	—	SEG1	—	—	—	—	—	—	Y	—
RB2	35	—	SEG2	—	—	—	—	—	—	Y	—
RB3	36	—	SEG3	—	—	—	—	—	—	Y	—
RB4	37	—	COM0	—	—	—	—	—	IOC	Y	—
RB5	38	—	COM1	—	—	—	—	—	IOC	Y	—
RB6	39	—	SEG14	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCK
RB7	40	—	SEG13	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	15	—	VLCD1	—	—	—	—	—	—	—	—
RC1	16	—	VLCD2	—	—	—	—	—	—	—	—
RC2	17	—	VLCD3	—	—	—	—	—	—	—	—
RC3	18	—	SEG6	—	—	—	—	—	—	—	—
RC4	23	—	SEG11	—	$\overline{T1G}$	—	—	SDO	—	—	—
RC5	24	—	SEG10	—	T1CKI	CCP1	—	—	—	—	—
RC6	25	—	SEG9	—	—	—	TX/CK	SCK/SCL	—	—	—
RC7	26	—	SEG8	—	—	—	RX/DT	SDI/SDA	—	—	—
RD0	19	—	COM3	—	—	—	—	—	—	—	—
RD1	20	—	—	—	—	—	—	—	—	—	—
RD2	21	—	—	—	—	CCP2	—	—	—	—	—
RD3	22	—	SEG16	—	—	—	—	—	—	—	—
RD4	27	—	SEG17	—	—	—	—	—	—	—	—
RD5	28	—	SEG18	—	—	—	—	—	—	—	—
RD6	29	—	SEG19	—	—	—	—	—	—	—	—
RD7	30	—	SEG20	—	—	—	—	—	—	—	—
RE0	8	AN5	SEG21	—	—	—	—	—	—	—	—
RE1	9	AN6	SEG22	—	—	—	—	—	—	—	—
RE2	10	AN7	SEG23	—	—	—	—	—	—	—	—
RE3	1	—	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
—	11	—	—	—	—	—	—	—	—	—	VDD
—	32	—	—	—	—	—	—	—	—	—	VDD
—	12	—	—	—	—	—	—	—	—	—	VSS
—	31	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pull-up enabled only with external $\overline{MCLR}$ configuration.

2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers (GPRs) and the Special Function Registers (SFRs). Bits RP0 and RP1 are bank select bits.

RP1	RP0		
0	0	→	Bank 0 is selected
0	1	→	Bank 1 is selected
1	0	→	Bank 2 is selected
1	1	→	Bank 3 is selected

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in another bank for code reduction and quicker access.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 256 x 8 bits in the PIC16F913/914, 352 x 8 bits in the PIC16F916/917 and 336 x 8 bits in the PIC16F946. Each register is accessed either directly or indirectly through the File Select Register (FSR) (see **Section 2.5 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Tables 2-1, 2-2, 2-3 and 2-4). These registers are static RAM.

The Special Function Registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

2.2.2.2 OPTION register

The OPTION register, shown in Register 2-2, is a readable and writable register, which contains various control bits to configure:

- Timer0/WDT prescaler
- External RB0/INT interrupt
- Timer0
- Weak pull-ups on PORTB

Note: To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting PSA bit of the OPTION register to '1'. See **Section 6.3 "Timer1 Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual bits in the WPUB register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

2.2.2.8 PCON Register

The Power Control (PCON) register contains flag bits (see Table 16-2) to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the software enable of the BOR.

The PCON register bits are shown in Register 2-8.

REGISTER 2-8: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	R/W-1	U-0	U-0	R/W-0	R/W-x
—	—	—	SBOREN	—	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **SBOREN:** Software BOR Enable bit(1)
- 1 = BOR enabled
- 0 = BOR disabled

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
- 1 = No Power-on Reset occurred
- 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
- 1 = No Brown-out Reset occurred
- 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

Note 1: Set BOREN<1:0> = 01 in the Configuration Word register for this bit to control the $\overline{BOR}$.

3.0 I/O PORTS

The PIC16F913/914/916/917/946 family of devices includes several 8-bit PORT registers along with their corresponding TRIS registers and one four bit port:

- PORTA and TRISA
- PORTB and TRISB
- PORTC and TRISC
- PORTD and TRISD(1)
- PORTE and TRISE
- PORTF and TRISF(2)
- PORTG and TRISG(2)

Note 1:	PIC16F914/917 and PIC16F946 only.
2:	PIC16F946 only

PORTA, PORTB, PORTC and RE3/$\overline{MCLR}$/VPP are implemented on all devices. PORTD and RE<2:0> (PORTE) are implemented only on the PIC16F914/917 and PIC16F946. RE<7:4> (PORTE), PORTF and PORTG are implemented only on the PIC16F946.

3.1 ANSEL Register

The ANSEL register (Register 3-1) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSEL bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSEL bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

REGISTER 3-1: ANSEL: ANALOG SELECT REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7(2)	ANS6(2)	ANS5(2)	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ANS<7:0>**: Analog Select bits
Analog select between analog or digital function on pins AN<7:0>, respectively.
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

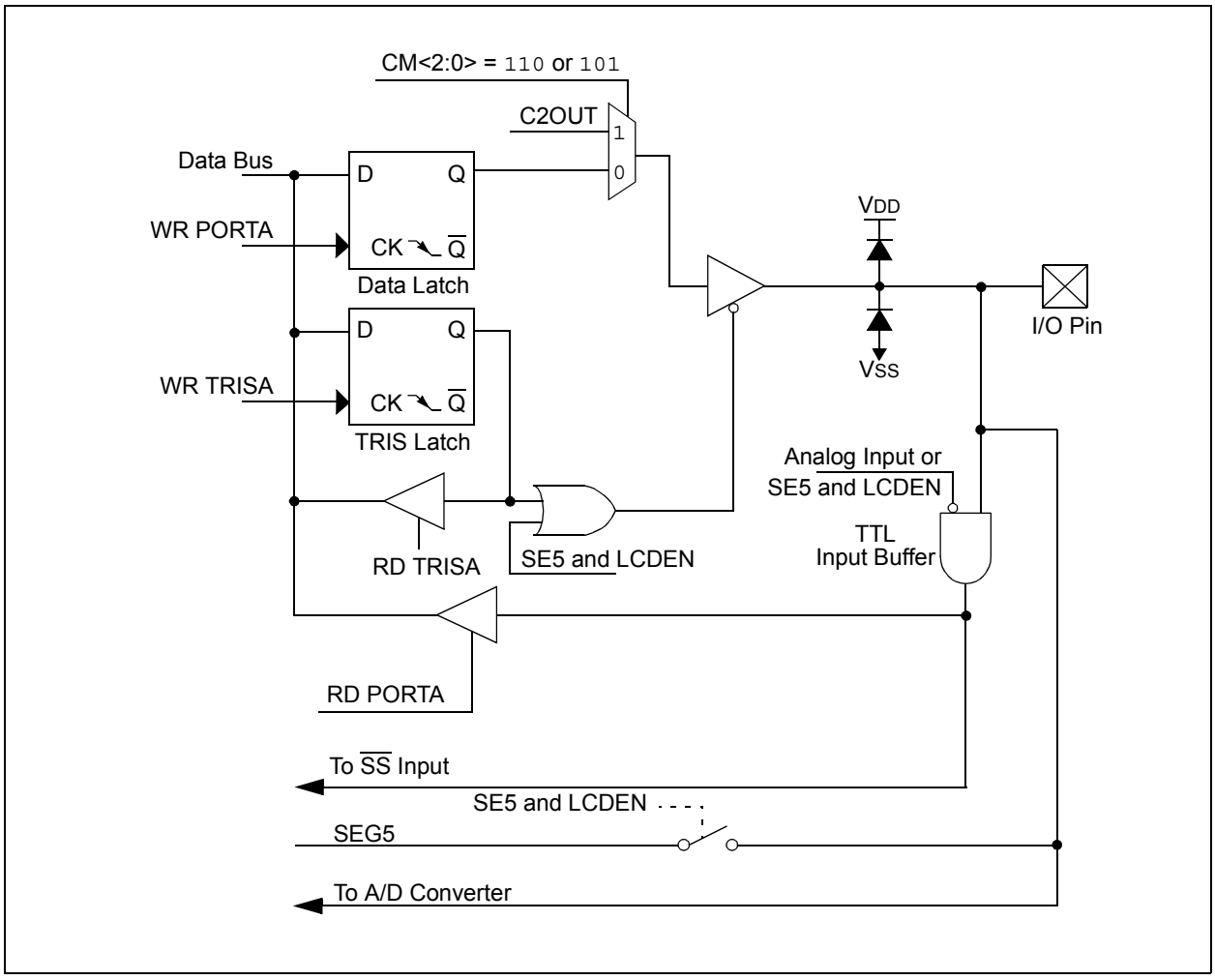
2: PIC16F914/PIC16F917/PIC16F946 only.

3.2.1.6 RA5/AN4/C2OUT/$\overline{SS}$/SEG5

Figure 3-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- a general purpose I/O
- a digital output from Comparator C2
- a slave select input
- an analog output for the LCD
- an analog input for the ADC

FIGURE 3-6: BLOCK DIAGRAM OF RA5



3.3 PORTB and TRISB Registers

PORTB is an 8-bit bidirectional I/O port. All PORTB pins can have a weak pull-up feature, and PORTB<7:4> implements an interrupt-on-input change function.

PORTB is also used for the Serial Flash programming interface and ICD interface.

EXAMPLE 3-2: INITIALIZING PORTB

```
BANKSEL PORTB       ;
CLRF    PORTB       ;Init PORTB
BANKSEL TRISB       ;
MOVLW   0FFh        ;Set RB<7:0> as inputs
MOVWF   TRISB       ;
```

3.4 Additional PORTB Pin Functions

RB<7:6> are used as data and clock signals, respectively, for both serial programming and the in-circuit debugger features on the device. Also, RB0 can be configured as an external interrupt input.

3.4.1 WEAK PULL-UPS

Each of the PORTB pins has an individually configurable internal weak pull-up. Control bits WPUB<7:0> enable or disable each pull-up. Refer to Register 3-7. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{RBPU}}$ bit of the OPTION register.

3.4.2 INTERRUPT-ON-CHANGE

Four of the PORTB pins are individually configurable as an interrupt-on-change pin. Control bits IOCB<7:4> enable or disable the interrupt function for each pin. Refer to Register 3-6. The interrupt-on-change feature is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTB. The 'mismatch' outputs of the last read are OR'd together to set the PORTB Change Interrupt flag bit (RBIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read or write of PORTB. This will end the mismatch condition.
b) Clear the flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading or writing PORTB will end the mismatch condition and allow flag bit RBIF to be cleared. The latch holding the last read value is not affected by a $\overline{\text{MCLR}}$ nor Brown-out Reset. After these Resets, the RBIF flag will continue to be set if a mismatch is present.

Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set. Furthermore, since a read or write on a port affects all bits of that port, care must be taken when using multiple pins in Interrupt-on-change mode. Changes on one pin may not be seen while servicing changes on another pin.

3.7.1 PIN DESCRIPTIONS AND DIAGRAMS

Each PORTE pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the Comparator or the ADC, refer to the appropriate section in this data sheet.

3.7.1.1 RE0/AN5/SEG21(1)

Figure 3-26 shows the diagram for this pin. The RE0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog output for the LCD

3.7.1.2 RE1/AN6/SEG22(1)

Figure 3-26 shows the diagram for this pin. The RE1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog output for the LCD

3.7.1.3 RE2/AN7/SEG23(1)

Figure 3-26 shows the diagram for this pin. The RE2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog output for the LCD

3.7.1.4 RE3/$\overline{\text{MCLR}}$/VPP

Figure 3-27 shows the diagram for this pin. The RE3 pin is configurable to function as one of the following:

- a digital input only
- as Master Clear Reset with weak pull-up
- a programming voltage reference input

3.7.1.5 RE4/SEG24(2)

Figure 3-28 shows the diagram for this pin. The RE4/SEG24 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog output for the LCD

3.7.1.6 RE5/SEG25(2)

Figure 3-28 shows the diagram for this pin. The RE5/SEG25 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog output for the LCD

3.7.1.7 RE6/SEG26(2)

Figure 3-28 shows the diagram for this pin. The RE6/SEG26 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog output for the LCD

3.7.1.8 RE7/SEG27(2)

Figure 3-28 shows the diagram for this pin. The RE7/SEG27 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog output for the LCD

Note 1: Pin is available on the PIC16F914/917 and PIC16F946 only.

2: Pin is available on the PIC16F946 only.

REGISTER 7-1: T2CON: TIMER 2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscaler Select bits

0000 = 1:1 Postscaler
0001 = 1:2 Postscaler
0010 = 1:3 Postscaler
0011 = 1:4 Postscaler
0100 = 1:5 Postscaler
0101 = 1:6 Postscaler
0110 = 1:7 Postscaler
0111 = 1:8 Postscaler
1000 = 1:9 Postscaler
1001 = 1:10 Postscaler
1010 = 1:11 Postscaler
1011 = 1:12 Postscaler
1100 = 1:13 Postscaler
1101 = 1:14 Postscaler
1110 = 1:15 Postscaler
1111 = 1:16 Postscaler

bit 2 **TMR2ON:** Timer2 On bit

1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PR2	Timer2 Module Period Register								1111 1111	1111 1111
TMR2	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for Timer2 module.

9.3 AUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The AUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

9.3.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the AUSART for Synchronous Master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the AUSART.

The LCD SEG8 and SEG9 functions must be disabled by clearing the SE8 and SE9 bits of the LCDSE1 register, if the RX/DT and TX/CK pins are shared with the LCD peripheral.

9.3.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the AUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

9.3.1.2 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the AUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

9.3.1.3 Synchronous Master Transmission Set-up:

1. Initialize the SPBRG register and the BRGH bit to achieve the desired baud rate (see **Section 9.2 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. Disable Receive mode by clearing bits SREN and CREN.
4. Enable Transmit mode by setting the TXEN bit.
5. If 9-bit transmission is desired, set the TX9 bit.
6. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
8. Start transmission by loading data to the TXREG register.

FIGURE 10-5: LCD SEGMENT MAPPING WORKSHEET (SHEET 2 OF 2)

LCD Function	COM0		COM1		COM2		COM3		Pin No.	PORT	Alternate Functions
	LCDDATAx Address	LCD Segment	LCDDATAx Address	LCD Segment	LCDDATAx Address	LCD Segment	LCDDATAx Address	LCD Segment	64-pin		
SEG24	LCDDATA12, 0		LCDDATA15, 0		LCDDATA18, 0		LCDDATA21, 0		37	RE4	
SEG25	LCDDATA12, 1		LCDDATA15, 1		LCDDATA18, 1		LCDDATA21, 1		42	RE5	
SEG26	LCDDATA12, 2		LCDDATA15, 2		LCDDATA18, 2		LCDDATA21, 2		43	RE6	
SEG27	LCDDATA12, 3		LCDDATA15, 3		LCDDATA18, 3		LCDDATA21, 3		44	RE7	
SEG28	LCDDATA12, 4		LCDDATA15, 4		LCDDATA18, 4		LCDDATA21, 4		45	RF4	
SEG29	LCDDATA12, 5		LCDDATA15, 5		LCDDATA18, 5		LCDDATA21, 5		46	RF5	
SEG30	LCDDATA12, 6		LCDDATA15, 6		LCDDATA18, 6		LCDDATA21, 6		47	RF6	
SEG31	LCDDATA12, 7		LCDDATA15, 7		LCDDATA18, 7		LCDDATA21, 7		48	RF7	
SEG32	LCDDATA13, 0		LCDDATA16, 0		LCDDATA19, 0		LCDDATA22, 0		11	RF0	
SEG33	LCDDATA13, 1		LCDDATA16, 1		LCDDATA19, 1		LCDDATA22, 1		12	RF1	
SEG34	LCDDATA13, 2		LCDDATA16, 2		LCDDATA19, 2		LCDDATA22, 2		13	RF2	
SEG35	LCDDATA13, 3		LCDDATA16, 3		LCDDATA19, 3		LCDDATA22, 3		14	RF3	
SEG36	LCDDATA13, 4		LCDDATA16, 4		LCDDATA19, 4		LCDDATA22, 4		3	RG0	
SEG37	LCDDATA13, 5		LCDDATA16, 5		LCDDATA19, 5		LCDDATA22, 5		4	RG1	
SEG38	LCDDATA13, 6		LCDDATA16, 6		LCDDATA19, 6		LCDDATA22, 6		5	RG2	
SEG39	LCDDATA13, 7		LCDDATA16, 7		LCDDATA19, 7		LCDDATA22, 7		6	RG3	
SEG40	LCDDATA14, 0		LCDDATA17, 0		LCDDATA20, 0		LCDDATA23, 0		7	RG4	
SEG41	LCDDATA14, 1		LCDDATA17, 1		LCDDATA20, 1		LCDDATA23, 1		8	RG5	

PIC16F946 only.

13.1.4 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must write two bytes of the address to the EEADRL and EEADRH registers, set the EEPGD control bit, and then set control bit RD of the EECON1 register. Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "BSF EECON1,RD" instruction to be ignored. The data is available in the very next cycle, in the EEDATL and EEDATH registers; therefore, it can be read as two bytes in the following instructions. EEDATL and EEDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

Note 1: The two instructions following a program memory read are required to be NOP's. This prevents the user from executing a two-cycle instruction on the next instruction after the RD bit is set.

2: If the WR bit is set when EEPGD = 1, the WR bit will be immediately reset to '0' and no operation will take place.

EXAMPLE 13-3: FLASH PROGRAM READ

```
        BANKSEL  EEADRL          ;
        MOVLW    MS_PROG_EE_ADDR;
        MOVWF    EEADRH          ;MS Byte of Program Address to read
        MOVLW    LS_PROG_EE_ADDR;
        MOVWF    EEADRL          ;LS Byte of Program Address to read
        BANKSEL  EECON1          ;
        BSF      EECON1, EEPGD   ;Point to PROGRAM memory
        BSF      EECON1, RD      ;EE Read
;
        NOP
        NOP                      ;Any instructions here are ignored as program
                                 ;memory is read in second cycle after BSF
;
        BANKSEL  EEDATL          ;
        MOVF     EEDATL, W       ;W = LS Byte of EEPROM Data program
        MOVWF    DATAL           ;
        MOVF     EEDATH, W       ;W = MS Byte of EEPROM Data program
        MOVWF    DATAH           ;
```

Required Sequence

15.3.3 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 15-4.

EQUATION 15-4: PWM RESOLUTION

$$Resolution = \frac{log[4(PR2 + 1)]}{log(2)} \ bits$$

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 15-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 15-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

15.3.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

15.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 4.0 "Oscillator Module (With Fail-Safe Clock Monitor)"** for additional details.

15.3.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

15.3.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCPx) output drivers by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPRxL register and CCPx bits of the CCPxCON register.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register.
   - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
   - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
   - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
   - Enable the CCPx pin output driver by clearing the associated TRIS bit.

TABLE 15-5: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCPxCON	—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0	--00 0000	--00 0000
CCPRxL	Capture/Compare/PWM Register X Low Byte								xxxx xxxx	uuuu uuuu
CCPRxH	Capture/Compare/PWM Register X High Byte								xxxx xxxx	uuuu uuuu
CMCON1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
LCDCON	LCDEN	$\overline{\text{SLPEN}}$	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	0000 0000
PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIE2	OSFIE	C2IE	C1IE	LCDIE	—	LVDIE	—	CCP2IE	0000 -0-0	0000 -0-0
PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	OSFIF	C2IF	C1IF	LCDIF	—	LVDIF	—	CCP2IF	0000 -0-0	0000 -0-0
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR2	Timer2 Module Register								0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TRISD(1)	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	1111 1111

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.

Note 1: PIC16F914/917 and PIC16F946 only.

16.2.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired, then OST is activated after the PWRT time-out has expired. The total time-out will vary based on oscillator configuration and $\overline{PWRTE}$ bit status. For example, in EC mode with $\overline{PWRTE}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 16-4, Figure 16-5 and Figure 16-6 depict time-out sequences. The device can execute code from the INTOSC while OST is active, by enabling Two-Speed Start-up or Fail-Safe Monitor (see **Section 4.7.2 "Two-Speed Start-up Sequence"** and **Section 4.8 "Fail-Safe Clock Monitor"**).

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{MCLR}$ high will begin execution immediately (see Figure 16-5). This is useful for testing purposes or to synchronize more than one PIC16F91X/946 device operating in parallel.

Table 16-5 shows the Reset conditions for some special registers, while Table 16-5 shows the Reset conditions for all the registers.

16.2.7 POWER CONTROL (PCON) REGISTER

The Power Control (PCON) register (address 8Eh) has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is $\overline{BOR}$ (Brown-out Reset). $\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{BOR}$ = 0, indicating that a Brown-out has occurred. The $\overline{BOR}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is $\overline{POR}$ (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{POR}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., V_{DD} may have gone too low).

For more information, see **Section 16.2.4 "Brown-Out Reset (BOR)"**.

TABLE 16-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1	
XT, HS, LP(1)	TPWRT + 1024 • TOSC	1024 • TOSC	TPWRT + 1024 • TOSC	1024 • TOSC	1024 • TOSC
RC, EC, INTOSC	TPWRT	—	TPWRT	—	—

Note 1: LP mode with T1OSC disabled.

TABLE 16-2: PCON BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	Condition
0	u	1	1	Power-on Reset
1	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	$\overline{MCLR}$ Reset during normal operation
u	u	1	0	$\overline{MCLR}$ Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 16-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets(1)
STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
PCON	—	—	—	SBOREN	—	—	$\overline{POR}$	$\overline{BOR}$	--01 --qq	--0u --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

RLF **Rotate Left f through Carry**

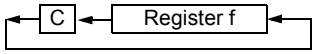
Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction

```
REG1    =   1110 0110
C       =   0
```

After Instruction

```
REG1    =   1110 0110
W       =   1100 1100
C       =   1
```

RRF **Rotate Right f through Carry**

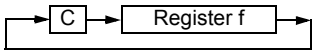
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP **Enter Sleep mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.

SUBLW **Subtract W from literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

19.6 Thermal Considerations

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C					
Param No.	**Symbol**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θJA	Thermal Resistance Junction to Ambient	60.0	°C/W	28-pin PDIP package
			80.0	°C/W	28-pin SOIC package
			90.0	°C/W	28-pin SSOP package
			27.5	°C/W	28-pin QFN 6x6 mm package
			47.2	°C/W	40-pin PDIP package
			46.0	°C/W	44-pin TQFP package
			24.4	°C/W	44-pin QFN 8x8 mm package
			77.0	°C/W	64-pin TQFP package
TH02	θJC	Thermal Resistance Junction to Case	31.4	°C/W	28-pin PDIP package
			24.0	°C/W	28-pin SOIC package
			24.0	°C/W	28-pin SSOP package
			20.0	°C/W	28-pin QFN 6x6 mm package
			24.7	°C/W	40-pin PDIP package
			14.5	°C/W	44-pin TQFP package
			20.0	°C/W	44-pin QFN 8x8 mm package
			24.4	°C/W	64-pin TQFP package
TH03	TJ	Junction Temperature	150	°C	For derated power calculations
TH04	PD	Power Dissipation	—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation	—	W	PINTERNAL = IDD x VDD **(NOTE 1)**
TH06	PI/O	I/O Power Dissipation	—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power	—	W	PDER = (TJ - TA)/θJA **(NOTE 2, 3)**

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

3: Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power (PDER).

FIGURE 20-4: MAXIMUM IDD vs. FOSC OVER VDD (HS MODE)

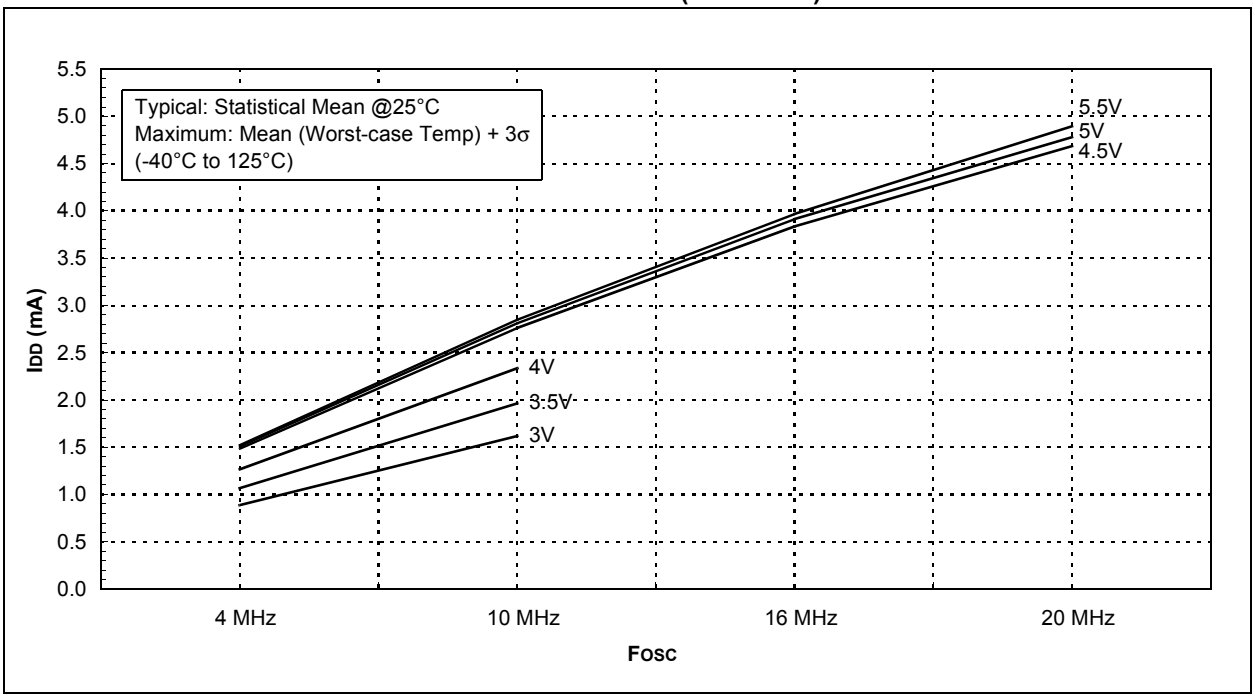


FIGURE 20-5: TYPICAL IDD vs. VDD OVER FOSC (XT MODE)

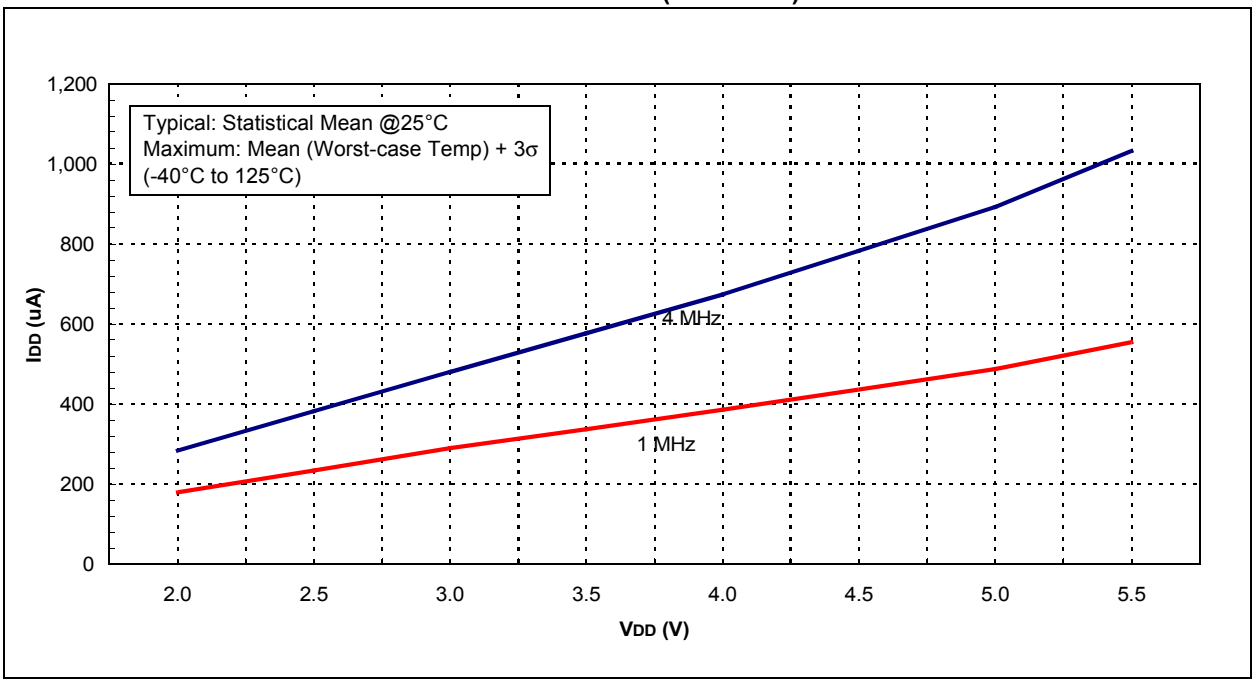


FIGURE 20-8: MAXIMUM IDD vs. VDD (EXTRC MODE)

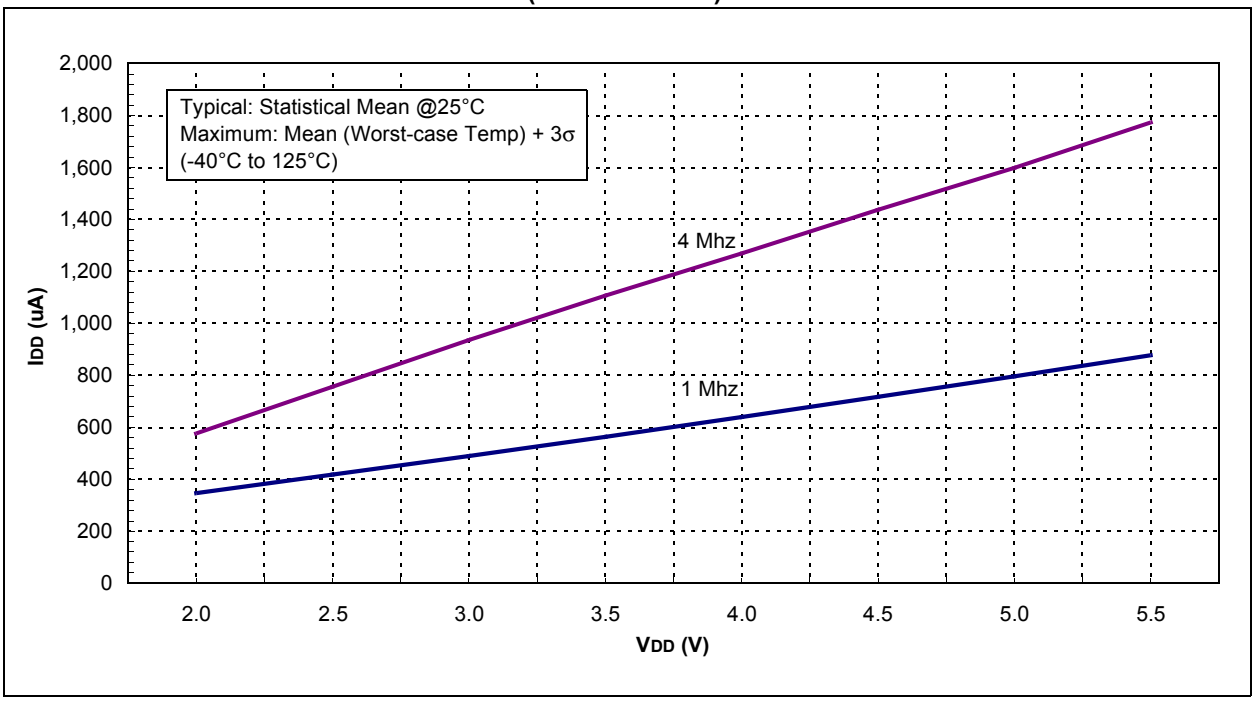


FIGURE 20-9: IDD vs. VDD OVER FOSC (LFINTOSC MODE, 31 kHz)

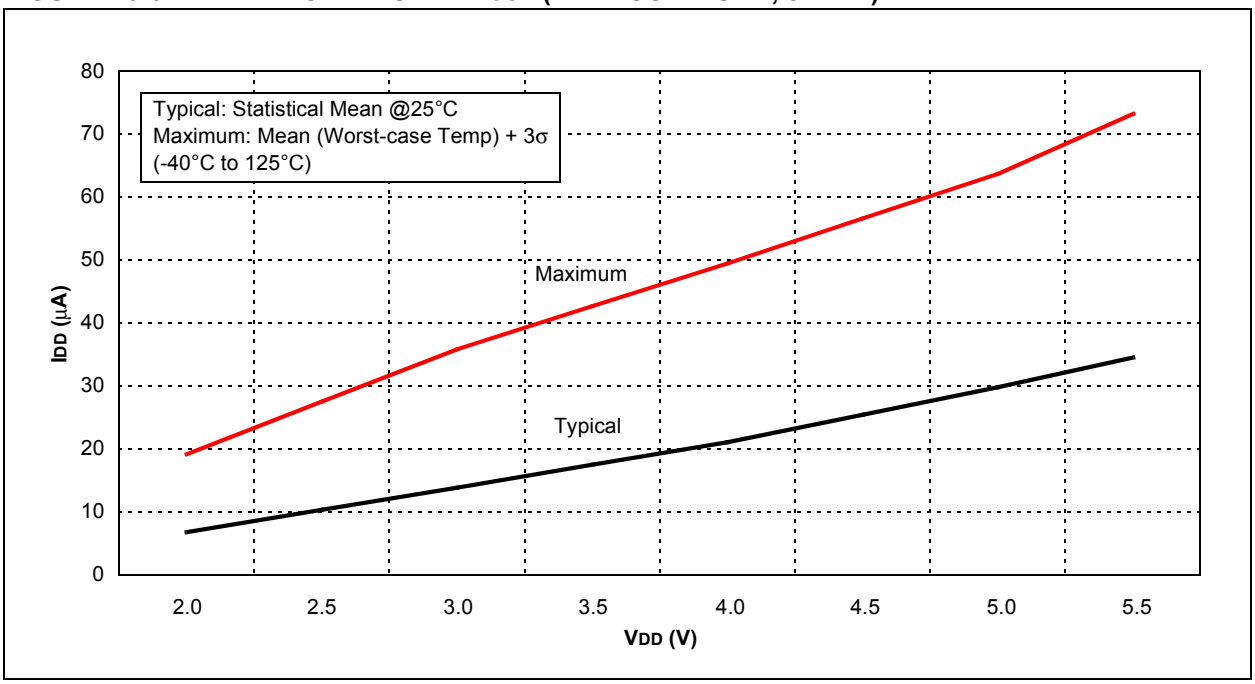


FIGURE 20-40: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (125°C)

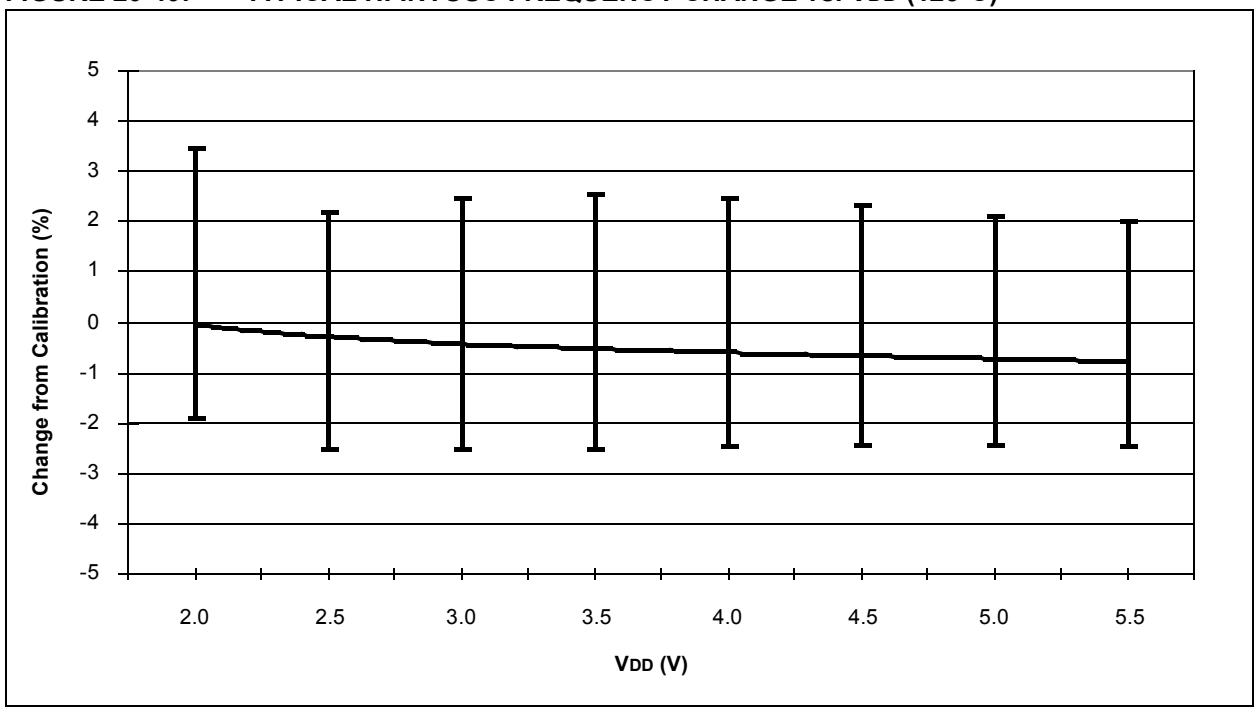


FIGURE 20-41: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (-40°C)