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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f916-e-sp



MICROCHIP

PIC16F913/914/916/917/946

28/40/44/64-Pin Flash-Based, 8-Bit CMOS Microcontrollers with LCD Driver and nanoWatt Technology

High-Performance RISC CPU:

- Only 35 instructions to learn:
 - All single-cycle instructions except branches
- Operating speed:
 - DC – 20 MHz oscillator/clock input
 - DC – 200 ns instruction cycle
- Program Memory Read (PMR) capability
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
 - Factory calibrated to $\pm 1\%$, typical
 - Software selectable frequency range of 8 MHz to 125 kHz
 - Software tunable
 - Two-Speed Start-up mode
 - External Oscillator fail detect for critical applications
 - Clock mode switching during operation for power savings
- Software selectable 31 kHz internal oscillator
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended temperature range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection
- High-Endurance Flash/EEPROM cell:
 - 100,000 write Flash endurance
 - 1,000,000 write EEPROM endurance
 - Flash/Data EEPROM retention: > 40 years

Low-Power Features:

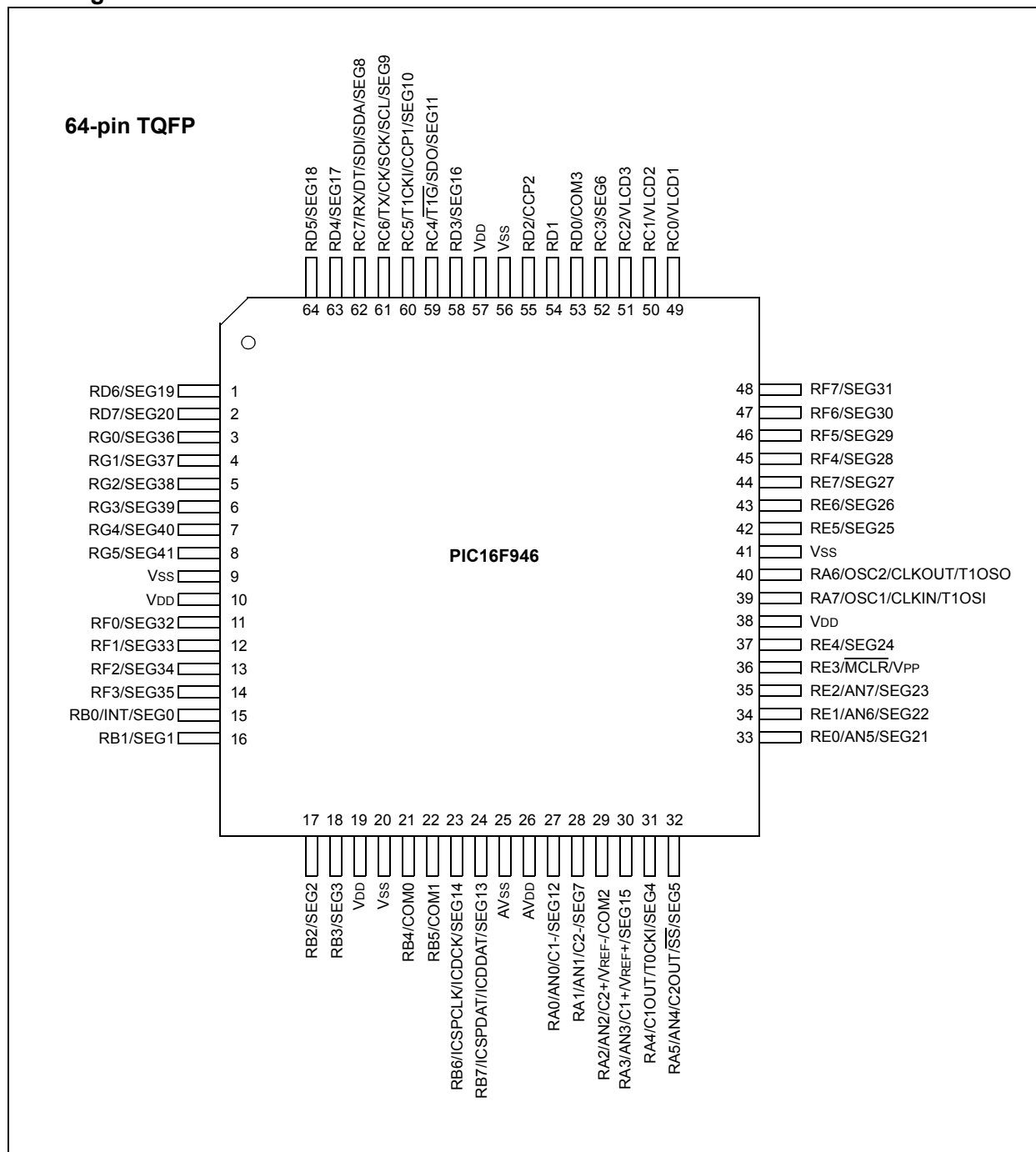
- Standby Current:
 - <100 nA @ 2.0V, typical
- Operating Current:
 - 11 μ A @ 32 kHz, 2.0V, typical
 - 220 μ A @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
 - 1 μ A @ 2.0V, typical

Peripheral Features:

- Liquid Crystal Display module:
 - Up to 60/96/168 pixel drive capability on 28/40/64-pin devices, respectively
 - Four commons
- Up to 24/35/53 I/O pins and 1 input-only pin:
 - High-current source/sink for direct LED drive
 - Interrupt-on-change pin
 - Individually programmable weak pull-ups
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Analog comparator module with:
 - Two analog comparators
 - Programmable on-chip voltage reference (CVREF) module (% of VDD)
 - Comparator inputs and outputs externally accessible
- A/D Converter:
 - 10-bit resolution and up to 8 channels
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Timer1 Gate (count enable)
 - Option to use OSC1 and OSC2 as Timer1 oscillator if INTOSCIO or LP mode is selected
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART)
- Up to 2 Capture, Compare, PWM modules:
 - 16-bit Capture, max. resolution 12.5 ns
 - 16-bit Compare, max. resolution 200 ns
 - 10-bit PWM, max. frequency 20 kHz
- Synchronous Serial Port (SSP) with I²C™

PIC16F913/914/916/917/946

Pin Diagram – PIC16F946



PIC16F913/914/916/917/946

TABLE 2-2: PIC16F91X/946 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	41,226
81h	OPTION_REG	RBP \overline{U}	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	33,227
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	40,226
83h	STATUS	IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	32,226
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	41,226
85h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	44,227
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	54,227
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	62,227
88h	TRISD ⁽³⁾	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	71,227
89h	TRISE	TRISE7 ⁽²⁾	TRISE6 ⁽²⁾	TRISE5 ⁽²⁾	TRISE4 ⁽²⁾	TRISE3 ⁽⁵⁾	TRISE2 ⁽³⁾	TRISE1 ⁽³⁾	TRISE0 ⁽³⁾	1111 1111	76,227
8Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	40,226
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	34,226
8Ch	PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	35,227
8Dh	PIE2	OSFIE	C2IE	C1IE	LCDIE	—	LVDIE	—	CCP2IE ⁽³⁾	0000 -0-0	36,227
8Eh	PCON	—	—	—	SBOREN	—	—	\overline{POR}	\overline{BOR}	---1 --qg	39,227
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS ⁽⁴⁾	HTS	LTS	SCS	-110 q000	88,227
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	92,227
91h	ANSEL	ANS7 ⁽³⁾	ANS6 ⁽³⁾	ANS5 ⁽³⁾	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	43,227
92h	PR2	Timer2 Period Register								1111 1111	107,227
93h	SSPADD	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	202,227
94h	SSPSTAT	SMP	CKE	D/ \overline{A}	P	S	R/ \overline{W}	UA	BF	0000 0000	194,227
95h	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	1111 1111	55,227
96h	IOCB	IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—	0000 ----	54,227
97h	CMCON1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10	117,227
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	130,227
99h	SPBRG	SPBRG7	SPBRG6	SPBRG5	SPBRG4	SPBRG3	SPBRG2	SPBRG1	SPBRG0	0000 0000	132,227
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	116,227
9Dh	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	118,227
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	182,227
9Fh	ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	181,227

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

- Note**
- 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.
 - 2: PIC16F946 only, forced '0' on PIC16F91X.
 - 3: PIC16F914/917 and PIC16F946 only, forced '0' on PIC16F913/916.
 - 4: The value of the OSTS bit is dependent on the value of the Configuration Word (CONFIG) of the device. See **Section 4.2 "Oscillator Control"**.
 - 5: Bit is read-only; TRISE3 = 1 always.

PIC16F913/914/916/917/946

REGISTER 5-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
<u>RBP</u> U	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **RBPU**: PORTB Pull-up Enable bit
 1 = PORTB pull-ups are disabled
 0 = PORTB pull-ups are enabled by individual PORT latch values
- bit 6 **INTEDG**: Interrupt Edge Select bit
 1 = Interrupt on rising edge of INT pin
 0 = Interrupt on falling edge of INT pin
- bit 5 **T0CS**: TMR0 Clock Source Select bit
 1 = Transition on T0CKI pin
 0 = Internal instruction cycle clock (Fosc/4)
- bit 4 **T0SE**: TMR0 Source Edge Select bit
 1 = Increment on high-to-low transition on T0CKI pin
 0 = Increment on low-to-high transition on T0CKI pin
- bit 3 **PSA**: Prescaler Assignment bit
 1 = Prescaler is assigned to the WDT
 0 = Prescaler is assigned to the Timer0 module
- bit 2-0 **PS<2:0>**: Prescaler Rate Select bits

BIT VALUE	TMR0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: A dedicated 16-bit WDT postscaler is available. See **Section 16.4 “Watchdog Timer (WDT)”** for more information.

TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
OPTION_REG	<u>RBP</u> U	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

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REGISTER 9-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN ⁽¹⁾	SYNC	—	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)
- bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission
- bit 5 **TXEN:** Transmit Enable bit⁽¹⁾
1 = Transmit enabled
0 = Transmit disabled
- bit 4 **SYNC:** AUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode
- bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full
- bit 0 **TX9D:** Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

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FIGURE 9-6: SYNCHRONOUS TRANSMISSION

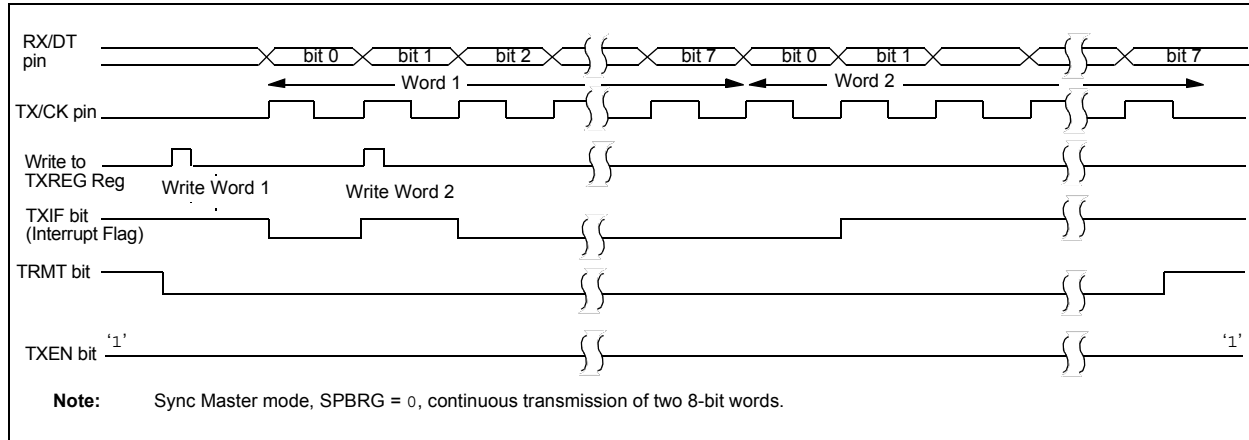


FIGURE 9-7: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)

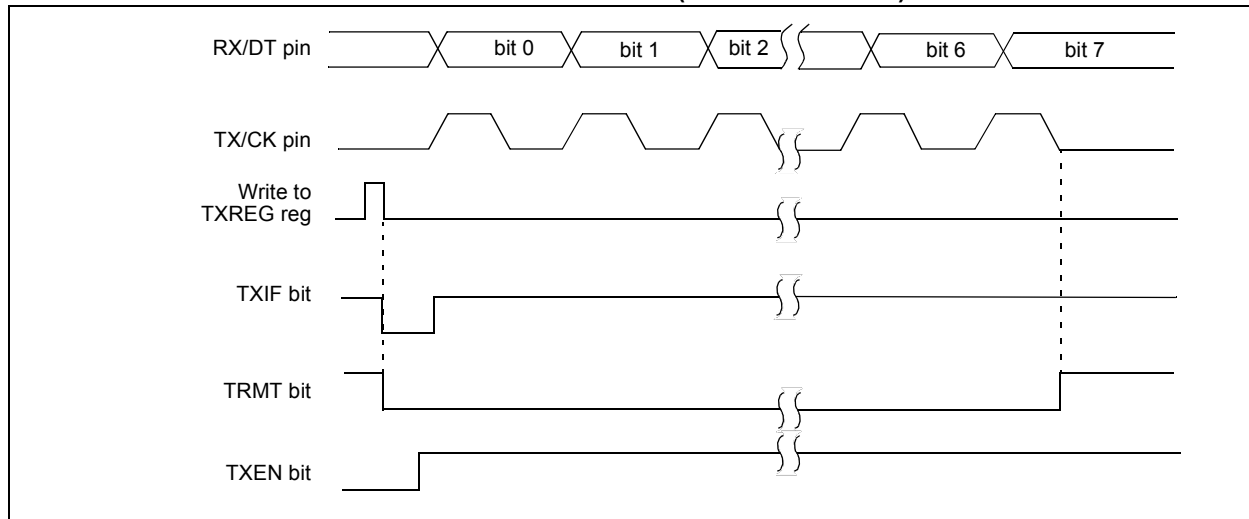


TABLE 9-6: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
LCDCON	LCDEN	SLPEN	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	0000 0000
PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Master Transmission.

12.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

12.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. See the corresponding Port section for more information.

Note: Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.
--

12.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 12.2 “ADC Operation”** for more information.

12.1.3 ADC VOLTAGE REFERENCE

The VCFG bits of the ADCON0 register provide independent control of the positive and negative voltage references. The positive voltage reference can be either VDD or an external voltage source. Likewise, the negative voltage reference can be either VSS or an external voltage source.

12.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods as shown in Figure 12-3.

For correct conversion, the appropriate TAD specification must be met. See A/D conversion requirements in **Section 19.0 “Electrical Specifications”** for more information. Table 12-1 gives examples of appropriate ADC clock selections.

Note: Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.
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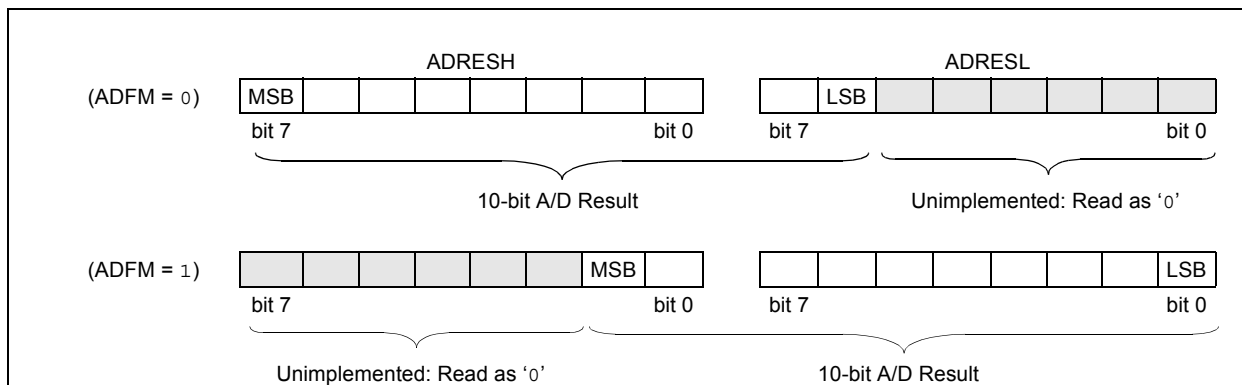
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12.1.6 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format.

Figure 12-4 shows the two output formats.

FIGURE 12-3: 10-BIT A/D CONVERSION RESULT FORMAT



12.2 ADC Operation

12.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/DONE bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note: The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to **Section 12.2.6 "A/D Conversion Procedure"**.

12.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONE bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

12.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete Analog-to-Digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

12.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

12.2.5 SPECIAL EVENT TRIGGER

The CCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/DONE bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See **Section 15.0 "Capture/Compare/PWM (CCP) Module"** for more information.

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NOTES:

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REGISTER 13-5: EECON1: EEPROM CONTROL REGISTER

R/W-x	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	—	—	—	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:

S = Bit can only be set

R = Readable bit

-n = Value at POR

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **EEPGD:** Program/Data EEPROM Select bit
 1 = Accesses program memory
 0 = Accesses data memory
- bit 6-4 **Unimplemented:** Read as '0'
- bit 3 **WRERR:** EEPROM Error Flag bit
 1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ Reset, any WDT Reset during normal operation or BOR Reset)
 0 = The write operation completed
- bit 2 **WREN:** EEPROM Write Enable bit
 1 = Allows write cycles
 0 = Inhibits write to the data EEPROM
- bit 1 **WR:** Write Control bit
 EEPGD = 1:
 This bit is ignored
 EEPGD = 0:
 1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
 0 = Write cycle to the data EEPROM is complete
- bit 0 **RD:** Read Control bit
 1 = Initiates a memory read (the RD is cleared in hardware and can only be set, not cleared, in software.)
 0 = Does not initiate a memory read

15.3.3 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 15-4.

EQUATION 15-4: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)} \text{ bits}$$

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 15-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 15-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

PIC16F913/914/916/917/946

15.3.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

15.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 4.0 “Oscillator Module (With Fail-Safe Clock Monitor)”** for additional details.

15.3.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

15.3.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCPx) output drivers by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPRxL register and CCPx bits of the CCPxCON register.
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register.
 - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
 - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
 - Enable the CCPx pin output driver by clearing the associated TRIS bit.

TABLE 15-5: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCPxCON	—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0	--00 0000	--00 0000
CCPRxL	Capture/Compare/PWM Register X Low Byte								xxxx xxxx	uuuu uuuu
CCPRxH	Capture/Compare/PWM Register X High Byte								xxxx xxxx	uuuu uuuu
CMCON1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
LCDCON	LCDEN	SLPEN	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	0000 0000
PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIE2	OSFIE	C2IE	C1IE	LCDIE	—	LVDIE	—	CCP2IE	0000 -0-0	0000 -0-0
PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	OSFIF	C2IF	C1IF	LCDIF	—	LVDIF	—	CCP2IF	0000 -0-0	0000 -0-0
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR2	Timer2 Module Register								0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TRISD ⁽¹⁾	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	1111 1111

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.

Note 1: PIC16F914/917 and PIC16F946 only.

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16.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 16-1. These bits are mapped in program memory location 2007h.

Note: Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "PIC16F91X/946 Memory Programming Specification" (DS41244) for more information.

REGISTER 16-1: CONFIG1: CONFIGURATION WORD REGISTER 1

—	—	—	DEBUG	FCMEN	IESO	BOREN1	BOREN0
bit 15							bit 8

CPD	CP	MCLRE	PWRT	WDTE	FOSC2	FOSC1	FOSC0
bit 7							bit 0

bit 15-13	Unimplemented: Read as '1'
bit 12	DEBUG: In-Circuit Debugger Mode bit 1 = In-Circuit Debugger disabled, RB6/ICSPCLK and RB7/ICSPDAT are general purpose I/O pins 0 = In-Circuit Debugger enabled, RB6/ICSPCLK and RB7/ICSPDAT are dedicated to the debugger
bit 11	FCMEN: Fail-Safe Clock Monitor Enabled bit 1 = Fail-Safe Clock Monitor is enabled 0 = Fail-Safe Clock Monitor is disabled
bit 10	IESO: Internal External Switchover bit 1 = Internal/External Switchover mode is enabled 0 = Internal/External Switchover mode is disabled
bit 9-8	BOREN<1:0>: Brown-out Reset Selection bits ⁽¹⁾ 11 = BOR enabled 10 = BOR enabled during operation and disabled in Sleep 01 = BOR controlled by SBOR bit of the PCON register 00 = BOR disabled
bit 7	CPD: Data Code Protection bit ⁽²⁾ 1 = Data memory code protection is disabled 0 = Data memory code protection is enabled
bit 6	CP: Code Protection bit ⁽³⁾ 1 = Program memory code protection is disabled 0 = Program memory code protection is enabled
bit 5	MCLRE: RE3/MCLR pin function select bit ⁽⁴⁾ 1 = RE3/MCLR pin function is MCLR 0 = RE3/MCLR pin function is digital input, MCLR internally tied to VDD
bit 4	PWRT: Power-up Timer Enable bit 1 = PWRT disabled 0 = PWRT enabled
bit 3	WDTE: Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled and can be enabled by SWDTEN bit of the WDTCON register
bit 2-0	FOSC<2:0>: Oscillator Selection bits 111 = RC oscillator: CLKOUT function on RA6/OSC2/CLKOUT/T1OSO pin, RC on RA7/OSC1/CLKIN/T1OSI 110 = RCIO oscillator: I/O function on RA6/OSC2/CLKOUT/T1OSO pin, RC on RA7/OSC1/CLKIN/T1OSI 101 = INTOSC oscillator: CLKOUT function on RA6/OSC2/CLKOUT/T1OSO pin, I/O function on RA7/OSC1/CLKIN/T1OSI 100 = INTOSCIO oscillator: I/O function on RA6/OSC2/CLKOUT/T1OSO pin, I/O function on RA7/OSC1/CLKIN/T1OSI 011 = EC: I/O function on RA6/OSC2/CLKOUT/T1OSO pin, CLKIN on RA7/OSC1/CLKIN/T1OSI 010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKOUT/T1OSO and RA7/OSC1/CLKIN/T1OSI 001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT/T1OSO and RA7/OSC1/CLKIN/T1OSI 000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKOUT/T1OSO and RA7/OSC1/CLKIN/T1OSI

- Note**
- 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
 - 2: The entire data EEPROM will be erased when the code protection is turned off.
 - 3: The entire program memory will be erased when the code protection is turned off.
 - 4: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

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16.2.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired, then OST is activated after the PWRT time-out has expired. The total time-out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 16-4, Figure 16-5 and Figure 16-6 depict time-out sequences. The device can execute code from the INTOSC while OST is active, by enabling Two-Speed Start-up or Fail-Safe Monitor (see **Section 4.7.2 “Two-Speed Start-up Sequence”** and **Section 4.8 “Fail-Safe Clock Monitor”**).

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 16-5). This is useful for testing purposes or to synchronize more than one PIC16F91X/946 device operating in parallel.

Table 16-5 shows the Reset conditions for some special registers, while Table 16-5 shows the Reset conditions for all the registers.

16.2.7 POWER CONTROL (PCON) REGISTER

The Power Control (PCON) register (address 8Eh) has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out Reset). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}} = 0$, indicating that a Brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a “don’t care” and is not necessarily predictable if the brown-out circuit is disabled ($\text{BOREN}<1:0> = 00$ in the Configuration Word register).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is a ‘0’ on Power-on Reset and unaffected otherwise. The user must write a ‘1’ to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is ‘0’, it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 16.2.4 “Brown-Out Reset (BOR)”**.

TABLE 16-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	
XT, HS, LP ⁽¹⁾	$\text{TPWRT} + 1024 \cdot \text{TOSC}$	$1024 \cdot \text{TOSC}$	$\text{TPWRT} + 1024 \cdot \text{TOSC}$	$1024 \cdot \text{TOSC}$	$1024 \cdot \text{TOSC}$
RC, EC, INTOSC	TPWRT	—	TPWRT	—	—

Note 1: LP mode with T1OSC disabled.

TABLE 16-2: PCON BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Condition
0	u	1	1	Power-on Reset
1	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
u	u	1	0	$\overline{\text{MCLR}}$ Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 16-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets ⁽¹⁾
STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
PCON	—	—	—	SBOREN	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	--01 --qq	--0u --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as ‘0’, q = value depends on condition. Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

18.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

18.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC® and MCU devices. It debugs and programs PIC® and dsPIC® Flash microcontrollers with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high speed, noise tolerant, low-voltage differential signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

18.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU STATUS and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

18.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

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19.3 DC Characteristics: PIC16F913/914/916/917/946-I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial					
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
D020	Power-down Base Current(IPD) ⁽²⁾	—	0.05	1.2	μA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	1.5	μA	3.0	
		—	0.35	1.8	μA	5.0	
		—	150	500	nA	3.0	$-40^{\circ}\text{C} \leq T_A \leq +25^{\circ}\text{C}$
D021		—	1.0	2.2	μA	2.0	WDT Current ⁽¹⁾
		—	2.0	4.0	μA	3.0	
		—	3.0	7.0	μA	5.0	
D022A		—	42	60	μA	3.0	BOR Current ⁽¹⁾
		—	85	122	μA	5.0	
D022B		—	22	28	μA	2.0	PLVD Current
		—	25	35	μA	3.0	
		—	33	45	μA	5.0	
D023		—	32	45	μA	2.0	Comparator Current ⁽¹⁾ , both comparators enabled
		—	60	78	μA	3.0	
		—	120	160	μA	5.0	
D024		—	30	36	μA	2.0	CVREF Current ⁽¹⁾ (high range)
		—	45	55	μA	3.0	
		—	75	95	μA	5.0	
D025*		—	39	47	μA	2.0	CVREF Current ⁽¹⁾ (low range)
		—	59	72	μA	3.0	
		—	98	124	μA	5.0	
D026		—	2.0	5.0	μA	2.0	T1OSC Current ⁽¹⁾ , 32.768 kHz
		—	2.5	5.5	μA	3.0	
		—	3.0	7.0	μA	5.0	
D027		—	0.30	1.6	μA	3.0	A/D Current ⁽¹⁾ , no conversion in progress
		—	0.36	1.9	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

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19.4 DC Characteristics: PIC16F913/914/916/917/946-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
D020E	Power-down Base Current (IPD) ⁽²⁾	—	0.05	9	μA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	11	μA	3.0	
		—	0.35	15	μA	5.0	
D021E		—	1	28	μA	2.0	WDT Current ⁽¹⁾
		—	2	30	μA	3.0	
		—	3	35	μA	5.0	
D022E		—	42	65	μA	3.0	BOR Current ⁽¹⁾
		—	85	127	μA	5.0	
D022B		—	22	48	μA	2.0	PLVD Current
		—	25	55	μA	3.0	
		—	33	65	μA	5.0	
D023E		—	32	45	μA	2.0	Comparator Current ⁽¹⁾ , both comparators enabled
		—	60	78	μA	3.0	
		—	120	160	μA	5.0	
D024E		—	30	70	μA	2.0	CVREF Current ⁽¹⁾ (high range)
		—	45	90	μA	3.0	
		—	75	120	μA	5.0	
D025E*		—	39	91	μA	2.0	CVREF Current ⁽¹⁾ (low range)
		—	59	117	μA	3.0	
		—	98	156	μA	5.0	
D026E		—	3.5	18	μA	2.0	T1OSC Current ⁽¹⁾ , 32.768 kHz
		—	4	21	μA	3.0	
		—	5	24	μA	5.0	
D027E		—	0.30	12	μA	3.0	A/D Current ⁽¹⁾ , no conversion in progress
		—	0.36	16	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
- 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

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19.7 Timing Parameter Symbolology

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	\overline{RD}
cs	\overline{CS}	rw	\overline{RD} or \overline{WR}
di	SDI	sc	SCK
do	SDO	ss	\overline{SS}
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	\overline{MCLR}	wr	\overline{WR}

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 19-3: LOAD CONDITIONS

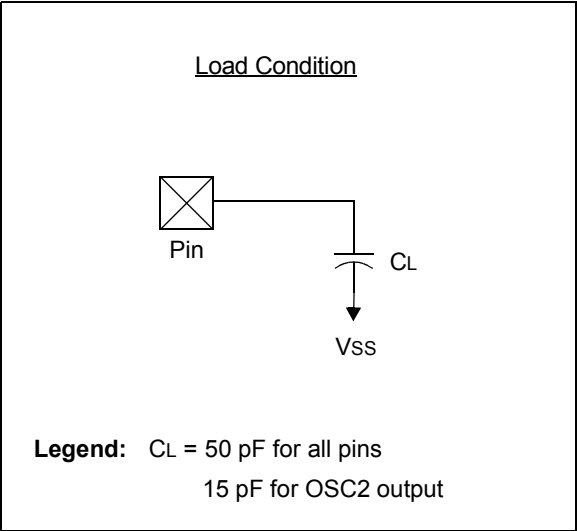


FIGURE 20-12: MAXIMUM I_{DD} vs. F_{OSC} OVER V_{DD} (HFINTOSC MODE)

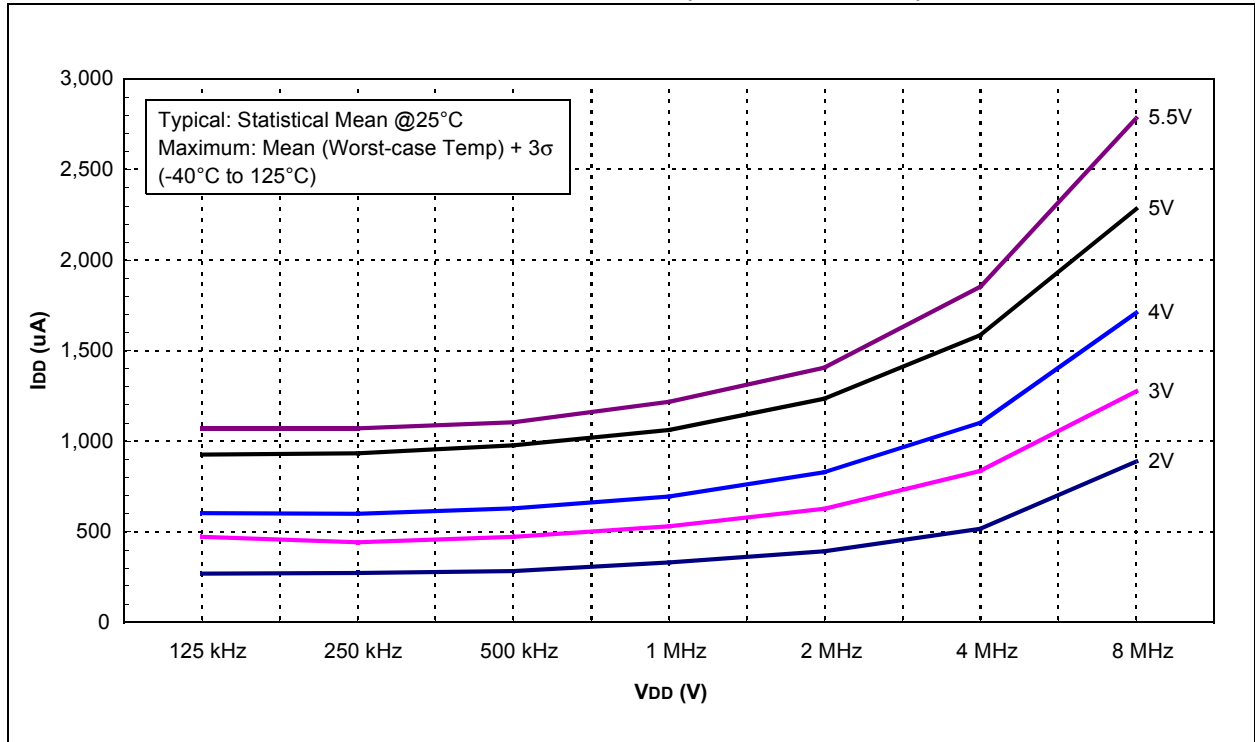
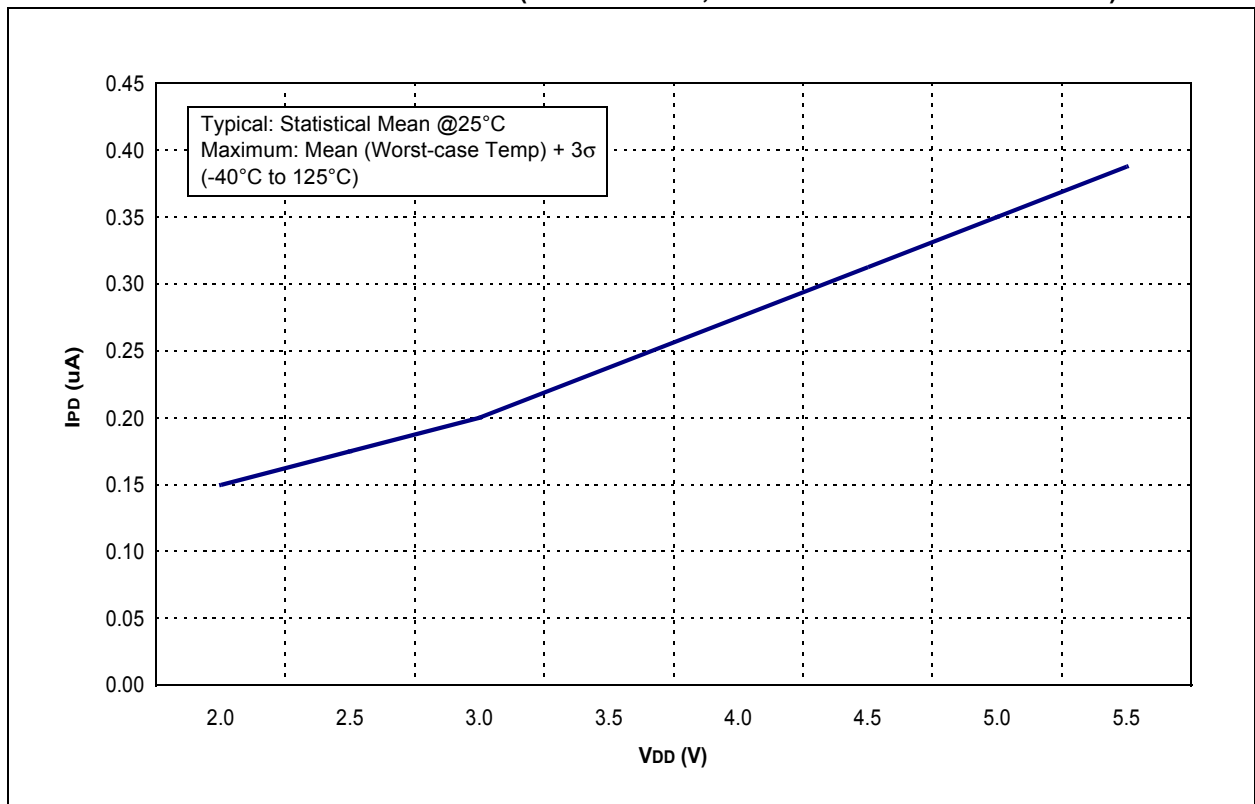


FIGURE 20-13: TYPICAL I_{PD} vs. V_{DD} (SLEEP MODE, ALL PERIPHERALS DISABLED)



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