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Product Status	Active
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Core Size	8-Bit
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Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f916-e-ss

TABLE 3: PIC16F913/916 28-PIN (QFN) SUMMARY

I/O	Pin	A/D	LCD	Comparators	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	27	AN0	SEG12	C1-	—	—	—	—	—	—	—
RA1	28	AN1	SEG7	C2-	—	—	—	—	—	—	—
RA2	1	AN2/VREF-	COM2	C2+	—	—	—	—	—	—	—
RA3	2	AN3/VREF+	SEG15/ COM3	C1+	—	—	—	—	—	—	—
RA4	3	—	SEG4	C1OUT	T0CKI	—	—	—	—	—	—
RA5	4	AN4	SEG5	C2OUT	—	—	—	$\overline{SS}$	—	—	—
RA6	7	—	—	—	T1OSO	—	—	—	—	—	OSC2/CLKOUT
RA7	6	—	—	—	T1OSI	—	—	—	—	—	OSC1/CLKIN
RB0	18	—	SEG0	—	—	—	—	—	INT	Y	—
RB1	19	—	SEG1	—	—	—	—	—	—	Y	—
RB2	20	—	SEG2	—	—	—	—	—	—	Y	—
RB3	21	—	SEG3	—	—	—	—	—	—	Y	—
RB4	22	—	COM0	—	—	—	—	—	IOC	Y	—
RB5	23	—	COM1	—	—	—	—	—	IOC	Y	—
RB6	24	—	SEG14	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCK
RB7	25	—	SEG13	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	8	—	VLCD1	—	—	—	—	—	—	—	—
RC1	9	—	VLCD2	—	—	—	—	—	—	—	—
RC2	10	—	VLCD3	—	—	—	—	—	—	—	—
RC3	11	—	SEG6	—	—	—	—	—	—	—	—
RC4	12	—	SEG11	—	$\overline{T1G}$	—	—	SDO	—	—	—
RC5	13	—	SEG10	—	T1CKI	CCP1	—	—	—	—	—
RC6	14	—	SEG9	—	—	—	TX/CK	SCK/SCL	—	—	—
RC7	15	—	SEG8	—	—	—	RX/DT	SDI/SDA	—	—	—
RE3	26	—	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
—	17	—	—	—	—	—	—	—	—	—	VDD
—	5	—	—	—	—	—	—	—	—	—	VSS
—	16	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pull-up enabled only with external $\overline{MCLR}$ configuration.

TABLE 5: PIC16F914/917 44-PIN (QFN) SUMMARY

I/O	Pin	A/D	LCD	Comparators	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	19	AN0	SEG12	C1-	—	—	—	—	—	—	—
RA1	20	AN1	SEG7	C2-	—	—	—	—	—	—	—
RA2	21	AN2/VREF-	COM2	C2+	—	—	—	—	—	—	—
RA3	22	AN3/VREF+	SEG15	C1+	—	—	—	—	—	—	—
RA4	23	—	SEG4	C1OUT	T0CKI	—	—	—	—	—	—
RA5	24	AN4	SEG5	C2OUT	—	—	—	$\overline{SS}$	—	—	—
RA6	33	—	—	—	T1OSO	—	—	—	—	—	OSC2/CLKOUT
RA7	32	—	—	—	T1OSI	—	—	—	—	—	OSC1/CLKIN
RB0	9	—	SEG0	—	—	—	—	—	INT	Y	—
RB1	10	—	SEG1	—	—	—	—	—	—	Y	—
RB2	11	—	SEG2	—	—	—	—	—	—	Y	—
RB3	12	—	SEG3	—	—	—	—	—	—	Y	—
RB4	14	—	COM0	—	—	—	—	—	IOC	Y	—
RB5	15	—	COM1	—	—	—	—	—	IOC	Y	—
RB6	16	—	SEG14	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCK
RB7	17	—	SEG13	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	34	—	VLCD1	—	—	—	—	—	—	—	—
RC1	35	—	VLCD2	—	—	—	—	—	—	—	—
RC2	36	—	VLCD3	—	—	—	—	—	—	—	—
RC3	37	—	SEG6	—	—	—	—	—	—	—	—
RC4	42	—	SEG11	—	$\overline{T1G}$	—	—	SDO	—	—	—
RC5	43	—	SEG10	—	T1CKI	CCP1	—	—	—	—	—
RC6	44	—	SEG9	—	—	—	TX/CK	SCK/SCL	—	—	—
RC7	1	—	SEG8	—	—	—	RX/DT	SDI/SDA	—	—	—
RD0	38	—	COM3	—	—	—	—	—	—	—	—
RD1	39	—	—	—	—	—	—	—	—	—	—
RD2	40	—	—	—	—	CCP2	—	—	—	—	—
RD3	41	—	SEG16	—	—	—	—	—	—	—	—
RD4	2	—	SEG17	—	—	—	—	—	—	—	—
RD5	3	—	SEG18	—	—	—	—	—	—	—	—
RD6	4	—	SEG19	—	—	—	—	—	—	—	—
RD7	5	—	SEG20	—	—	—	—	—	—	—	—
RE0	25	AN5	SEG21	—	—	—	—	—	—	—	—
RE1	26	AN6	SEG22	—	—	—	—	—	—	—	—
RE2	27	AN7	SEG23	—	—	—	—	—	—	—	—
RE3	18	—	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
—	7	—	—	—	—	—	—	—	—	—	VDD
—	8	—	—	—	—	—	—	—	—	—	VDD
—	28	—	—	—	—	—	—	—	—	—	VDD
—	6	—	—	—	—	—	—	—	—	—	VSS
—	30	—	—	—	—	—	—	—	—	—	VSS
—	13	—	—	—	—	—	—	—	—	—	NC
—	29	—	—	—	—	—	—	—	—	—	NC

Note 1: Pull-up enabled only with external $\overline{MCLR}$ configuration.

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTB change and external RB0/INT/SEG0 pin interrupts.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE(1)	T0IF(2)	INTF	RBIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE:** PORTB Change Interrupt Enable bit(1)
1 = Enables the PORTB change interrupt
0 = Disables the PORTB change interrupt

bit 2 **T0IF:** Timer0 Overflow Interrupt Flag bit(2)
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF:** PORTB Change Interrupt Flag bit
1 = When at least one of the PORTB general purpose I/O pins changed state (must be cleared in software)
0 = None of the PORTB general purpose I/O pins have changed state

Note 1: The appropriate bits in the IOCB register must also be set.
2: T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on Reset and should be initialized before clearing T0IF bit.

2.2.2.5 PIE2 Register

The PIE2 register contains the interrupt enable bits, as shown in Register 2-5.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-5: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0
OSFIE	C2IE	C1IE	LCDIE	—	LVDIE	—	CCP2IE(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enables oscillator fail interrupt
0 = Disables oscillator fail interrupt

bit 6 **C2IE:** Comparator C2 Interrupt Enable bit
1 = Enables Comparator C2 interrupt
0 = Disables Comparator C2 interrupt

bit 5 **C1IE:** Comparator C1 Interrupt Enable bit
1 = Enables Comparator C1 interrupt
0 = Disables Comparator C1 interrupt

bit 4 **LCDIE:** LCD Module Interrupt Enable bit
1 = Enables LCD interrupt
0 = Disables LCD interrupt

bit 3 **Unimplemented:** Read as '0'

bit 2 **LVDIE:** Low Voltage Detect Interrupt Enable bit
1 = Enables LVD Interrupt
0 = Disables LVD Interrupt

bit 1 **Unimplemented:** Read as '0'

bit 0 **CCP2IE:** CCP2 Interrupt Enable bit(1)
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

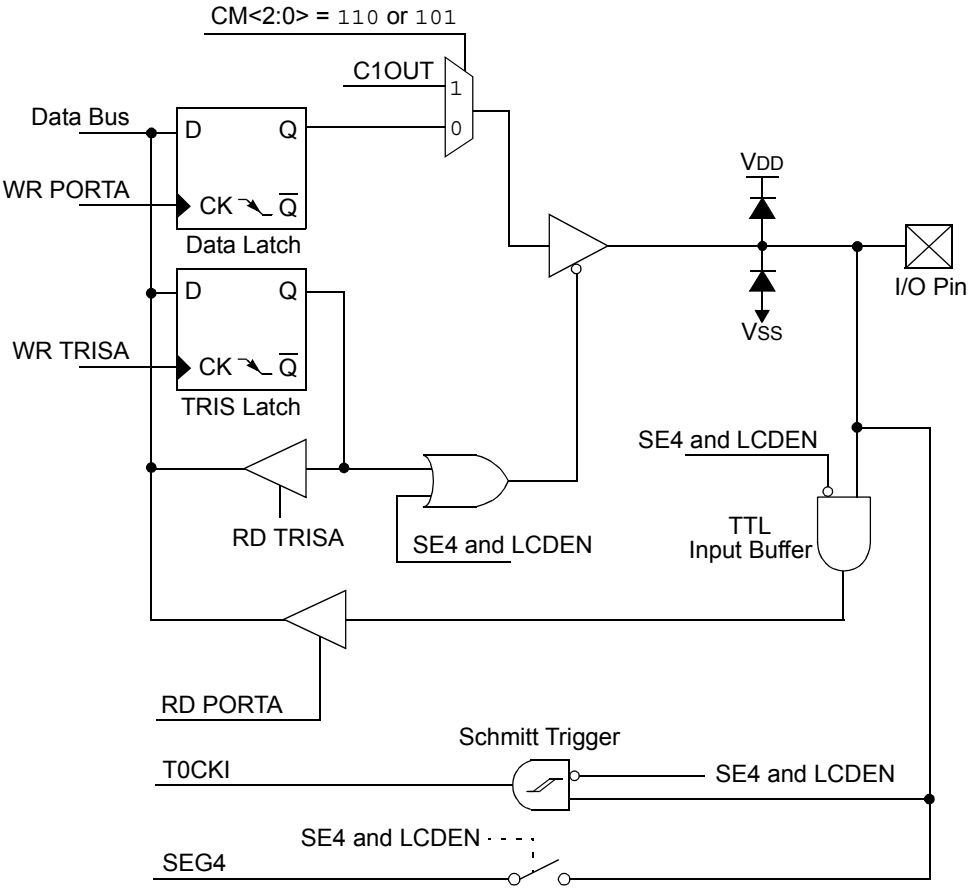
Note 1: PIC16F914/PIC16F917/PIC16F946 only.

3.2.1.5 RA4/C1OUT/T0CKI/SEG4

Figure 3-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- a digital output from Comparator C1
- a clock input for Timer0
- an analog output for the LCD

FIGURE 3-5: BLOCK DIAGRAM OF RA4

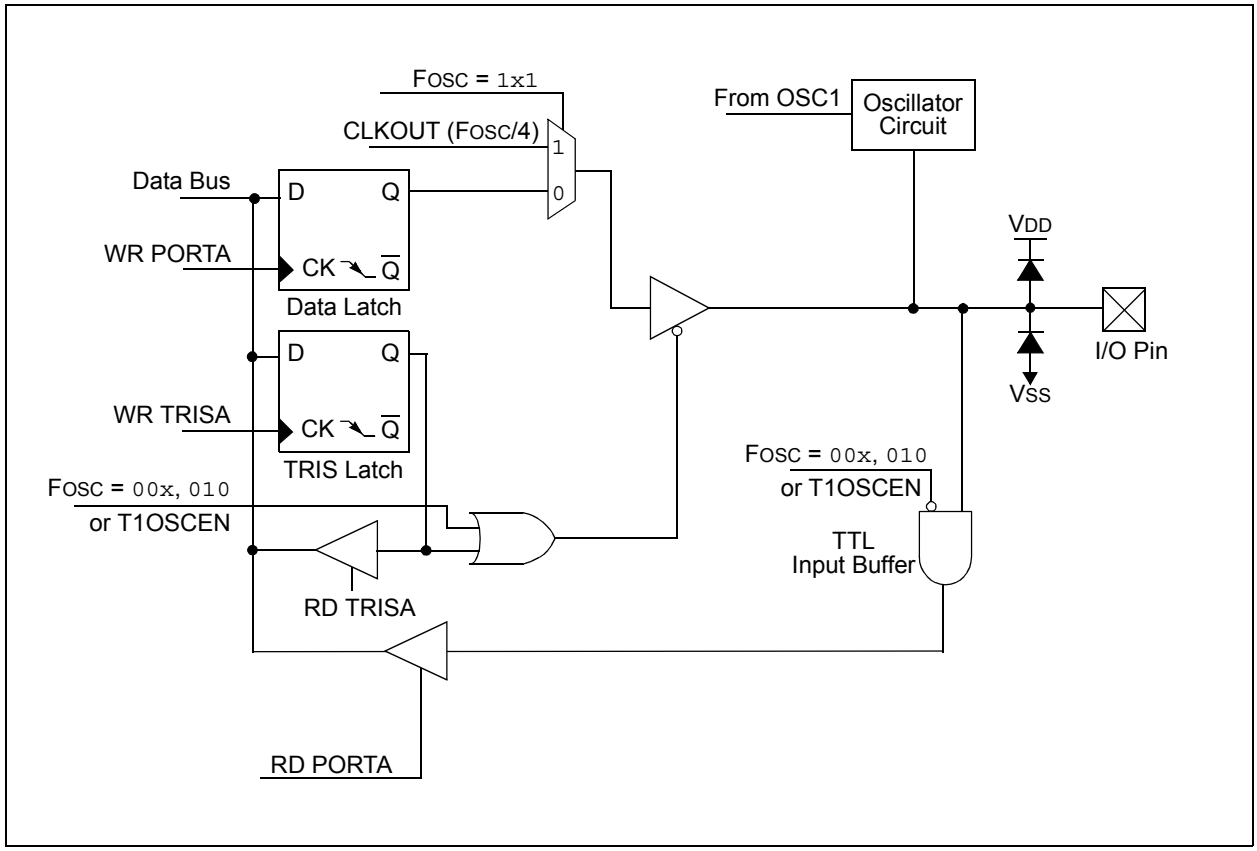


3.2.1.7 RA6/OSC2/CLKOUT/T1OSO

Figure 3-7 shows the diagram for this pin. The RA6 pin is configurable to function as one of the following:

- a general purpose I/O
- a crystal/resonator connection
- a clock output
- a Timer1 oscillator connection

FIGURE 3-7: BLOCK DIAGRAM OF RA6



3.2.1.8 RA7/OSC1/CLKIN/T1OSI

Figure 3-8 shows the diagram for this pin. The RA7 pin is configurable to function as one of the following:

- a general purpose I/O
- a crystal/resonator connection
- a clock input
- a Timer1 oscillator connection

FIGURE 3-8: BLOCK DIAGRAM OF RA7

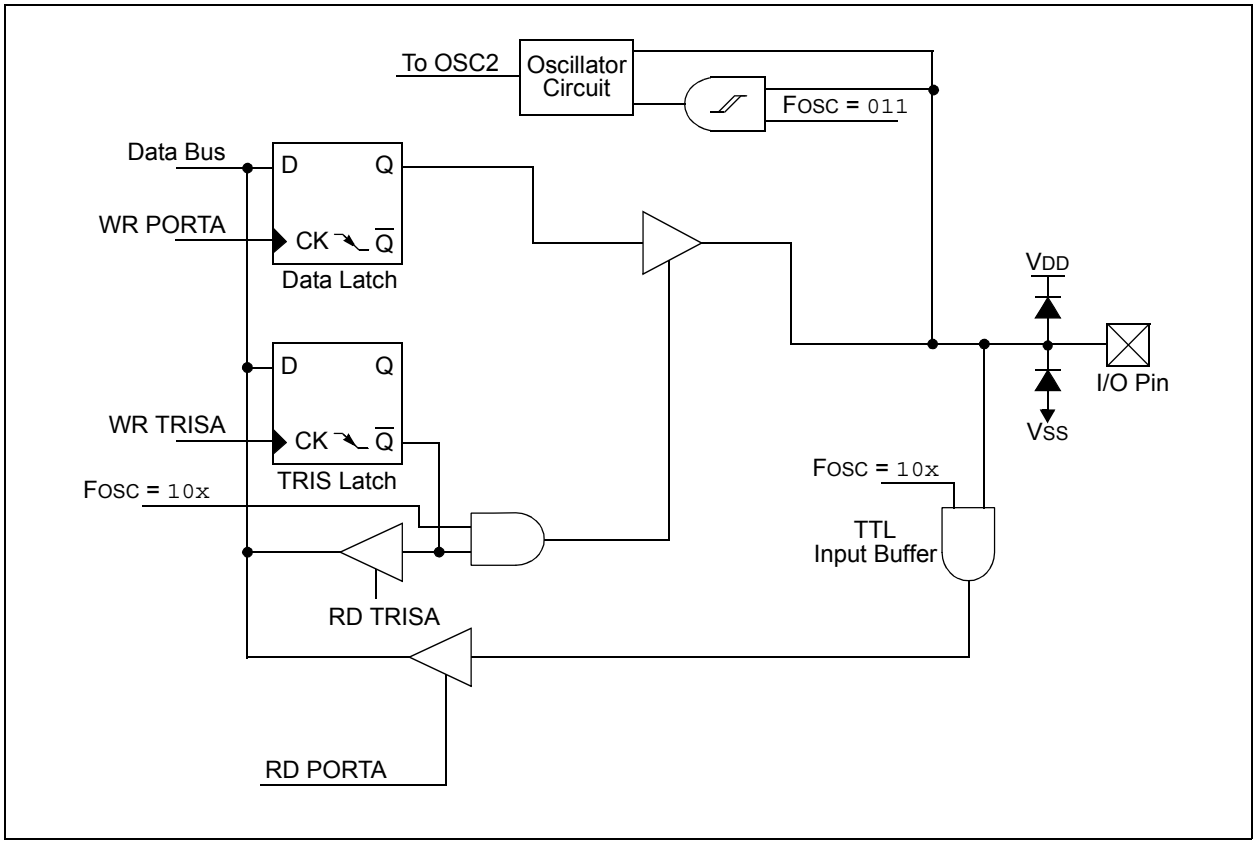


TABLE 3-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	ADFM	VCFG1	VCFG0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
CONFIG(1)	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—
OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
LCDCON	LCDEN	$\overline{\text{SLPEN}}$	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE0	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	0000 0000	uuuu uuuu
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	uuuu uuuu
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx xxxx	uuuu uuuu
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.
Note 1: See Configuration Word register (CONFIG) for operation of all register bits.

FIGURE 3-15: BLOCK DIAGRAM OF RC1

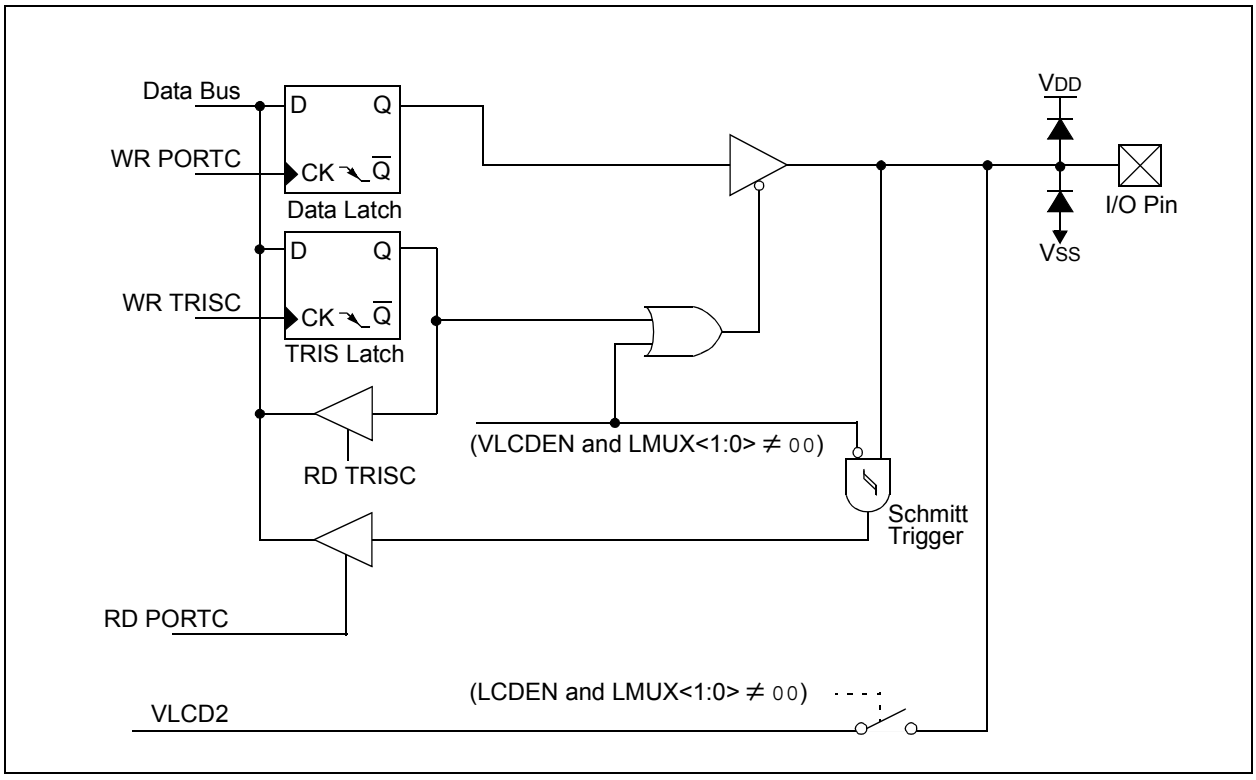
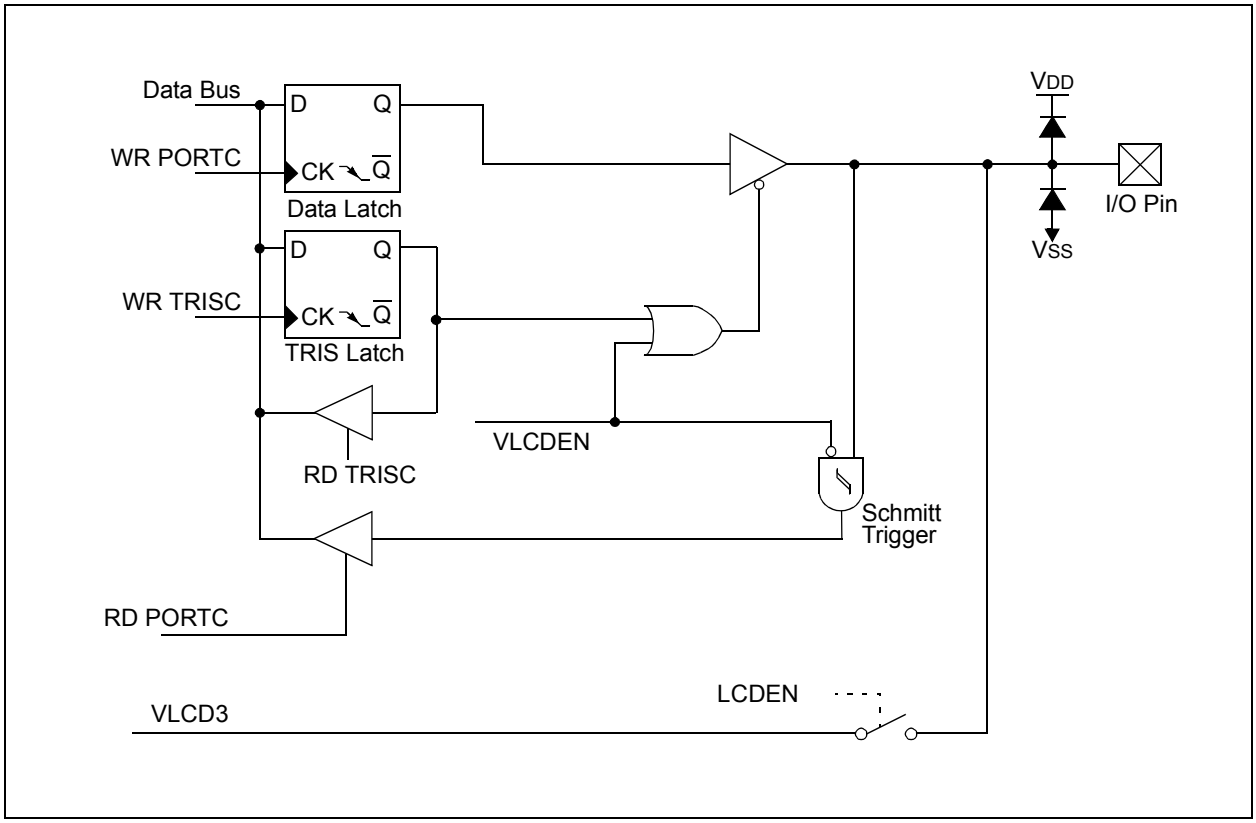


FIGURE 3-16: BLOCK DIAGRAM OF RC2



3.7.1 PIN DESCRIPTIONS AND DIAGRAMS

Each PORTE pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the Comparator or the ADC, refer to the appropriate section in this data sheet.

3.7.1.1 RE0/AN5/SEG21(1)

Figure 3-26 shows the diagram for this pin. The RE0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog output for the LCD

3.7.1.2 RE1/AN6/SEG22(1)

Figure 3-26 shows the diagram for this pin. The RE1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog output for the LCD

3.7.1.3 RE2/AN7/SEG23(1)

Figure 3-26 shows the diagram for this pin. The RE2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog output for the LCD

3.7.1.4 RE3/$\overline{\text{MCLR}}$/VPP

Figure 3-27 shows the diagram for this pin. The RE3 pin is configurable to function as one of the following:

- a digital input only
- as Master Clear Reset with weak pull-up
- a programming voltage reference input

3.7.1.5 RE4/SEG24(2)

Figure 3-28 shows the diagram for this pin. The RE4/SEG24 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog output for the LCD

3.7.1.6 RE5/SEG25(2)

Figure 3-28 shows the diagram for this pin. The RE5/SEG25 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog output for the LCD

3.7.1.7 RE6/SEG26(2)

Figure 3-28 shows the diagram for this pin. The RE6/SEG26 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog output for the LCD

3.7.1.8 RE7/SEG27(2)

Figure 3-28 shows the diagram for this pin. The RE7/SEG27 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog output for the LCD

Note 1: Pin is available on the PIC16F914/917 and PIC16F946 only.

2: Pin is available on the PIC16F946 only.

4.4.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 4-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

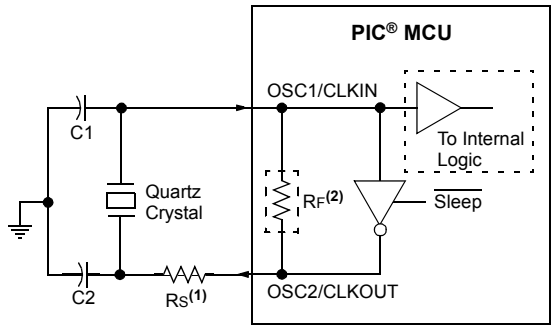
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 4-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: A series resistor (RS) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

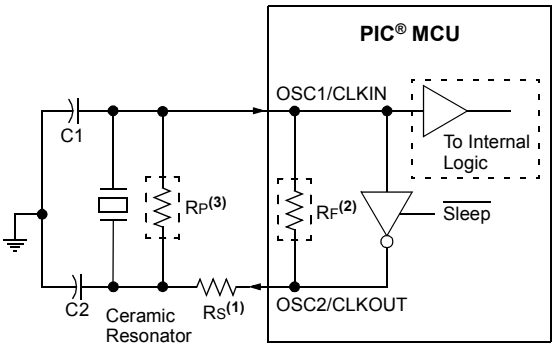
Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)

FIGURE 4-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)

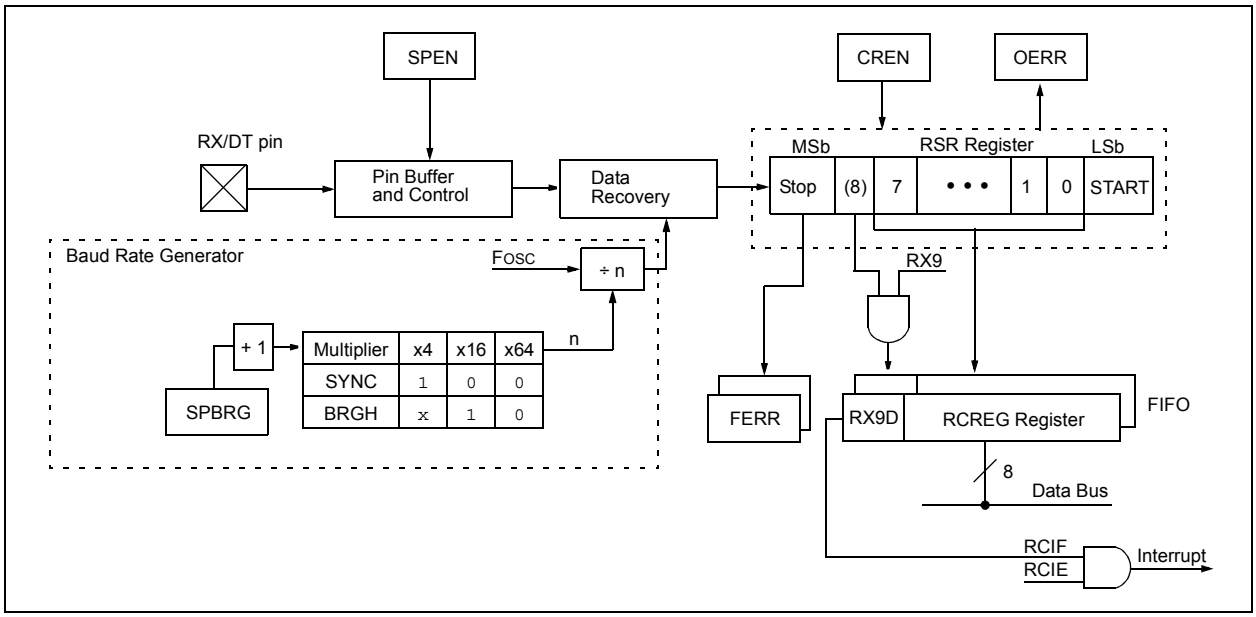


Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

FIGURE 9-2: AUSART RECEIVE BLOCK DIAGRAM

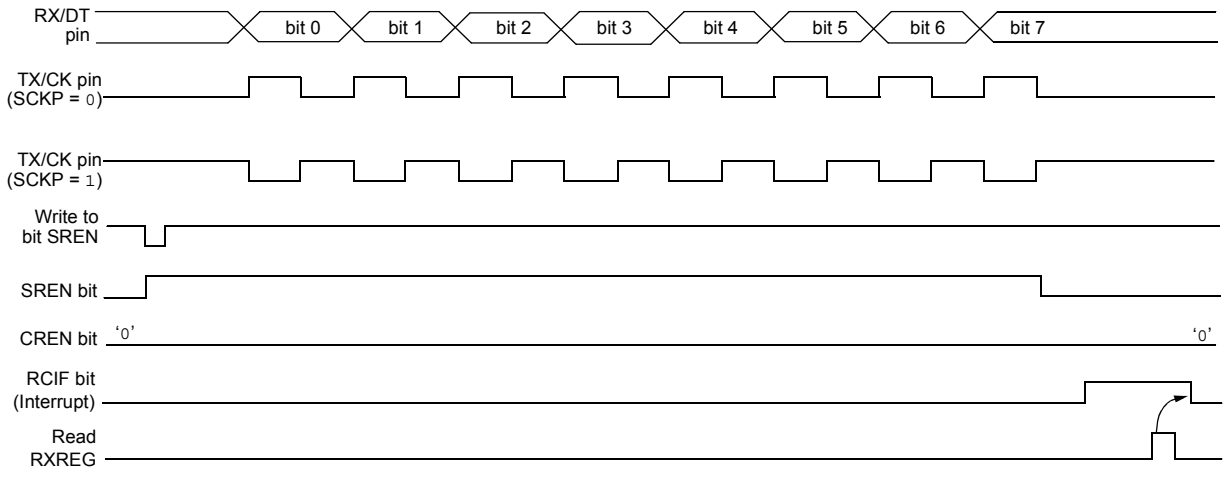


The operation of the AUSART module is controlled through two registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)

These registers are detailed in Register 9-1 and Register 9-2 respectively.

FIGURE 9-8: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

TABLE 9-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
LCDCON	LCDEN	$\overline{\text{SLPEN}}$	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	0000 0000
PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCREG	AUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	0000 000X
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Master Reception.

10.2 LCD Clock Source Selection

The LCD driver module has 3 possible clock sources:

- FOSC/8192
- T1OSC/32
- LFINTOSC/32

The first clock source is the system clock divided by 8192 (FOSC/8192). This divider ratio is chosen to provide about 1 kHz output when the system clock is 8 MHz. The divider is not programmable. Instead, the LCD prescaler bits LP<3:0> of the LCDPS register are used to set the LCD frame clock rate.

The second clock source is the T1OSC/32. This also gives about 1 kHz when a 32.768 kHz crystal is used with the Timer1 oscillator. To use the Timer1 oscillator as a clock source, the T1OSCEN bit of the T1CON register should be set.

The third clock source is the 31 kHz LFINTOSC/32, which provides approximately 1 kHz output.

The second and third clock sources may be used to continue running the LCD while the processor is in Sleep.

Using bits CS<1:0> of the LCDCON register can select any of these clock sources.

10.2.1 LCD PRESCALER

A 4-bit counter is available as a prescaler for the LCD clock. The prescaler is not directly readable or writable; its value is set by the LP<3:0> bits of the LCDPS register, which determine the prescaler assignment and prescale ratio.

The prescale values are selectable from 1:1 through 1:16.

10.3 LCD Bias Types

The LCD driver module can be configured into one of three bias types:

- Static Bias (2 voltage levels: VSS and VDD)
- 1/2 Bias (3 voltage levels: VSS, 1/2 VDD and VDD)
- 1/3 Bias (4 voltage levels: VSS, 1/3 VDD, 2/3 VDD and VDD)

This module uses an external resistor ladder to generate the LCD bias voltages.

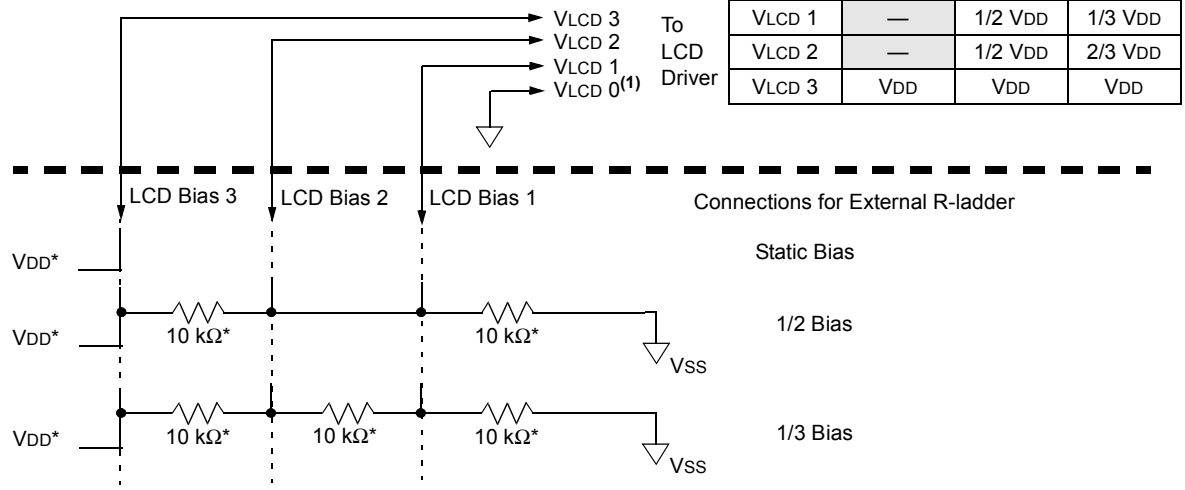
The external resistor ladder should be connected to the VLCD1 pin (Bias 1), VLCD2 pin (Bias 2), VLCD3 pin (Bias 3) and VSS. The VLCD3 pin should also be connected to VDD.

Figure 10-2 shows the proper way to connect the resistor ladder to the Bias pins..

Note:	VLCD pins used to supply LCD bias voltage are enabled on power-up (POR) and must be disabled by the user by clearing the VLCDEN bit of the LCDCON register.

FIGURE 10-2: LCD BIAS RESISTOR LADDER CONNECTION DIAGRAM

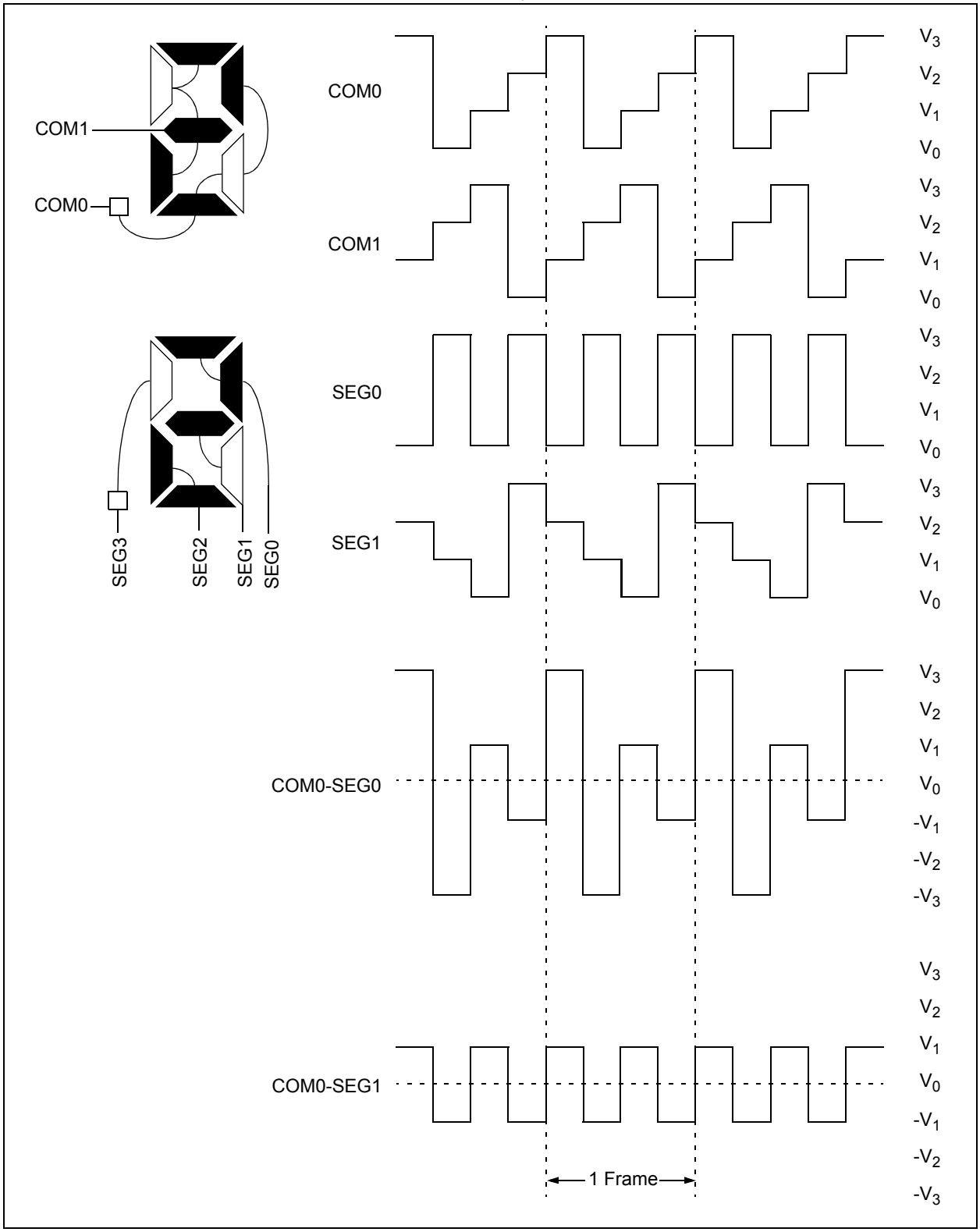
	Static Bias	1/2 Bias	1/3 Bias
VLCD 0	VSS	VSS	VSS
VLCD 1	—	1/2 VDD	1/3 VDD
VLCD 2	—	1/2 VDD	2/3 VDD
VLCD 3	VDD	VDD	VDD



* These values are provided for design guidance only and should be optimized for the application by the designer.

Note 1: Internal connection.

FIGURE 10-9: TYPE-A WAVEFORMS IN 1/2 MUX, 1/3 BIAS DRIVE



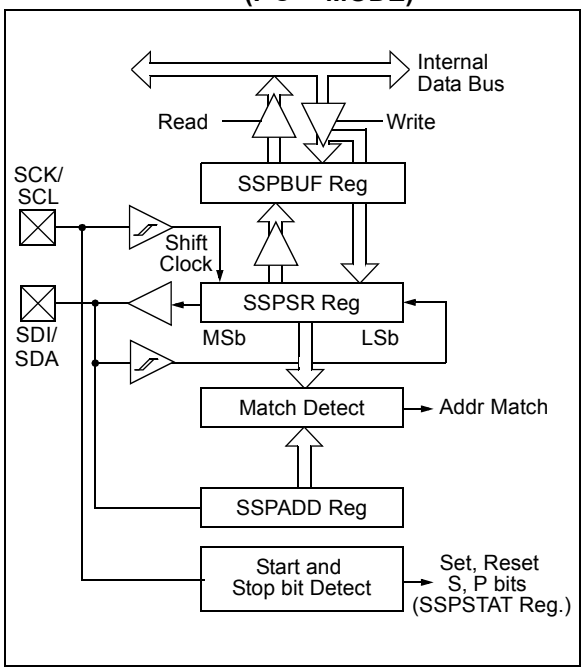
14.11 SSP I²C Operation

The SSP module in I²C mode, fully implements all slave functions, except general call support, and provides interrupts on Start and Stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the Standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer. These are the RC6/TX/CK/SCK/SCL/SEG9 pin, which is the clock (SCL), and the RC7/RX/DT/SDI/SDA/SEG8 pin, which is the data (SDA).

The SSP module functions are enabled by setting SSP enable bit SSPEN (SSPCON<5>).

FIGURE 14-7: SSP BLOCK DIAGRAM (I²C™ MODE)



The SSP module has five registers for the I²C operation, which are listed below.

- SSP Control register (SSPCON)
- SSP STATUS register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift register (SSPSR) – Not directly accessible
- SSP Address register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with Start and Stop bit interrupts enabled to support Firmware Master mode
- I²C Slave mode (10-bit address), with Start and Stop bit interrupts enabled to support Firmware Master mode
- I²C Start and Stop bit interrupts enabled to support Firmware Master mode; Slave is idle

Selection of any I²C mode with the SSPEN bit set forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I²C module.

14.12 Slave Mode

In Slave mode, the SCL and SDA pins must be configured as inputs (TRISC<7,6> are set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge ($\overline{ACK}$) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this $\overline{ACK}$ pulse. They include (either or both):

a) The Buffer Full bit BF of the SSPSTAT register was set before the transfer was received.

b) The overflow bit SSPOV of the SSPCON register was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF of the PIR1 register is set. Table 14-3 shows the results of when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. For high and low times of the I²C specification, as well as the requirements of the SSP module, see **Section 19.0 "Electrical Specifications"**.

14.12.1 ADDRESSING

Once the SSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of register SSPADD <7:1>. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

a) The SSPSR register value is loaded into the SSPBUF register.
b) The buffer full bit, BF is set.
c) An $\overline{ACK}$ pulse is generated.
d) SSP interrupt flag bit, SSPIF of the PIR1 register is set (interrupt is generated if enabled) on the falling edge of the ninth SCL pulse.

In 10-bit Address mode, two address bytes need to be received by the slave (Figure 14-8). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/$\overline{W}$ (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address.

The sequence of events for 10-bit address is as follows, with steps 7-9 for slave-transmitter:

1. Receive first (high) byte of address (bits SSPIF, BF and bit UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with second (low) byte of address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of address (bits SSPIF, BF and UA are set).
5. Update the SSPADD register with the first (high) byte of address; if match releases SCL line, this will clear bit UA.
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive repeated Start condition.
8. Receive first (high) byte of address (bits SSPIF and BF are set).
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

TABLE 14-3: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received		SSPSR → SSPBUF	Generate $\overline{ACK}$ Pulse	Set bit SSPIF (SSP Interrupt occurs if enabled)
BF	SSPOV			
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

Note: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

16.2.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register selects one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit of the PCON register enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 16-1 for the Configuration Word definition.

If VDD falls below VBOR for greater than parameter (TBOR) (see **Section 19.0 "Electrical Specifications"**), the Brown-out situation will reset the device. This will occur regardless of VDD slew rate. A Reset is not insured to occur if VDD falls below VBOR for less than parameter (TBOR).

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 16-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional 64 ms.

Note: The Power-up Timer is enabled by the $\overline{\text{PWRTE}}$ bit in the Configuration Word.

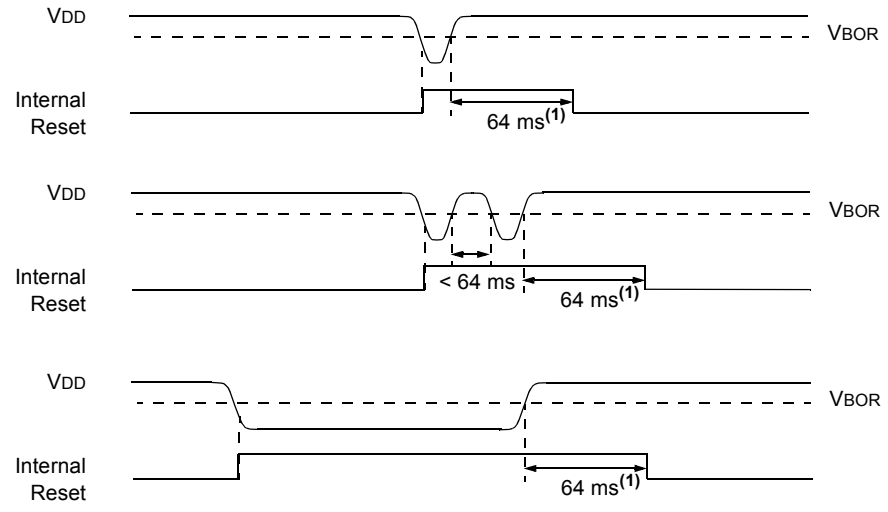
If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

16.2.5 BOR CALIBRATION

The PIC16F91X/946 stores the BOR calibration values in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the "*PIC16F91X/946 Memory Programming Specification*" (DS41244) and thus, does not require reprogramming.

Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F91X/946 Memory Programming Specification*" (DS41244) for more information.

FIGURE 16-3: BROWN-OUT SITUATIONS



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.

FIGURE 16-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{MCLR}$): CASE 1

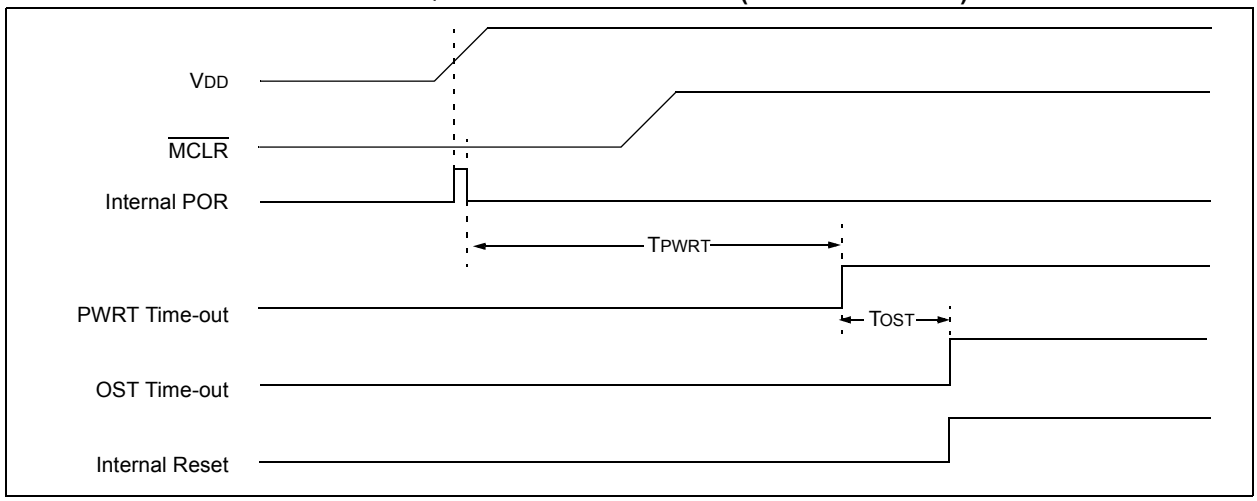


FIGURE 16-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{MCLR}$): CASE 2

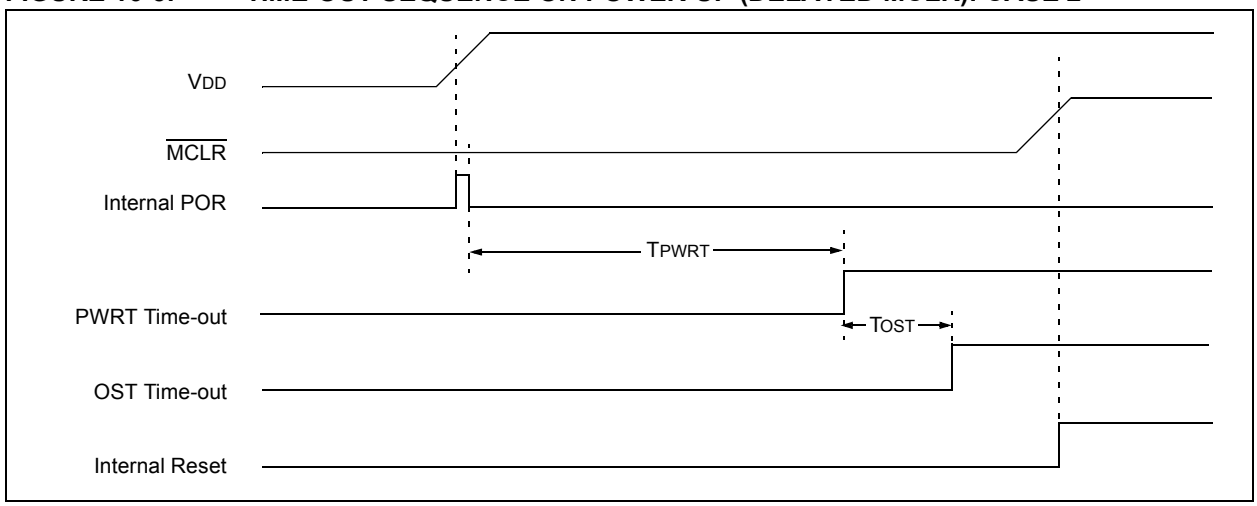
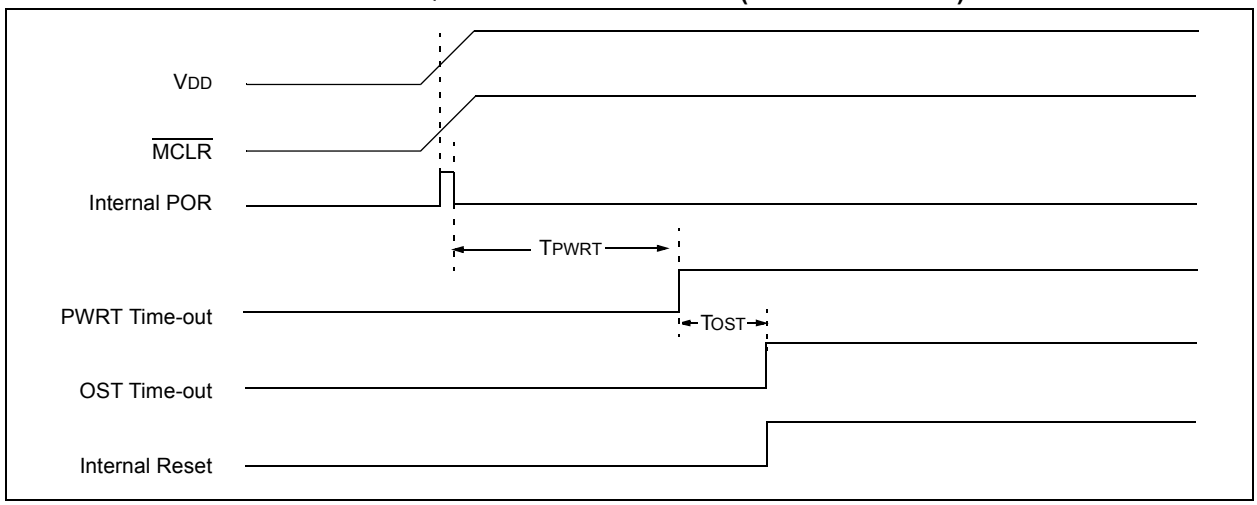


FIGURE 16-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ WITH VDD): CASE 3



18.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

18.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

18.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

18.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

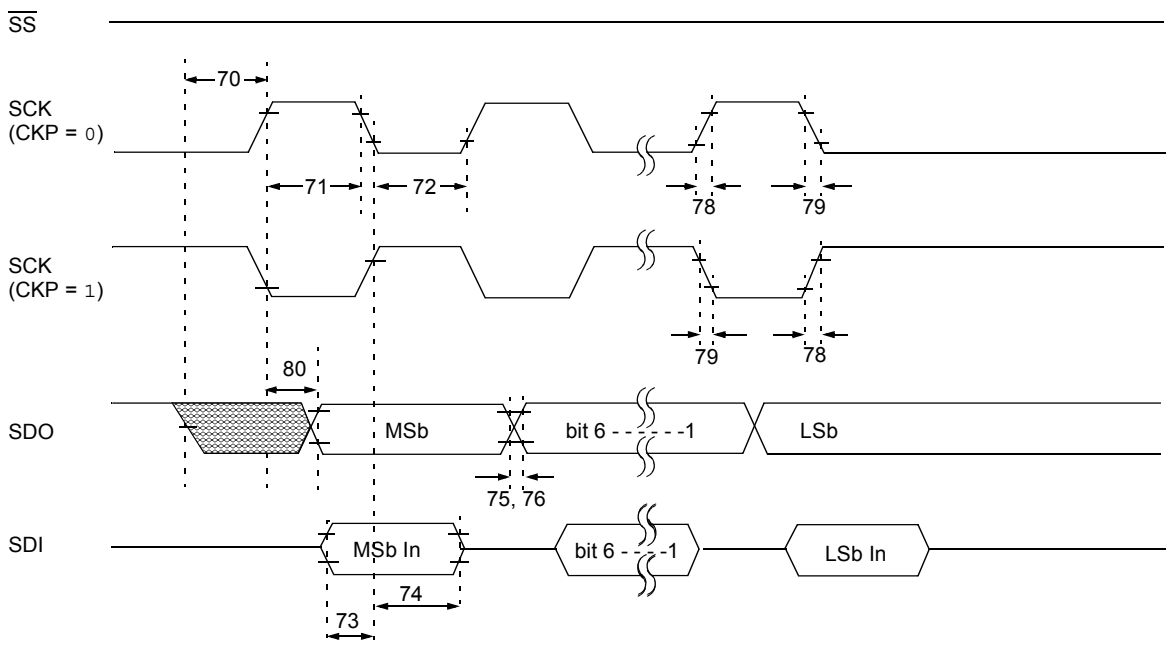
- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

18.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

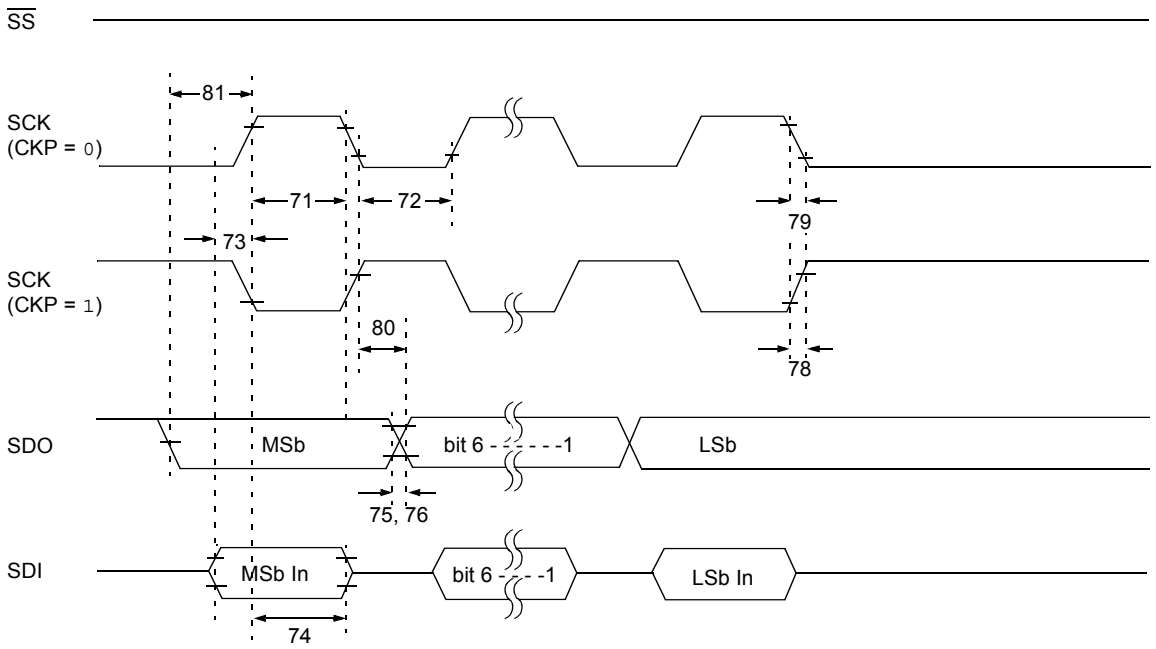
The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

FIGURE 19-14: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)



Note: Refer to Figure 19-3 for load conditions.

FIGURE 19-15: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 19-3 for load conditions.