Microchip Technology - PIC16F916T-I/SS Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f916t-i-ss

PIC16F913/914/916/917/946

28/40/44/64-Pin Flash-Based, 8-Bit CMOS Microcontrollers with LCD Driver and nanoWatt Technology

High-Performance RISC CPU:

- Only 35 instructions to learn:
  - All single-cycle instructions except branches
- Operating speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Program Memory Read (PMR) capability
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range of 8 MHz to 125 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - External Oscillator fail detect for critical applications
  - Clock mode switching during operation for power savings
- Software selectable 31 kHz internal oscillator
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended temperature range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM retention: > 40 years

Low-Power Features:

- Standby Current:
  - <100 nA @ 2.0V, typical
- Operating Current:
  - 11 μA @ 32 kHz, 2.0V, typical
  - 220 μA @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical

Peripheral Features:

- Liquid Crystal Display module:
  - Up to 60/96/168 pixel drive capability on 28/40/64-pin devices, respectively
  - Four commons
- Up to 24/35/53 I/O pins and 1 input-only pin:
  - High-current source/sink for direct LED drive
  - Interrupt-on-change pin
  - Individually programmable weak pull-ups
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Analog comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (CV_{REF}) module (% of V_{DD})
  - Comparator inputs and outputs externally accessible
- A/D Converter:
  - 10-bit resolution and up to 8 channels
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 as Timer1 oscillator if INTOSCIO or LP mode is selected
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART)
- Up to 2 Capture, Compare, PWM modules:
  - 16-bit Capture, max. resolution 12.5 ns
  - 16-bit Compare, max. resolution 200 ns
  - 10-bit PWM, max. frequency 20 kHz
- Synchronous Serial Port (SSP) with I^2C™

TABLE 2: PIC16F913/916 28-PIN (PDIP, SOIC, SSOP) SUMMARY

I/O	Pin	A/D	LCD	Comparators	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	2	AN0	SEG12	C1-	—	—	—	—	—	—	—
RA1	3	AN1	SEG7	C2-	—	—	—	—	—	—	—
RA2	4	AN2/VREF-	COM2	C2+	—	—	—	—	—	—	—
RA3	5	AN3/VREF+	SEG15/ COM3	C1+	—	—	—	—	—	—	—
RA4	6	—	SEG4	C1OUT	T0CKI	—	—	—	—	—	—
RA5	7	—	SEG5	C2OUT	—	—	—	$\overline{SS}$	—	—	—
RA6	10	—	—	—	T1OSO	—	—	—	—	—	OSC2/CLKOUT
RA7	9	—	—	—	T1OSI	—	—	—	—	—	OSC1/CLKIN
RB0	21	—	SEG0	—	—	—	—	—	INT	Y	—
RB1	22	—	SEG1	—	—	—	—	—	—	Y	—
RB2	23	—	SEG2	—	—	—	—	—	—	Y	—
RB3	24	—	SEG3	—	—	—	—	—	—	Y	—
RB4	25	—	COM0	—	—	—	—	—	IOC	Y	—
RB5	26	—	COM1	—	—	—	—	—	IOC	Y	—
RB6	27	—	SEG14	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCK
RB7	28	—	SEG13	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	11	—	VLCD1	—	—	—	—	—	—	—	—
RC1	12	—	VLCD2	—	—	—	—	—	—	—	—
RC2	13	—	VLCD3	—	—	—	—	—	—	—	—
RC3	14	—	SEG6	—	—	—	—	—	—	—	—
RC4	15	—	SEG11	—	$\overline{T1G}$	—	—	SDO	—	—	—
RC5	16	—	SEG10	—	T1CKI	CCP1	—	—	—	—	—
RC6	17	—	SEG9	—	—	—	TX/CK	SCK/SCL	—	—	—
RC7	18	—	SEG8	—	—	—	RX/DT	SDI/SDA	—	—	—
RE3	1	—	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
—	20	—	—	—	—	—	—	—	—	—	VDD
—	8	—	—	—	—	—	—	—	—	—	VSS
—	19	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pull-up enabled only with external $\overline{MCLR}$ configuration.

TABLE 1-1: PIC16F91X/946 PINOUT DESCRIPTIONS (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB1/SEG1	RB1	TTL	CMOS	General purpose I/O. Individually enabled pull-up.
	SEG1	—	AN	LCD analog output.
RB2/SEG2	RB2	TTL	CMOS	General purpose I/O. Individually enabled pull-up.
	SEG2	—	AN	LCD analog output.
RB3/SEG3	RB3	TTL	CMOS	General purpose I/O. Individually enabled pull-up.
	SEG3	—	AN	LCD analog output.
RB4/COM0	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	COM0	—	AN	LCD analog output.
RB5/COM1	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	COM1	—	AN	LCD analog output.
RB6/ICSPCLK/ICDCK/SEG14	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPCLK	ST	—	ICSP™ clock.
	ICDCK	ST	—	ICD clock.
	SEG14	—	AN	LCD analog output.
RB7/ICSPDAT/ICDDAT/SEG13	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPDAT	ST	CMOS	ICSP Data I/O.
	ICDDAT	ST	CMOS	ICD Data I/O.
	SEG13	—	AN	LCD analog output.
RC0/VLCD1	RC0	ST	CMOS	General purpose I/O.
	VLCD1	AN	—	LCD analog input.
RC1/VLCD2	RC1	ST	CMOS	General purpose I/O.
	VLCD2	AN	—	LCD analog input.
RC2/VLCD3	RC2	ST	CMOS	General purpose I/O.
	VLCD3	AN	—	LCD analog input.
RC3/SEG6	RC3	ST	CMOS	General purpose I/O.
	SEG6	—	AN	LCD analog output.
RC4/$\overline{T1G}$/SDO/SEG11	RC4	ST	CMOS	General purpose I/O.
	$\overline{T1G}$	ST	—	Timer1 gate input.
	SDO	—	CMOS	Serial data output.
	SEG11	—	AN	LCD analog output.
RC5/T1CKI/CCP1/SEG10	RC5	ST	CMOS	General purpose I/O.
	T1CKI	ST	—	Timer1 clock input.
	CCP1	ST	CMOS	Capture 1 input/Compare 1 output/PWM 1 output.
	SEG10	—	AN	LCD analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels P = Power
HV = High Voltage XTAL = Crystal

Note 1: COM3 is available on RA3 for the PIC16F913/916 and on RD0 for the PIC16F914/917 and PIC16F946.
2: Pins available on PIC16F914/917 and PIC16F946 only.
3: Pins available on PIC16F946 only.
4: I^2C Schmitt trigger inputs have special input levels.

FIGURE 2-4: PIC16F914/917 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr. (1)	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	LCDCON	107h		187h
PORTD	08h	TRISD	88h	LCDPS	108h		188h
PORTE	09h	TRISE	89h	LVDCON	109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATL	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADRL	10Dh	EECON2(1)	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCTUNE	90h	LCDDATA0	110h		190h
TMR2	11h	ANSEL	91h	LCDDATA1	111h		
T2CON	12h	PR2	92h	LCDDATA2	112h		
SSPBUF	13h	SSPADD	93h	LCDDATA3	113h		
SSPCON	14h	SSPSTAT	94h	LCDDATA4	114h		
CCPR1L	15h	WPUB	95h	LCDDATA5	115h		
CCPR1H	16h	IOCB	96h	LCDDATA6	116h		
CCP1CON	17h	CMCON1	97h	LCDDATA7	117h		
RCSTA	18h	TXSTA	98h	LCDDATA8	118h		
TXREG	19h	SPBRG	99h	LCDDATA9	119h	General Purpose Register(2)	
RCREG	1Ah		9Ah	LCDDATA10	11Ah		
CCPR2L	1Bh		9Bh	LCDDATA11	11Bh		
CCPR2H	1Ch	CMCON0	9Ch	LCDSE0	11Ch		
CCP2CON	1Dh	VRCON	9Dh	LCDSE1	11Dh	96 Bytes	
ADRESH	1Eh	ADRESL	9Eh	LCDSE2	11Eh		
ADCON0	1Fh	ADCON1	9Fh		11Fh		
	20h		A0h		120h		
General Purpose Register 96 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes			
			EFh		16Fh		1EFh
		accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h	accesses 70h-7Fh	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: On the PIC16F914, unimplemented data memory locations, read as '0'.

FIGURE 2-5: PIC16F946 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr. (1)	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h	TRISF	185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	LCDCON	107h	TRISG	187h
PORTD	08h	TRISD	88h	LCDPS	108h	PORTF	188h
PORTE	09h	TRISE	89h	LVDCON	109h	PORTG	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATL	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADRL	10Dh	EECON2(1)	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCTUNE	90h	LCDDATA0	110h	LCDDATA12	190h
TMR2	11h	ANSEL	91h	LCDDATA1	111h	LCDDATA13	191h
T2CON	12h	PR2	92h	LCDDATA2	112h	LCDDATA14	192h
SSPBUF	13h	SSPADD	93h	LCDDATA3	113h	LCDDATA15	193h
SSPCON	14h	SSPSTAT	94h	LCDDATA4	114h	LCDDATA16	194h
CCPR1L	15h	WPUB	95h	LCDDATA5	115h	LCDDATA17	195h
CCPR1H	16h	IOCB	96h	LCDDATA6	116h	LCDDATA18	196h
CCP1CON	17h	CMCON1	97h	LCDDATA7	117h	LCDDATA19	197h
RCSTA	18h	TXSTA	98h	LCDDATA8	118h	LCDDATA20	198h
TXREG	19h	SPBRG	99h	LCDDATA9	119h	LCDDATA21	199h
RCREG	1Ah		9Ah	LCDDATA10	11Ah	LCDDATA22	19Ah
CCPR2L	1Bh		9Bh	LCDDATA11	11Bh	LCDDATA23	19Bh
CCPR2H	1Ch	CMCON0	9Ch	LCDSE0	11Ch	LCDSE3	19Ch
CCP2CON	1Dh	VRCON	9Dh	LCDSE1	11Dh	LCDSE4	19Dh
ADRESH	1Eh	ADRESL	9Eh	LCDSE2	11Eh	LCDSE5	19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h – 7Fh	General Purpose Register 80 Bytes	A0h – EFh	General Purpose Register 80 Bytes	120h – 16Fh	General Purpose Register 80 Bytes	1A0h – 1EFh
accesses 70h-7Fh		accesses 70h-7Fh	F0h – FFh	accesses 70h-7Fh	170h – 17Fh	accesses 70h-7Fh	1F0h – 1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

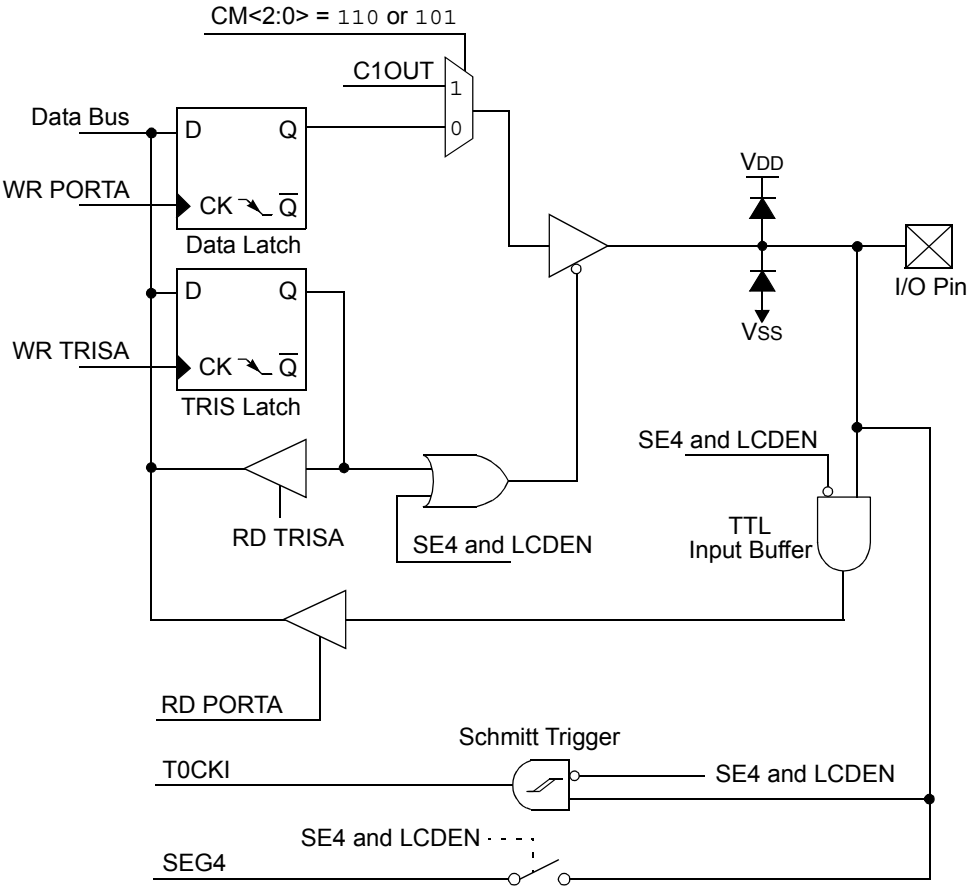
Note 1: Not a physical register.

3.2.1.5 RA4/C1OUT/T0CKI/SEG4

Figure 3-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- a digital output from Comparator C1
- a clock input for Timer0
- an analog output for the LCD

FIGURE 3-5: BLOCK DIAGRAM OF RA4

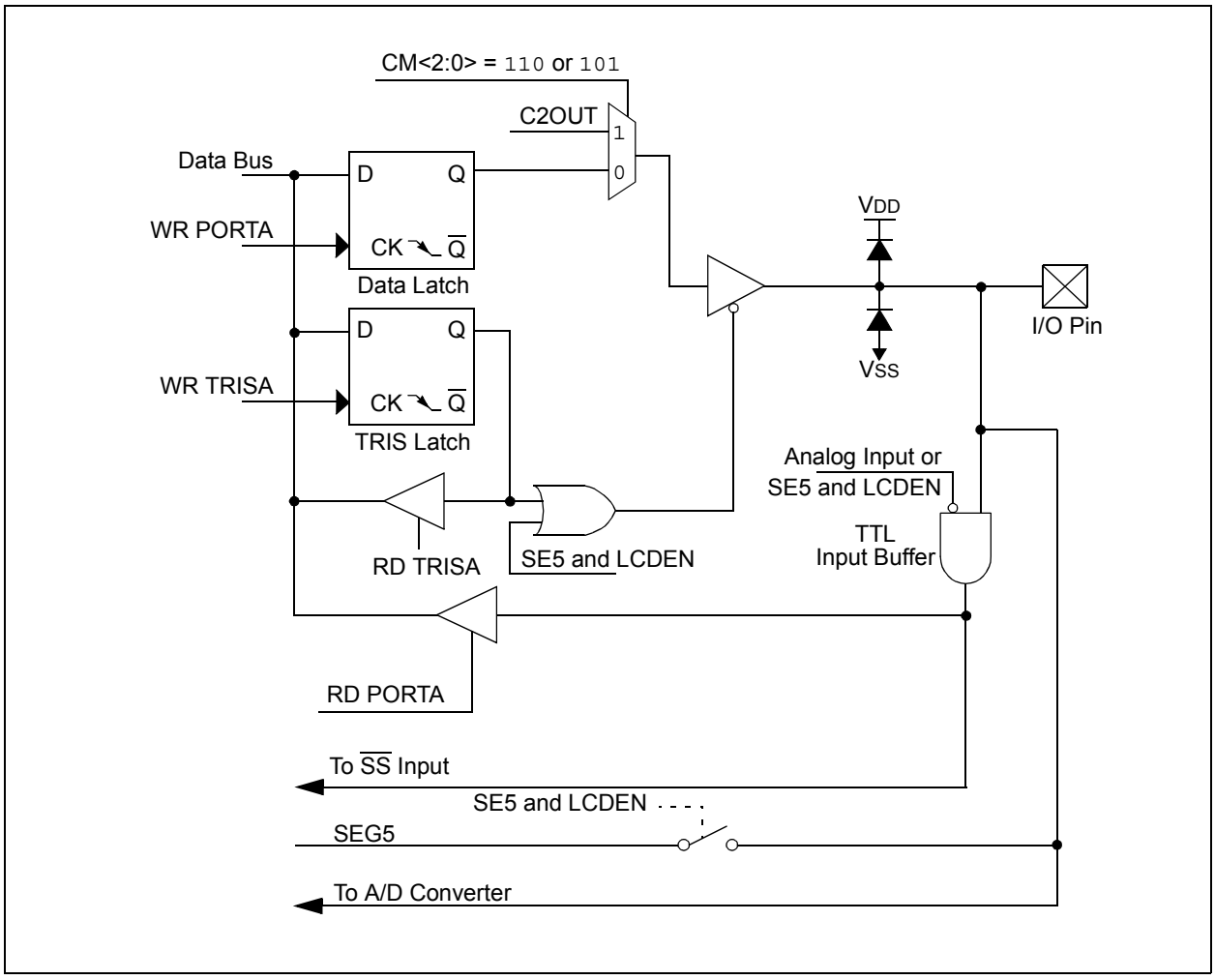


3.2.1.6 RA5/AN4/C2OUT/$\overline{SS}$/SEG5

Figure 3-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- a general purpose I/O
- a digital output from Comparator C2
- a slave select input
- an analog output for the LCD
- an analog input for the ADC

FIGURE 3-6: BLOCK DIAGRAM OF RA5



3.6 PORTD and TRISD Registers

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configured as an input or output. PORTD is only available on the PIC16F914/917 and PIC16F946.

EXAMPLE 3-4: INITIALIZING PORTD

```
BANKSEL PORTD       ;
CLRF    PORTD       ;Init PORTD
BANKSEL TRISD       ;
MOVLW   0FF         ;Set RD<7:0> as inputs
MOVWF   TRISD       ;
```

REGISTER 3-10: PORTD: PORTD REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **RD<7:0>**: PORTD I/O Pin bits
1 = Port pin is >VIH min.
0 = Port pin is <VIL max.

REGISTER 3-11: TRISD: PORTD TRI-STATE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **TRISD<7:0>:** PORTD Tri-State Control bits
1 = PORTD pin configured as an input (tri-stated)
0 = PORTD pin configured as an output

6.10 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 6-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 6-1: T1CON: TIMER 1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV(1)	TMR1GE(2)	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **T1GINV:** Timer1 Gate Invert bit(1)
1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 6 **TMR1GE:** Timer1 Gate Enable bit(2)
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 counting is controlled by the Timer1 Gate function
0 = Timer1 is always counting

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If INTOSC without CLKOUT oscillator is active:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
Else:
This bit is ignored. LP oscillator is disabled.

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.
2: TMR1GE bit must be set to use either $\overline{\text{T1G}}$ pin or C2OUT, as selected by the T1GSS bit of the CMCON1 register, as a Timer1 gate source.

8.1.1 ANALOG INPUT CONNECTION CONSIDERATIONS

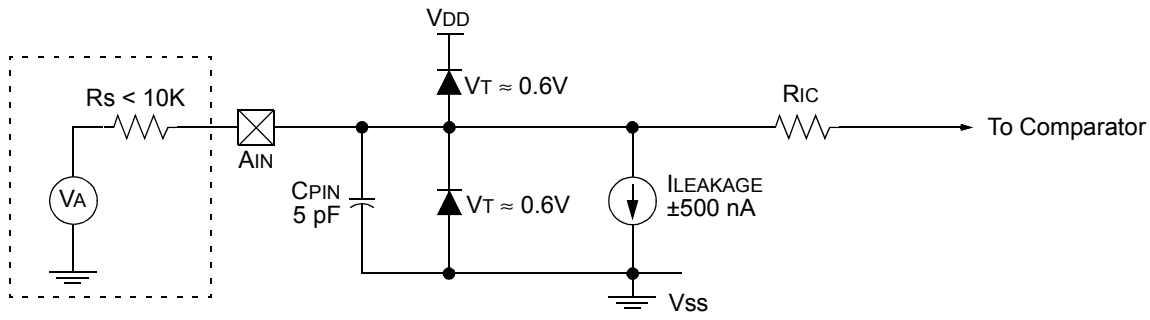
A simplified circuit for an analog input is shown in Figure 8-4. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 8-4: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage
VT = Threshold Voltage

TABLE 12-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	ADFM	VCFG1	VCFG0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	-000 ----
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
LCDCON	LCDEN	$\overline{\text{SLPEN}}$	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE0	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	0000 0000	0000 0000
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	0000 0000
LCDSE2(1)	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000	0000 0000
PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx xxxx	uuuu uuuu
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
PORTE	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx xxxx	uuuu uuuu
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 ----	1111 ----
TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for ADC module.

15.1 Capture Mode

In Capture mode, CCPRxH:CCPRxL captures the 16-bit value of the TMR1 register when an event occurs on pin CCPx. An event is defined as one of the following and is configured by the CCPxM<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

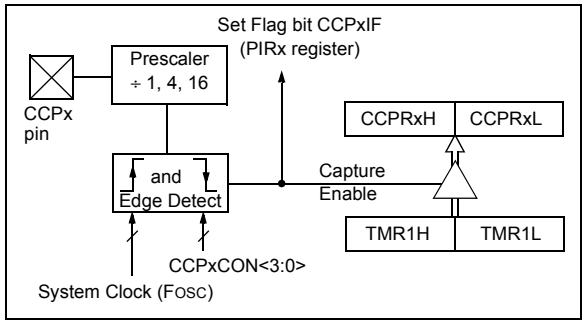
When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value (see Figure 15-1).

15.1.1 CCPx PIN CONFIGURATION

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 15-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



15.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

15.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIEx register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIRx register following any change in operating mode.

15.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCPxM<3:0> bits of the CCPxCON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler (see Example 15-1).

EXAMPLE 15-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
BANKSEL CCP1CON     ;Set Bank bits to point
                    ;to CCP1CON
CLRF    CCP1CON     ;Turn CCP module off
MOVLW   NEW_CAPT_PS ;Load the W reg with
                    ; the new prescaler
                    ; move value and CCP ON
MOVWF   CCP1CON     ;Load CCP1CON with this
                    ; value
```

16.2.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register selects one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit of the PCON register enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 16-1 for the Configuration Word definition.

If VDD falls below VBOR for greater than parameter (TBOR) (see **Section 19.0 "Electrical Specifications"**), the Brown-out situation will reset the device. This will occur regardless of VDD slew rate. A Reset is not insured to occur if VDD falls below VBOR for less than parameter (TBOR).

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 16-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional 64 ms.

Note: The Power-up Timer is enabled by the $\overline{\text{PWRTE}}$ bit in the Configuration Word.

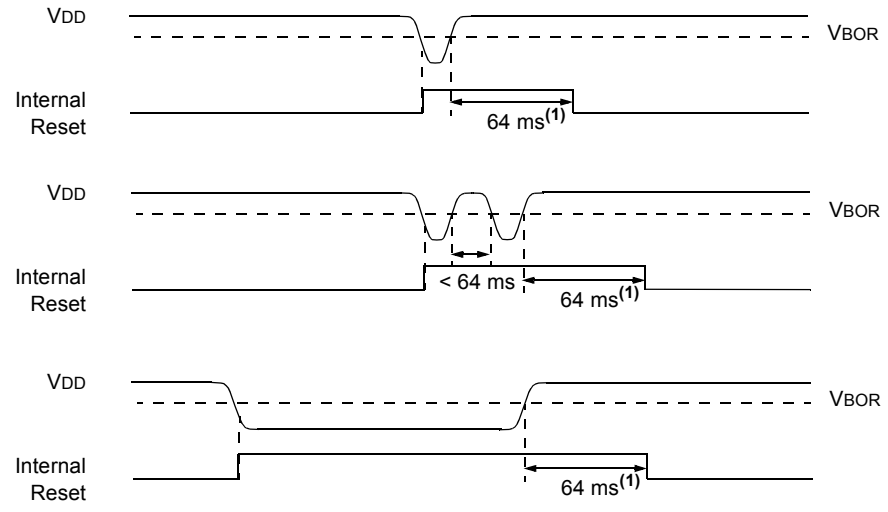
If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

16.2.5 BOR CALIBRATION

The PIC16F91X/946 stores the BOR calibration values in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the "*PIC16F91X/946 Memory Programming Specification*" (DS41244) and thus, does not require reprogramming.

Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F91X/946 Memory Programming Specification*" (DS41244) for more information.

FIGURE 16-3: BROWN-OUT SITUATIONS



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.

16.6 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP for verification purposes.

Note:	The entire data EEPROM and Flash program memory will be erased when the code protection is turned off. See the "*PIC16F91X/946 Memory Programming Specification*" (DS41244) for more information.

16.7 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

16.8 In-Circuit Serial Programming

The PIC16F91X/946 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for:

- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the RB7/ICSPDAT/ICDDAT/SEG13 and RB6/ICSPCLK/ICDCK/SEG14 pins low, while raising the $\overline{\text{MCLR}}$ (V_{PP}) pin from V_{IL} to V_{IHH}. See "*PIC16F91X/946 Memory Programming Specification*" (DS41244) for more information. RB7 becomes the programming data and the RB6 becomes the programming clock. Both RB7 and RB6 are Schmitt Trigger inputs in this mode.

After Reset, to place the device into Program/Verify mode, the Program Counter (PC) is at location 0000h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the "*PIC16F91X/946 Memory Programming Specification*" (DS41244).

A typical In-Circuit Serial Programming connection is shown in Figure 16-11.

FIGURE 16-11: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION

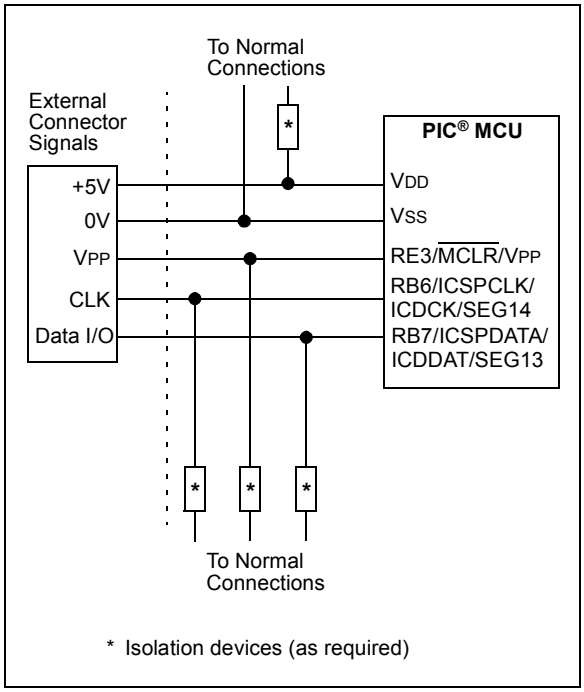


TABLE 19-8: PIC16F913/914/916/917/946 A/D CONVERTER (ADC) CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10 bits	bit	
AD02	EIL	Integral Error	—	—	±1	LSb	VREF = 5.12V
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.12V
AD04	EOFF	Offset Error	—	—	±1	LSb	VREF = 5.12V
AD07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.12V
AD06 AD06A	VREF	Reference Voltage(1)	2.2 2.7	—	VDD VDD	V	 Absolute minimum to ensure 1 LSb accuracy
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
AD09*	IREF	VREF Input Current(1)	10	—	1000	µA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
			—	—	50	µA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

FIGURE 20-8: MAXIMUM IDD vs. VDD (EXTRC MODE)

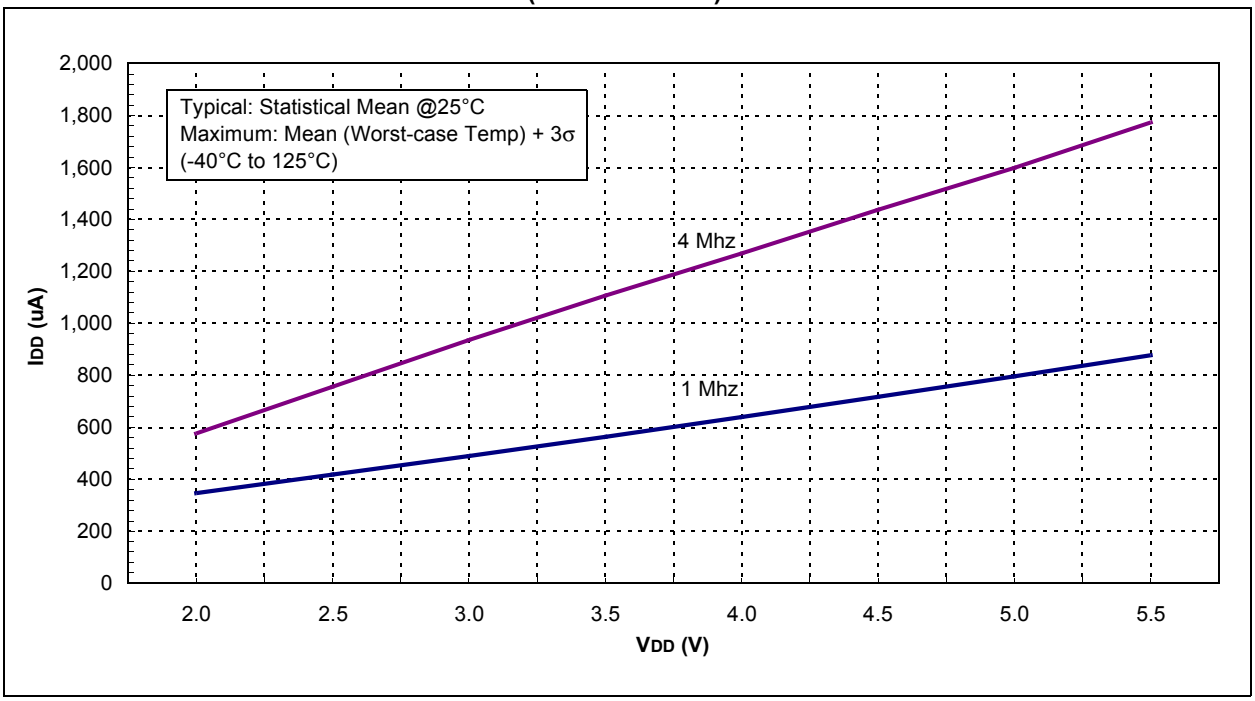


FIGURE 20-9: IDD vs. VDD OVER FOSC (LFINTOSC MODE, 31 kHz)

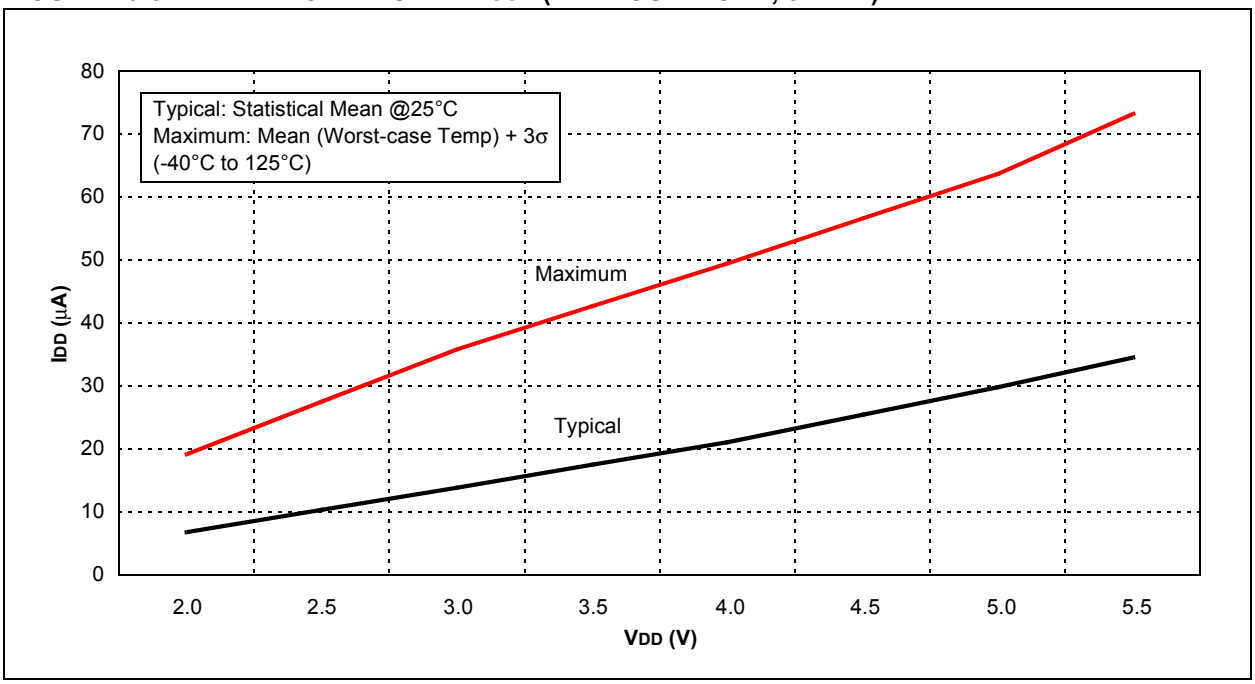


FIGURE 20-14: MAXIMUM IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

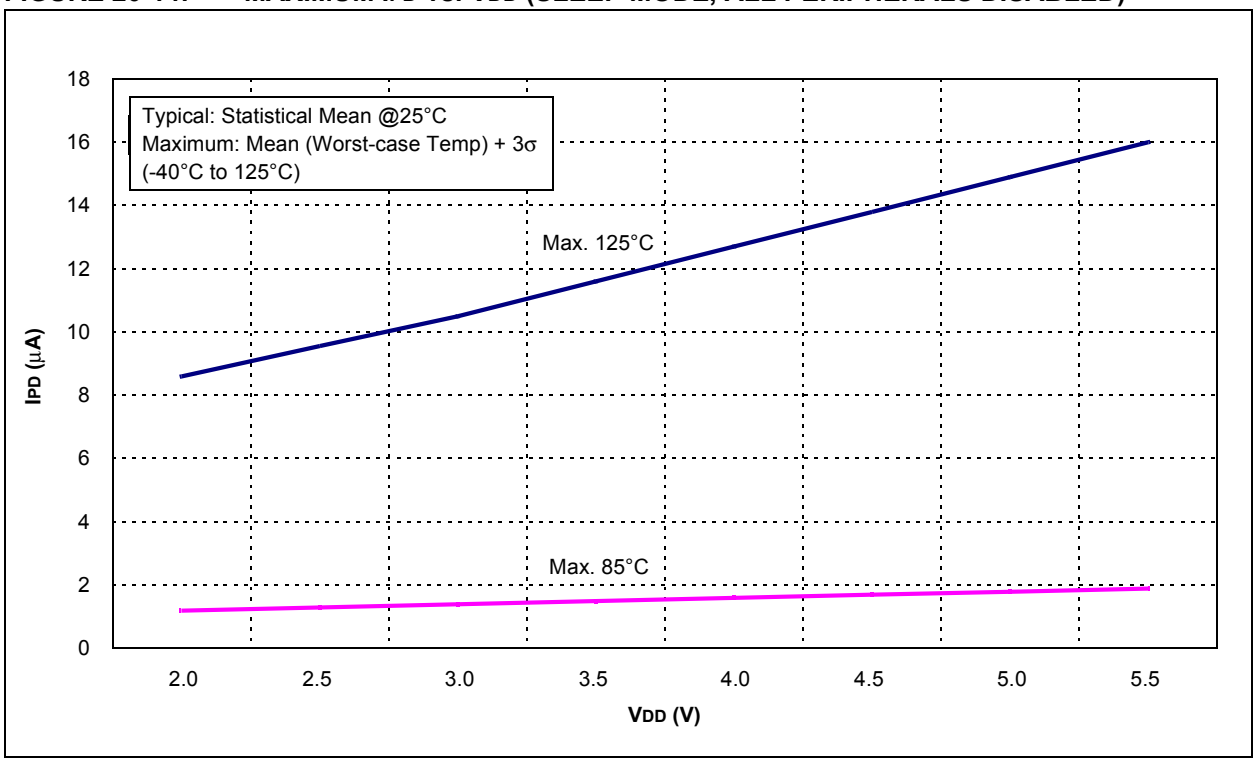


FIGURE 20-15: COMPARATOR IPD vs. VDD (BOTH COMPARATORS ENABLED)

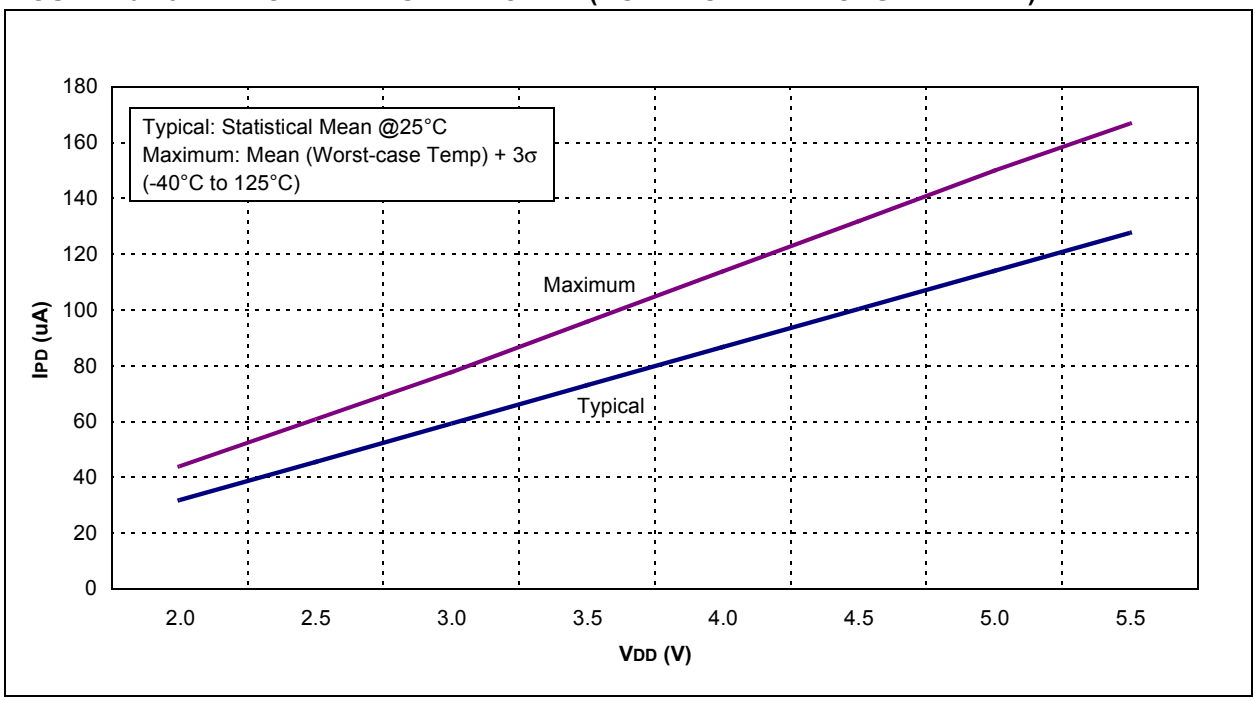


FIGURE 20-30: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

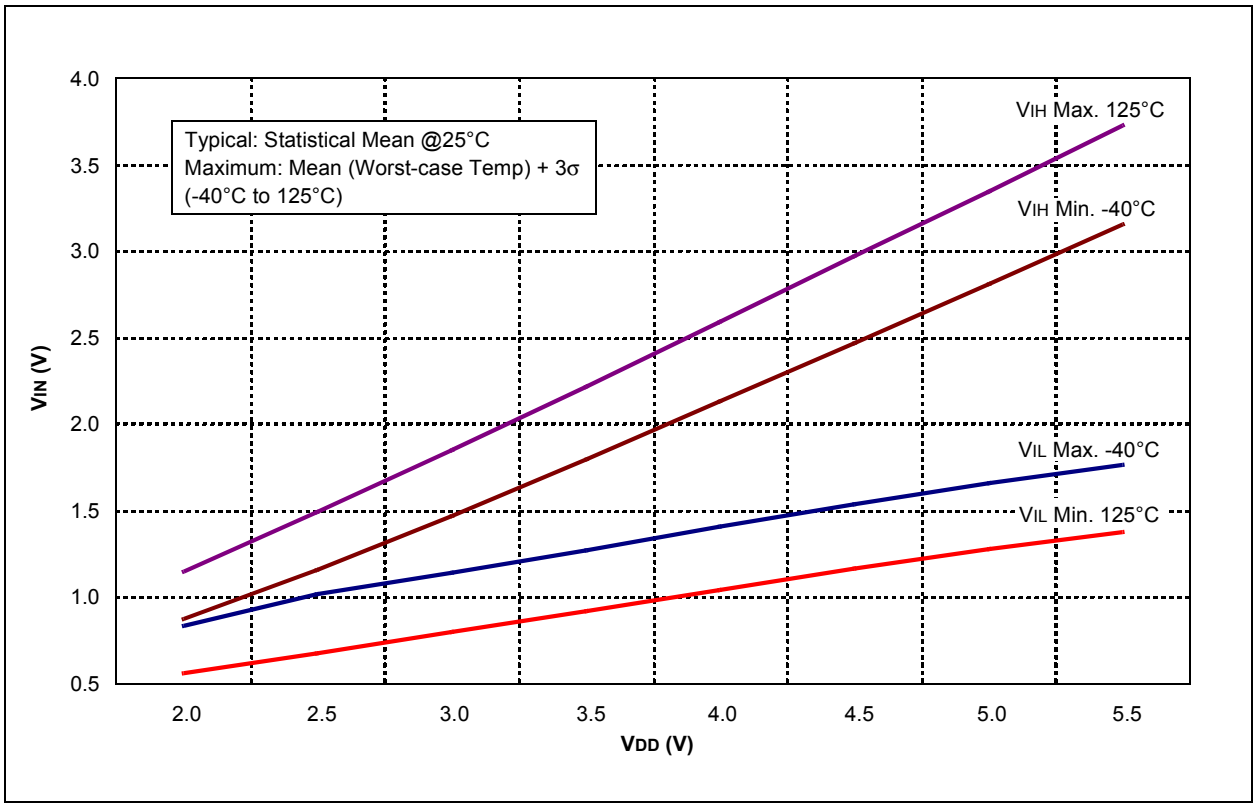
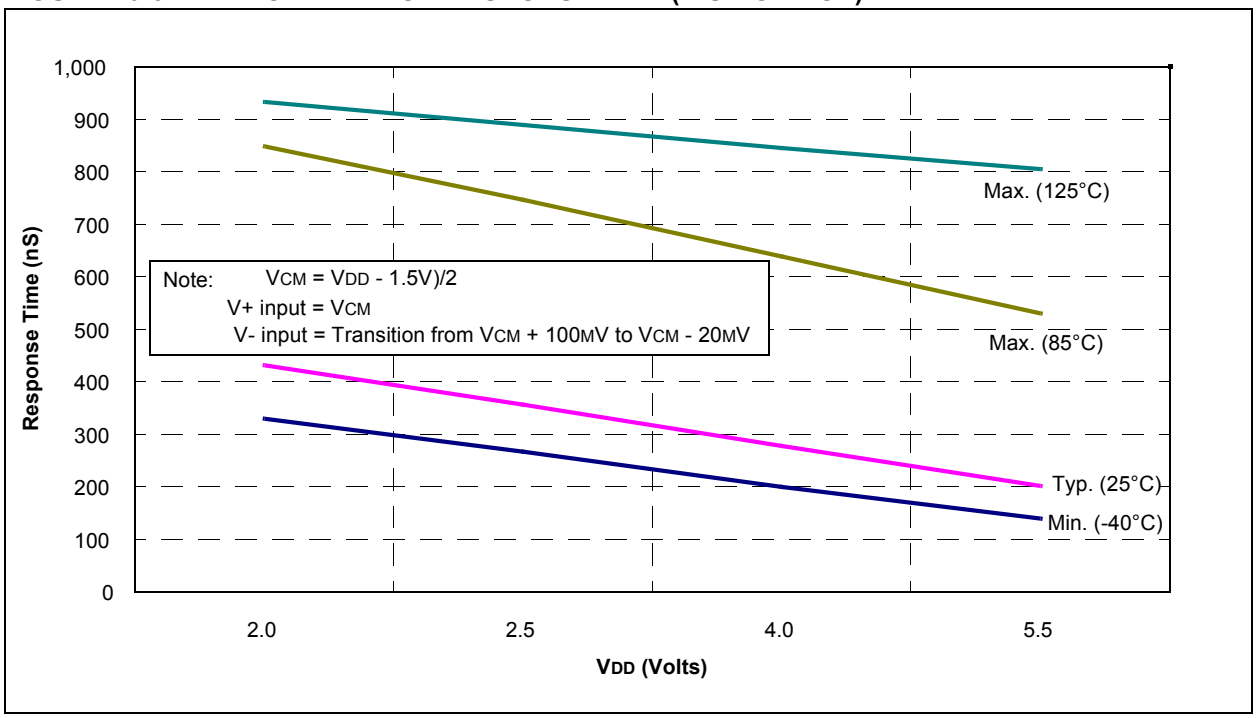
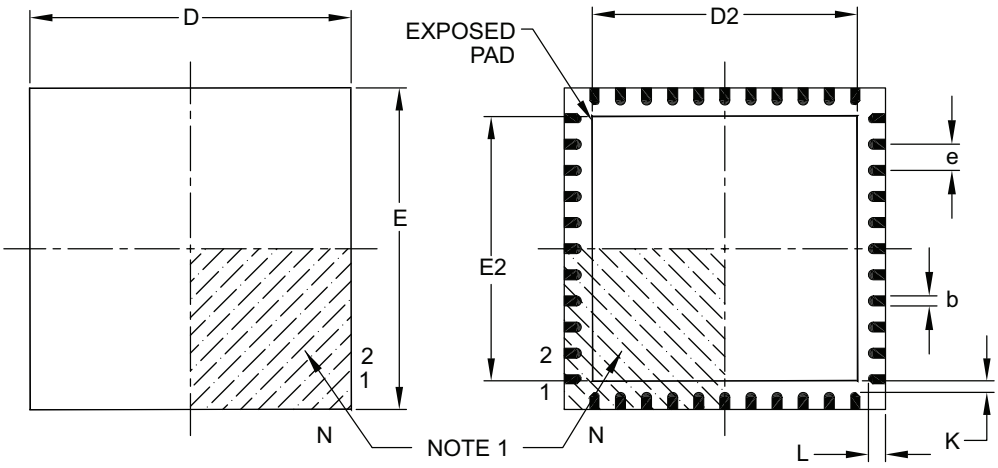


FIGURE 20-31: COMPARATOR RESPONSE TIME (RISING EDGE)

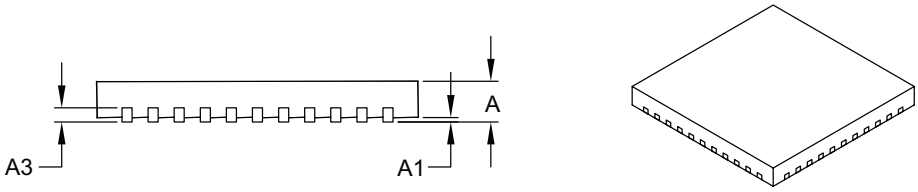


44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW **BOTTOM VIEW**



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B