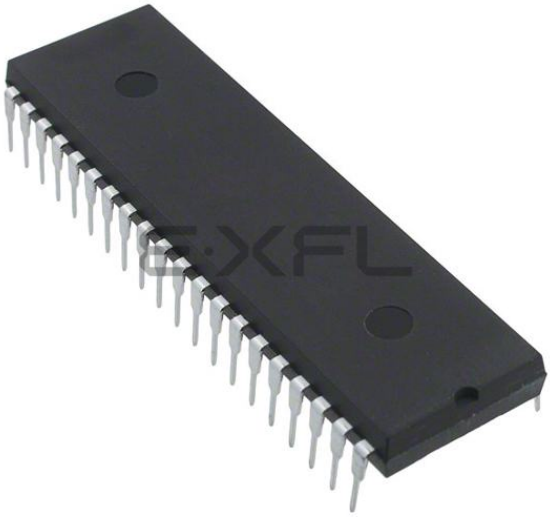

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f917-e-p

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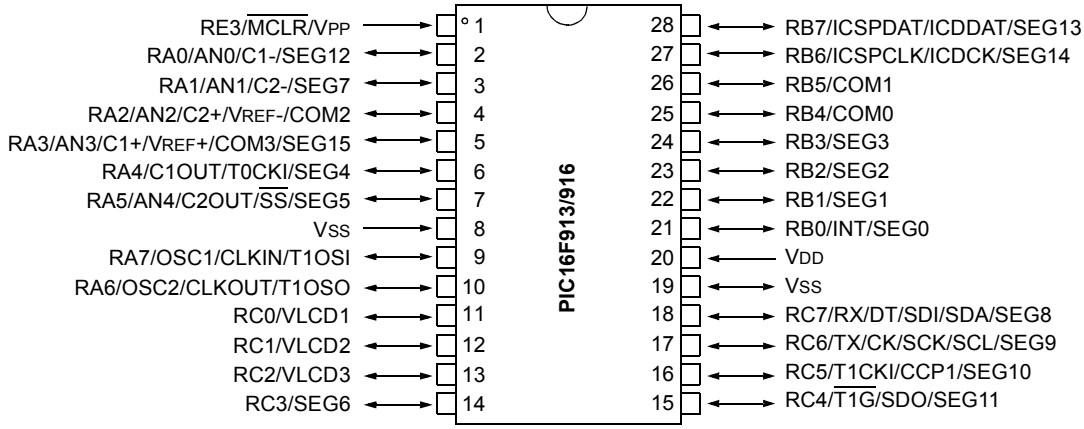
Pin Diagrams – PIC16F913/916, 28-Pin

28-pin PDIP, SOIC, SSOP



28-pin QFN

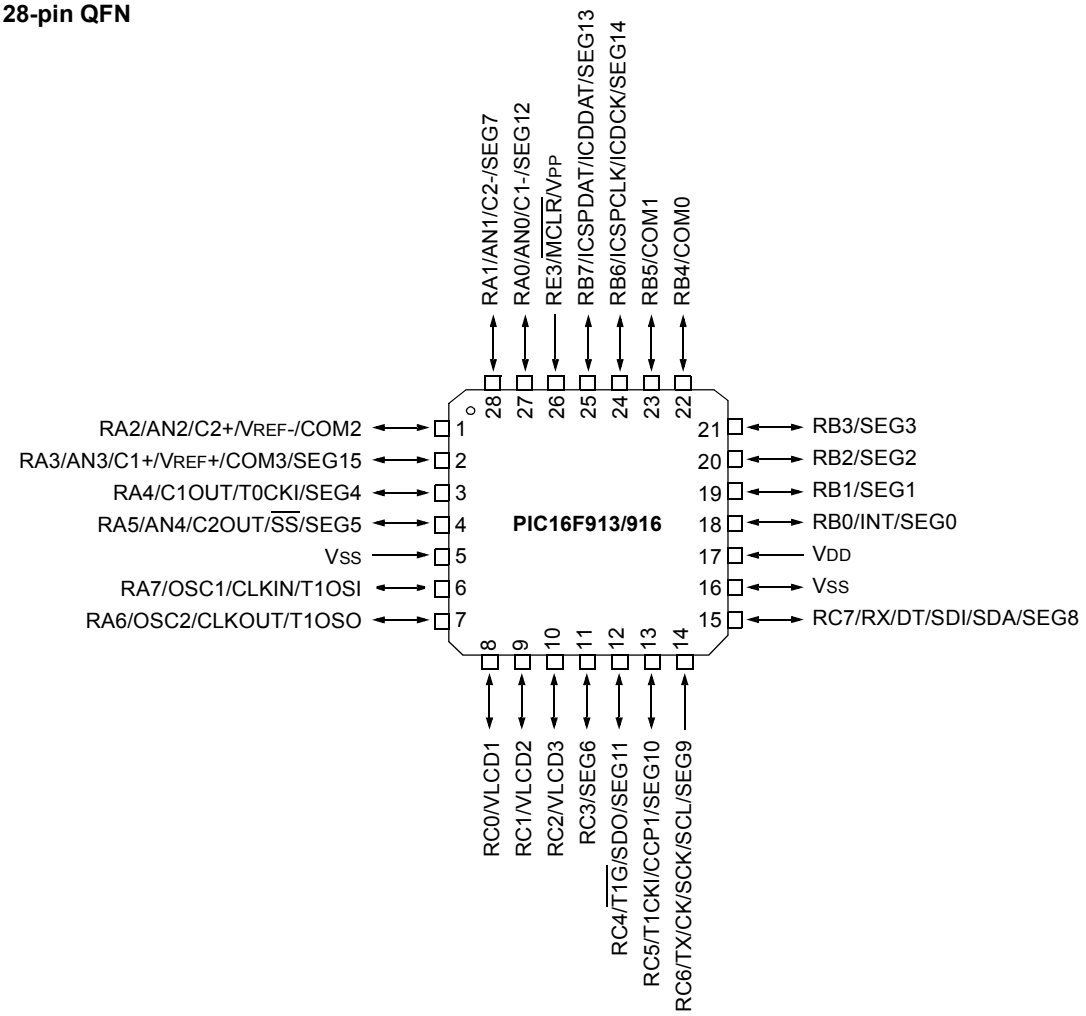


TABLE 2-3: PIC16F91X/946 SPECIAL FUNCTION REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 2											
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	41,226
101h	TMR0	Timer0 Module Register								xxxx xxxx	99,226
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	40,226
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	32,226
104h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	41,226
105h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	235,227
106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	54,226
107h	LCDCON	LCDEN	$\overline{SLPEN}$	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	145,227
108h	LCDPS	WFT	BIASMD	LCDA	WA	LP3	LP2	LP1	LP0	0000 0000	146,227
109h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -100	145,228
10Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	40,226
10Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	34,226
10Ch	EEDATL	EEDATL7	EEDATL6	EEDATL5	EEDATL4	EEDATL3	EEDATL2	EEDATL1	EEDATL0	0000 0000	188,228
10Dh	EEADRL	EEADRL7	EEADRL6	EEADRL5	EEADRL4	EEADRL3	EEADRL2	EEADRL1	EEADRL0	0000 0000	188,228
10Eh	EEDATH	—	—	EEDATH5	EEDATH4	EEDATH3	EEDATH2	EEDATH1	EEDATH0	--00 0000	188,228
10Fh	EEADRH	—	—	—	EEADRH4	EEADRH3	EEADRH2	EEADRH1	EEADRH0	---0 0000	188,228
110h	LCDDATA0	SEG7 COM0	SEG6 COM0	SEG5 COM0	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0	xxxx xxxx	147,228
111h	LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	SEG12 COM0	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0	xxxx xxxx	147,228
112h	LCDDATA2(2)	SEG23 COM0	SEG22 COM0	SEG21 COM0	SEG20 COM0	SEG19 COM0	SEG18 COM0	SEG17 COM0	SEG16 COM0	xxxx xxxx	147,228
113h	LCDDATA3	SEG7 COM1	SEG6 COM1	SEG5 COM1	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1	xxxx xxxx	147,228
114h	LCDDATA4	SEG15 COM1	SEG14 COM1	SEG13 COM1	SEG12 COM1	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1	xxxx xxxx	147,228
115h	LCDDATA5(2)	SEG23 COM1	SEG22 COM1	SEG21 COM1	SEG20 COM1	SEG19 COM1	SEG18 COM1	SEG17 COM1	SEG16 COM1	xxxx xxxx	147,228
116h	LCDDATA6	SEG7 COM2	SEG6 COM2	SEG5 COM2	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2	xxxx xxxx	147,228
117h	LCDDATA7	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2	xxxx xxxx	147,228
118h	LCDDATA8(2)	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2	xxxx xxxx	147,228
119h	LCDDATA9	SEG7 COM3	SEG6 COM3	SEG5 COM3	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3	xxxx xxxx	147,228
11Ah	LCDDATA10	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3	xxxx xxxx	147,228
11Bh	LCDDATA11(2)	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3	xxxx xxxx	147,228
11Ch	LCDSE0(3)	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	0000 0000	147,228
11Dh	LCDSE1(3)	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	147,228
11Eh	LCDSE2(2,3)	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000	147,228
11Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: PIC16F914/917 and PIC16F946 only.

3: This register is only initialized by a POR or BOR reset and is unchanged by other Resets.

2.2.2.8 PCON Register

The Power Control (PCON) register contains flag bits (see Table 16-2) to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the software enable of the BOR.

The PCON register bits are shown in Register 2-8.

REGISTER 2-8: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	R/W-1	U-0	U-0	R/W-0	R/W-x
—	—	—	SBOREN	—	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **SBOREN:** Software BOR Enable bit(1)
- 1 = BOR enabled
- 0 = BOR disabled

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
- 1 = No Power-on Reset occurred
- 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
- 1 = No Brown-out Reset occurred
- 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

Note 1: Set BOREN<1:0> = 01 in the Configuration Word register for this bit to control the $\overline{BOR}$.

8.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparators are very useful mixed signal building blocks because they provide analog functionality independent of the program execution. The Analog Comparator module includes the following features:

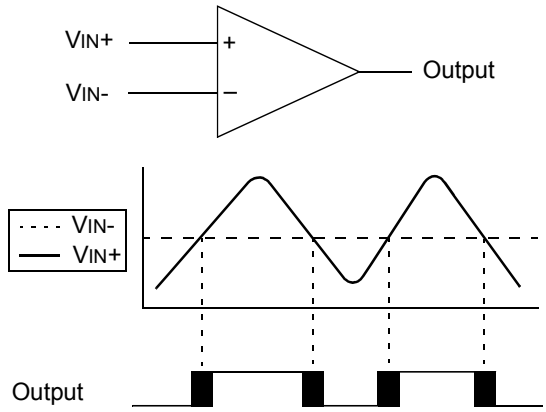
- Dual comparators
- Multiple comparator configurations
- Comparator outputs are available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- Programmable voltage reference

Note:	Only Comparator C2 can be linked to Timer1.

8.1 Comparator Overview

A comparator is shown in Figure 8-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

FIGURE 8-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

This device contains two comparators as shown in Figure 8-2 and Figure 8-3. The comparators are not independently configurable.

REGISTER 10-1: LCDCON: LIQUID CRYSTAL DISPLAY CONTROL REGISTER

R/W-0	R/W-0	R/C-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
LCDEN	$\overline{\text{SLPEN}}$	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
C = Only clearable bit	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
-n = Value at POR			

bit 7 **LCDEN:** LCD Driver Enable bit
1 = LCD driver module is enabled
0 = LCD driver module is disabled

bit 6 **$\overline{\text{SLPEN}}$:** LCD Driver Enable in Sleep mode bit
1 = LCD driver module is disabled in Sleep mode
0 = LCD driver module is enabled in Sleep mode

bit 5 **WERR:** LCD Write Failed Error bit
1 = LCDDATAx register written while the WA bit of the LCDPS register = 0 (must be cleared in software)
0 = No LCD write error

bit 4 **VLCDEN:** LCD Bias Voltage Pins Enable bit
1 = VLCD pins are enabled
0 = VLCD pins are disabled

bit 3-2 **CS<1:0>:** Clock Source Select bits
00 = FOSC/8192
01 = T1OSC (Timer1)/32
1x = LFINTOSC (31 kHz)/32

bit 1-0 **LMUX<1:0>:** Commons Select bits

LMUX<1:0>	Multiplex	Maximum Number of Pixels			Bias
		PIC16F913/916	PIC16F914/917	PIC16F946	
00	Static (COM0)	16	24	42	Static
01	1/2 (COM<1:0>)	32	48	84	1/2 or 1/3
10	1/3 (COM<2:0>)	48	72	126	1/2 or 1/3
11	1/4 (COM<3:0>)	60(1)	96	168	1/3

Note 1: On PIC16F913/916 devices, COM3 and SEG15 are shared on one pin, limiting the device from driving 64 pixels.

FIGURE 13-1: FLASH PROGRAM MEMORY READ CYCLE EXECUTION

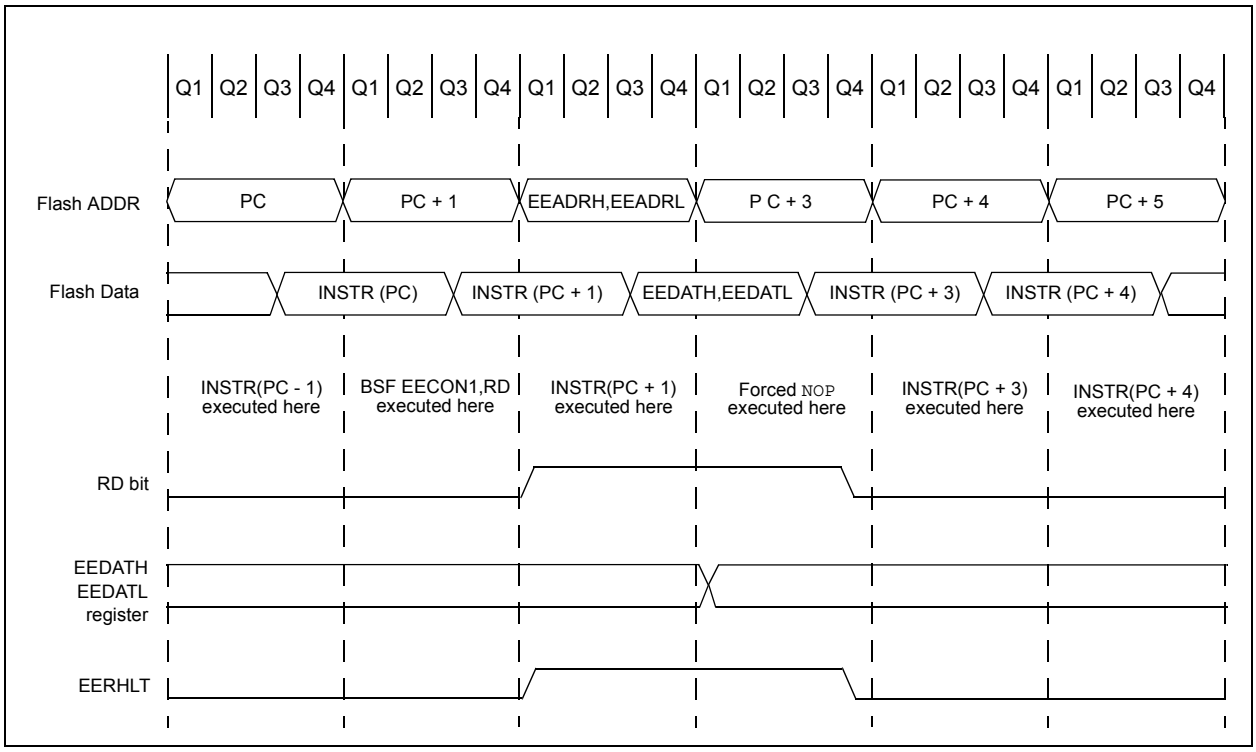


TABLE 13-1: SUMMARY OF ASSOCIATED REGISTERS WITH DATA EEPROM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
EEADRH	—	—	—	EEADRH4	EEADRH3	EEADRH2	EEADRH1	EEADRH0	---0 0000	---0 0000
EEADRL	EEADRL7	EEADRL6	EEADRL5	EEADRL4	EEADRL3	EEADRL2	EEADRL1	EEADRL0	0000 0000	0000 0000
EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	0--- x000	---- q000
EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
EEDATH	—	—	EEDATH5	EEDATH4	EEDATH3	EEDATH2	EEDATH1	EEDATH0	--00 0000	--00 0000
EEDATL	EEDATL7	EEDATL6	EEDATL5	EEDATL4	EEDATL3	EEDATL2	EEDATL1	EEDATL0	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition.
Shaded cells are not used by data EEPROM module.

REGISTER 14-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3(2)	SSPM2(2)	SSPM1(2)	SSPM0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WCOL**: Write Collision Detect bit
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6 **SSPOV**: Receive Overflow Indicator bit
In SPI mode:
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
0 = No overflow
In I^2C™ mode:
1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode. SSPOV must be cleared in software in either mode.
0 = No overflow

bit 5 **SSPEN**: Synchronous Serial Port Enable bit
In SPI mode:
1 = Enables serial port and configures SCK, SDO and SDI as serial port pins
0 = Disables serial port and configures these pins as I/O port pins
In I^2C mode:
1 = Enables the serial port and configures the SDA and SCL pins as serial port pins
0 = Disables serial port and configures these pins as I/O port pins
In both modes, when enabled, these pins must be properly configured as input or output.

bit 4 **CKP**: Clock Polarity Select bit
In SPI mode:
1 = Idle state for clock is a high level (Microwire default)
0 = Idle state for clock is a low level (Microwire alternate)
In I^2C mode:
SCK release control
1 = Enable clock
0 = Holds clock low (clock stretch). (Used to ensure data setup time.)

bit 3-0 **SSPM<3:0>**: Synchronous Serial Port Mode Select bits
0000 = SPI Master mode, clock = FOSC/4
0001 = SPI Master mode, clock = FOSC/16
0010 = SPI Master mode, clock = FOSC/64
0011 = SPI Master mode, clock = TMR2 output/2
0100 = SPI Slave mode, clock = SCK pin. $\overline{SS}$ pin control enabled.
0101 = SPI Slave mode, clock = SCK pin. $\overline{SS}$ pin control disabled. $\overline{SS}$ can be used as I/O pin.
0110 = I^2C Slave mode, 7-bit address
0111 = I^2C Slave mode, 10-bit address
1000 = Reserved
1001 = Reserved
1010 = Reserved
1011 = I^2C Firmware Controlled Master mode (slave IDLE)
1100 = Reserved
1101 = Reserved
1110 = I^2C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1111 = I^2C Slave mode, 10-bit address with Start and Stop bit interrupts enabled

NOTES:

16.0 SPECIAL FEATURES OF THE CPU

The PIC16F91X/946 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving features and offer code protection.

These features are:

- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator Selection
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™

The PIC16F91X/946 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions-on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost, while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 16-1).

TABLE 16-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset	• $\overline{\text{MCLR}}$ Reset • WDT Reset • Brown-out Reset(1)	• Wake-up from Sleep through interrupt • Wake-up from Sleep through WDT time-out
LVDCON	109h	--00 -100	--00 -100	--uu -uuu
EEDATL	10Ch	0000 0000	0000 0000	uuuu uuuu
EEADRL	10Dh	0000 0000	0000 0000	uuuu uuuu
EEDATH	10Eh	--00 0000	0000 0000	uuuu uuuu
EEADRH	10Fh	---0 0000	0000 0000	uuuu uuuu
LCDDATA0	110h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA1	111h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA2(6)	112h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA3	113h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA4	114h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA5(6)	115h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA6	116h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA7	117h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA8(6)	118h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA9	119h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA10	11Ah	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA11(6)	11Bh	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDSE0	11Ch	0000 0000	uuuu uuuu	uuuu uuuu
LCDSE1	11Dh	0000 0000	uuuu uuuu	uuuu uuuu
LCDSE2(6)	11Eh	0000 0000	uuuu uuuu	uuuu uuuu
TRISF(7)	185h	1111 1111	1111 1111	uuuu uuuu
TRISG(7)	187h	--11 1111	--11 1111	--uu uuuu
PORTF(7)	188h	xxxx xxxx	0000 0000	uuuu uuuu
PORTG(7)	189h	--xx xxxx	--00 0000	--uu uuuu
LCDDATA12(7)	190h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA13(7)	191h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA14(7)	192h	---- --xx	---- --uu	---- --uu
LCDDATA15(7)	193h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA16(7)	194h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA17(7)	195h	---- --xx	---- --uu	---- --uu
LCDDATA18(7)	196h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA19(7)	197h	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA20(7)	198h	---- --xx	---- --uu	---- --uu
LCDDATA21(7)	199h	xxxx xxxx	uuuu uuuu	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 16-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: PIC16F914/917 and PIC16F946 only.

7: PIC16F946 only.

16.9 In-Circuit Debugger

When the debug bit in the Configuration Word register is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB® ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. See Table 16-9 for more detail.

Note: The user's application must have the circuitry required to support ICD functionality. Once the ICD circuitry is enabled, normal device pin functions on RB6/ICSPCLK/ICDCK/SEG14 and RB7/ICSPDAT/ICDDAT/SEG13 will not be usable. The ICD circuitry uses these pins for communication with the ICD2 external debugger.

For more information, see "*Using MPLAB® ICD 2*" (DS51265), available on Microchip's web site (www.microchip.com).

16.9.1 ICD PINOUT

The devices in the PIC16F91X/946 family carry the circuitry for the In-Circuit Debugger on-chip and on existing device pins. This eliminates the need for a separate die or package for the ICD device. The pinout for the ICD device is the same as the devices (see **Section 1.0 "Device Overview"** for complete pinout and pin descriptions). Table 16-9 shows the location and function of the ICD related pins on the 28 and 40-pin devices.

TABLE 16-9: PIC16F91X/946-ICD PIN DESCRIPTIONS

Pin Numbers			Name	Type	Pull-up	Description
PDIP		TQFP				
PIC16F914/917	PIC16F913/916	PIC16F946				
40	28	24	ICDDATA	TTL	—	In Circuit Debugger Bidirectional data
39	27	23	ICDCLK	ST	—	In Circuit Debugger Bidirectional clock
1	1	36	$\overline{MCLR}$/VPP	HV	—	Programming voltage
11,32	20	10, 19, 38, 51	VDD	P	—	Power
12,31	8,19	9, 20, 41, 56	VSS	P	—	Ground
—	—	26	AVDD	P	—	Analog power
—	—	25	AVSS	P	—	Analog ground

Legend: TTL = TTL input buffer, ST = Schmitt Trigger input buffer, P = Power, HV = High Voltage

TABLE 19-8: PIC16F913/914/916/917/946 A/D CONVERTER (ADC) CHARACTERISTICS

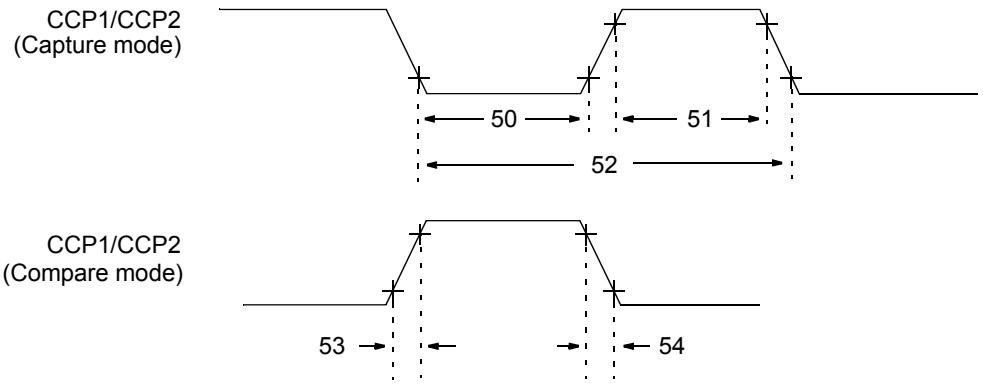
Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10 bits	bit	
AD02	EIL	Integral Error	—	—	±1	LSb	VREF = 5.12V
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.12V
AD04	EOFF	Offset Error	—	—	±1	LSb	VREF = 5.12V
AD07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.12V
AD06 AD06A	VREF	Reference Voltage(1)	2.2 2.7	—	VDD VDD	V	 Absolute minimum to ensure 1 LSb accuracy
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
AD09*	IREF	VREF Input Current(1)	10	—	1000	µA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
			—	—	50	µA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

FIGURE 19-13: CAPTURE/COMPARE/PWM TIMINGS



Note: Refer to Figure 19-3 for load conditions.

TABLE 19-12: CAPTURE/COMPARE/PWM (CCP) REQUIREMENTS

Param. No.	Sym.	Characteristic			Min.	Typ†	Max.	Units	Conditions
50*	TccL	CCPx input low time	No Prescaler		0.5TCY + 5	—	—	ns	
			With Prescaler	3.0-5.5V	10	—	—	ns	
				2.0-5.5V	20	—	—	ns	
51*	TccH	CCPx input high time	No Prescaler		0.5TCY + 5	—	—	ns	
			With Prescaler	3.0-5.5V	10	—	—	ns	
				2.0-5.5V	20	—	—	ns	
52*	TccP	CCPx input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCPx output fall time		3.0-5.5V	—	10	25	ns	
				2.0-5.5V	—	25	50	ns	
54*	TccF	CCPx output fall time		3.0-5.5V	—	10	25	ns	
				2.0-5.5V	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 19-13: PIC16F913/914/916/917/946 PLVD CHARACTERISTICS:

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C Operating Voltage VDD Range 2.0V-5.5V					
Sym.	**Characteristic**		**Min.**	**Typ†**	**Max. (85°C)**	**Max. (125°C)**	**Units**	**Conditions**
VPLVD	PLVD Voltage	LVDL<2:0> = 001	1.900	2.0	2.100	2.125	V	
		LVDL<2:0> = 010	2.000	2.1	2.200	2.225	V	
		LVDL<2:0> = 011	2.100	2.2	2.300	2.325	V	
		LVDL<2:0> = 100	2.200	2.3	2.400	2.425	V	
		LVDL<2:0> = 101	3.825	4.0	4.175	4.200	V	
		LVDL<2:0> = 110	4.025	4.2	4.375	4.400	V	
		LVDL<2:0> = 111	4.425	4.5	4.675	4.700	V	
*TPLVDS	PLVD Settling time		—	50 25	—	—	µs	VDD = 5.0V VDD = 3.0V

* These parameters are characterized but not tested

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

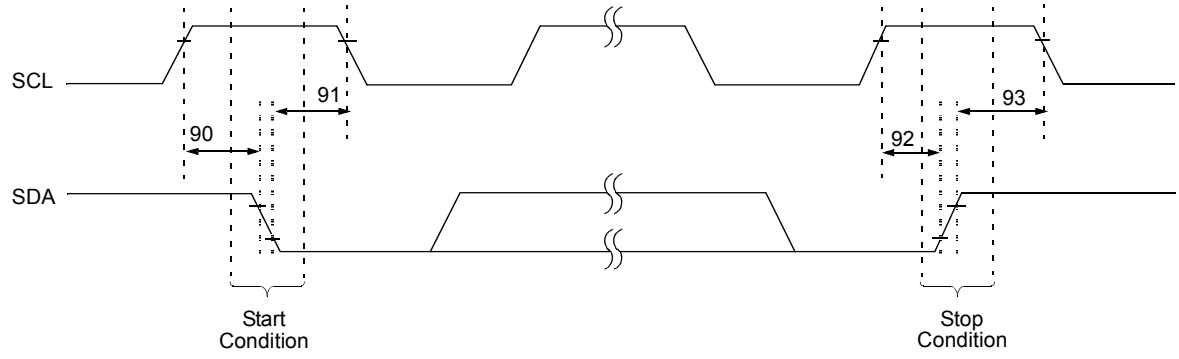
TABLE 19-14: SPI MODE REQUIREMENTS

Param No.	Symbol	Characteristic		Min.	Typ†	Max.	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ input		Tcy	—	—	ns	
71*	TscH	SCK input high time (Slave mode)		Tcy + 20	—	—	ns	
72*	TscL	SCK input low time (Slave mode)		Tcy + 20	—	—	ns	
73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75*	TdoR	SDO data output rise time	3.0-5.5V	—	10	25	ns	
			2.0-5.5V	—	25	50	ns	
76*	TdoF	SDO data output fall time		—	10	25	ns	
77*	TssH2doZ	$\overline{SS}\uparrow$ to SDO output high-impedance		10	—	50	ns	
78*	TscR	SCK output rise time (Master mode)	3.0-5.5V	—	10	25	ns	
			2.0-5.5V	—	25	50	ns	
79*	TscF	SCK output fall time (Master mode)		—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	3.0-5.5V	—	—	50	ns	
			2.0-5.5V	—	—	145	ns	
81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge		Tcy	—	—	ns	
82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge		—	—	50	ns	
83*	TscH2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge		1.5Tcy + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-18: I^2C™ BUS START/STOP BITS TIMING



Note: Refer to Figure 19-3 for load conditions.

FIGURE 20-30: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

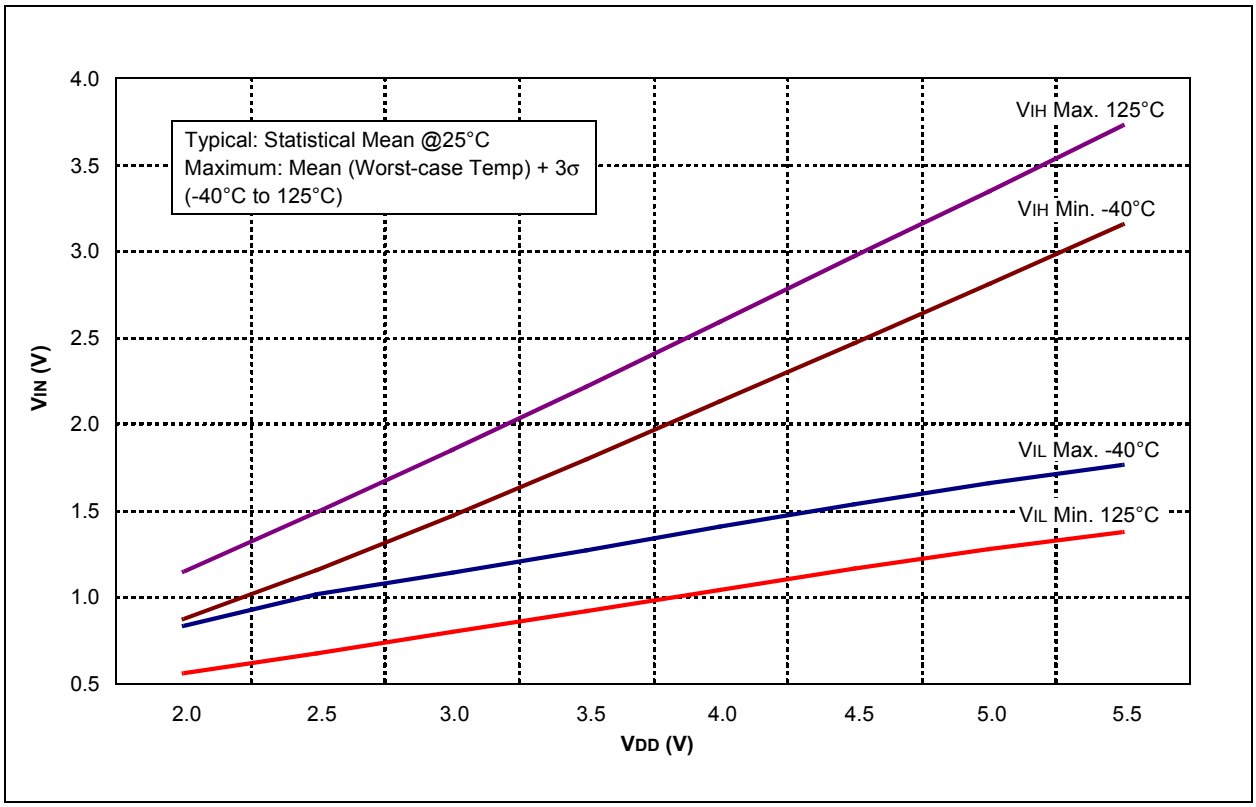


FIGURE 20-31: COMPARATOR RESPONSE TIME (RISING EDGE)

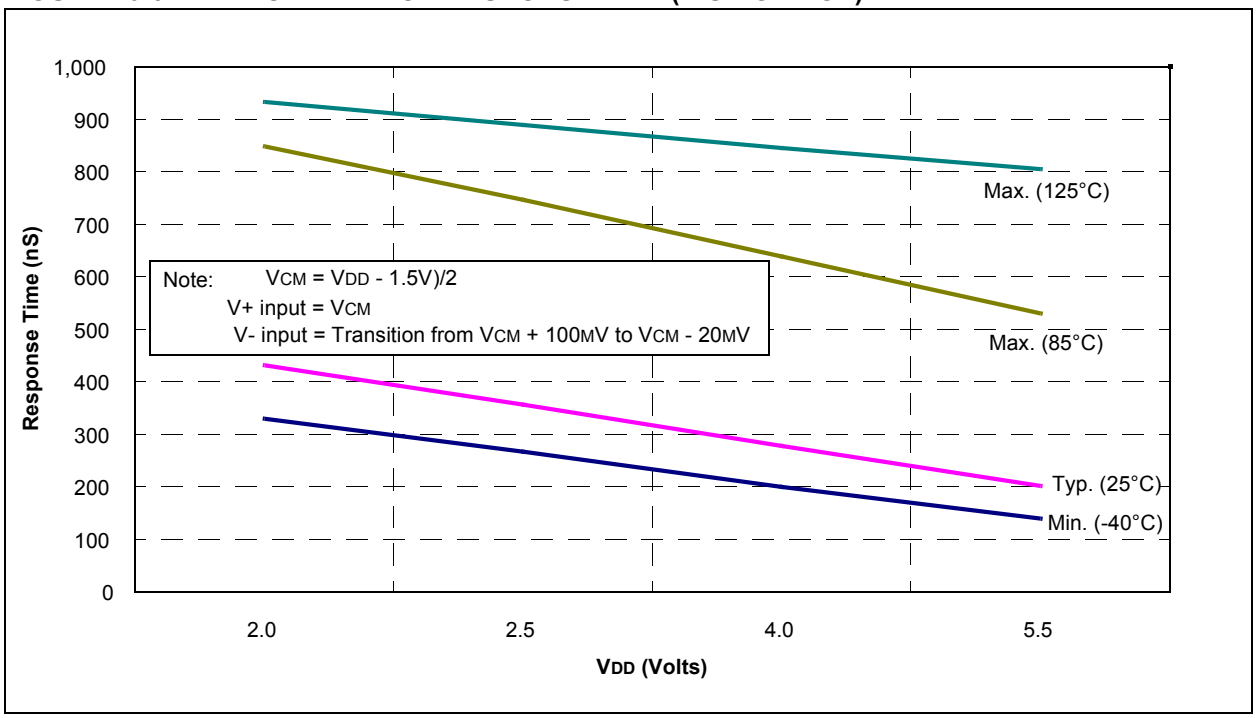


FIGURE 20-34: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE

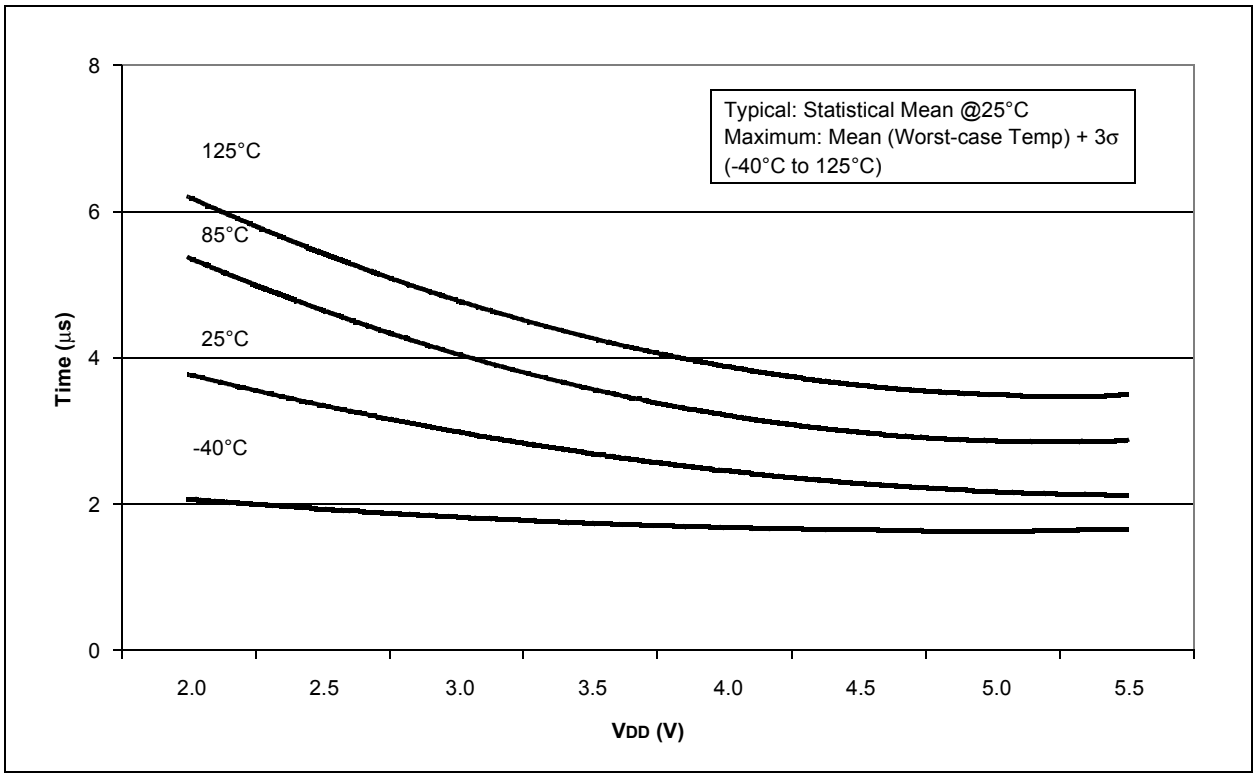
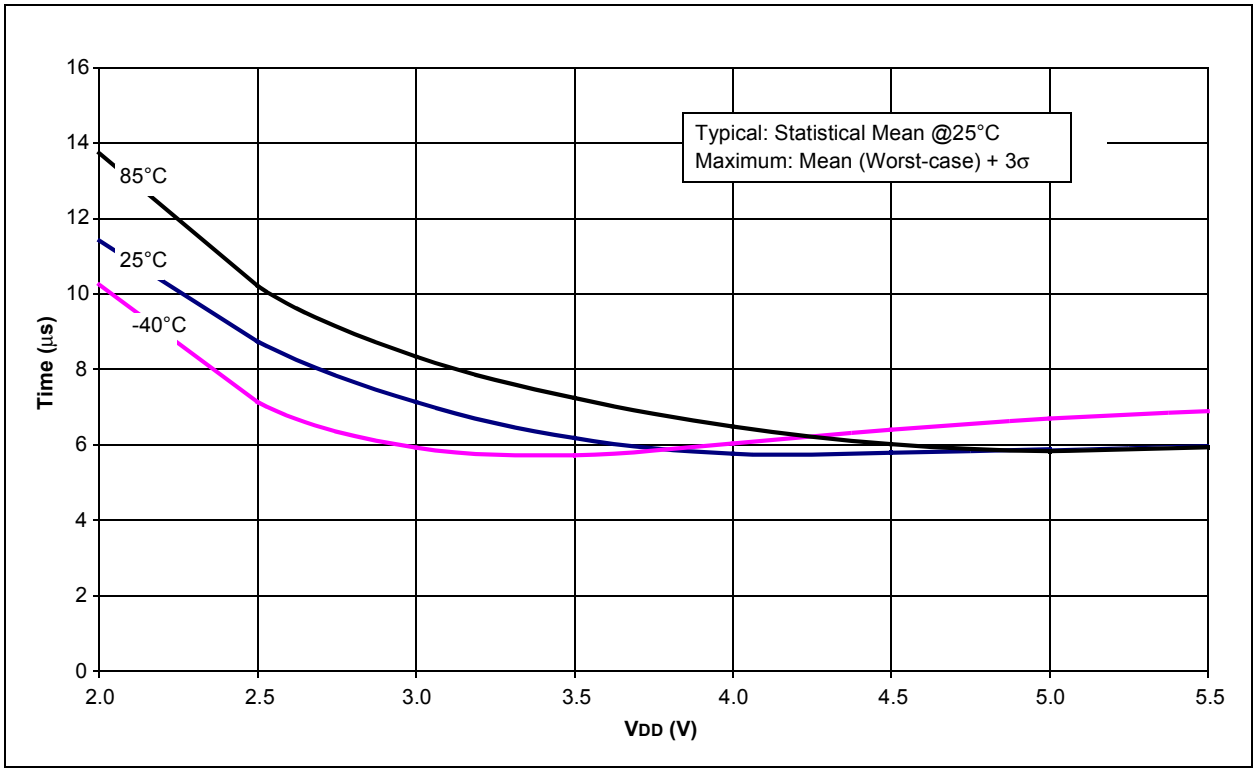


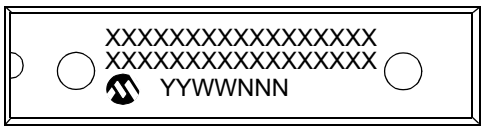
FIGURE 20-35: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE



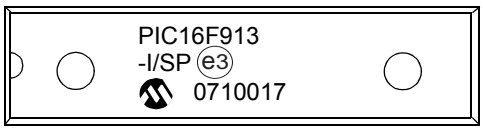
21.0 PACKAGING INFORMATION

21.1 Package Marking Information

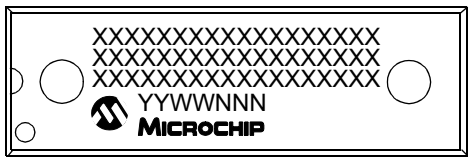
28-Lead SPDIP



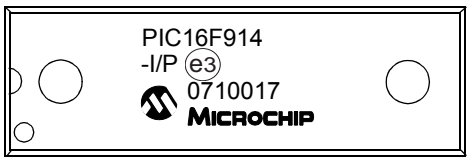
Example



40-Lead PDIP



Example



28-Lead QFN

Example

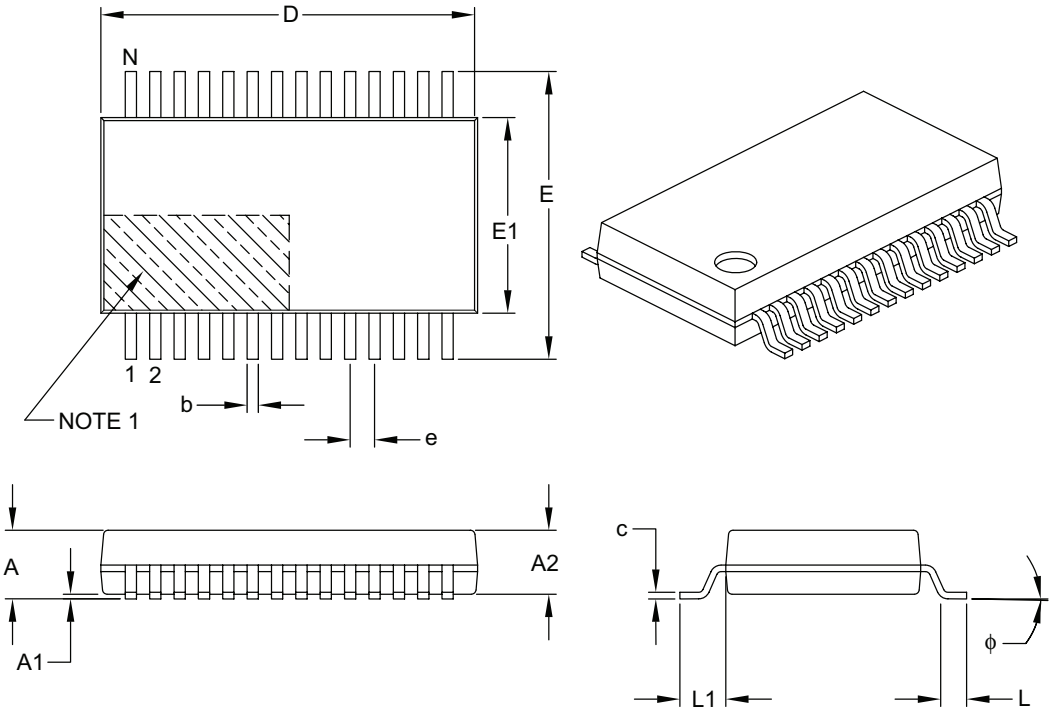
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard PIC® device marking consists of Microchip part number, year code, week code and traceability code. For PIC® device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B