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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f917-e-pt

PIC16F913/914/916/917/946

2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers (GPRs) and the Special Function Registers (SFRs). Bits RP0 and RP1 are bank select bits.

<u>RP1</u>	<u>RP0</u>	
0	0	→ Bank 0 is selected
0	1	→ Bank 1 is selected
1	0	→ Bank 2 is selected
1	1	→ Bank 3 is selected

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in another bank for code reduction and quicker access.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 256 x 8 bits in the PIC16F913/914, 352 x 8 bits in the PIC16F916/917 and 336 x 8 bits in the PIC16F946. Each register is accessed either directly or indirectly through the File Select Register (FSR) (see **Section 2.5 “Indirect Addressing, INDF and FSR Registers”**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Tables 2-1, 2-2, 2-3 and 2-4). These registers are static RAM.

The Special Function Registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

3.5.1.4 RC3/SEG6

Figure 3-17 shows the diagram for this pin. The RC3 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog output for the LCD

FIGURE 3-17: BLOCK DIAGRAM OF RC3

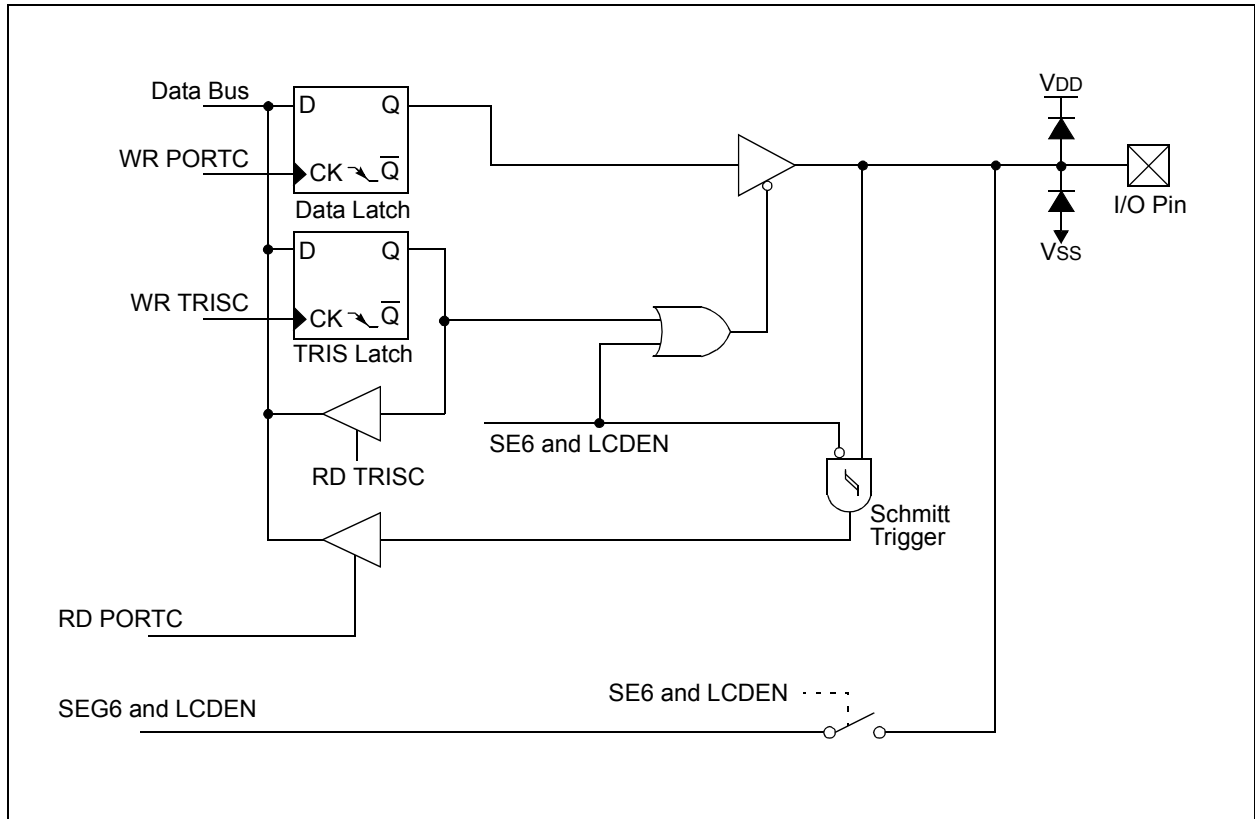


FIGURE 3-28: BLOCK DIAGRAM OF RE<7:4> (PIC16F946 ONLY)

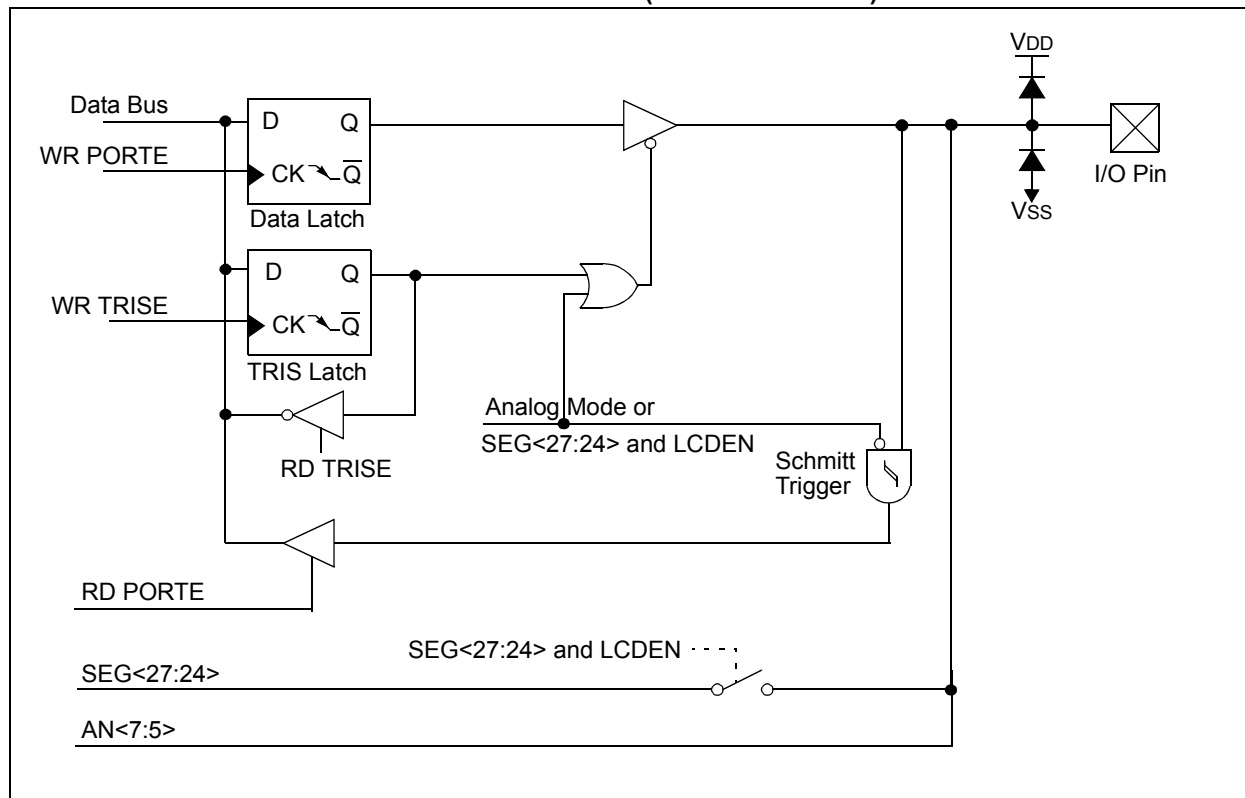


FIGURE 8-8: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

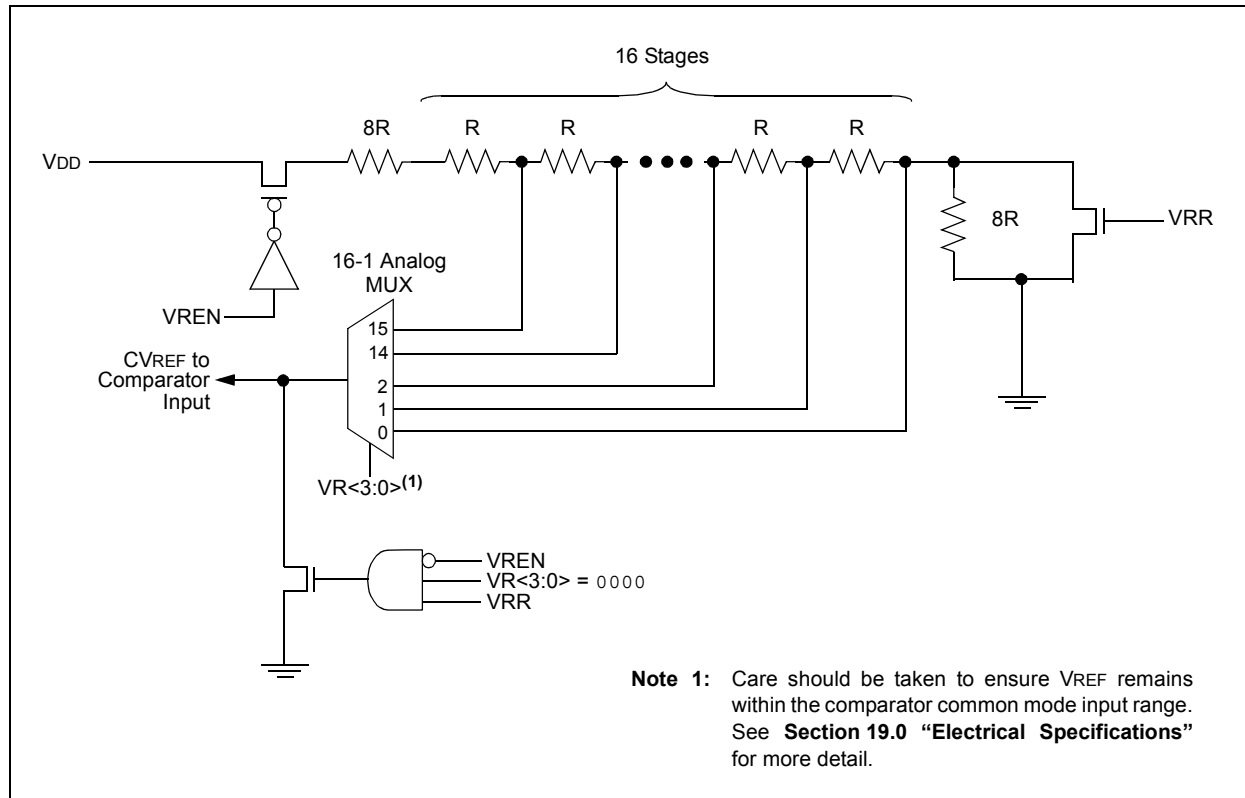


TABLE 8-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
CMCON1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE2	OSFIE	C2IE	C1IE	LCDIE	—	LVDIE	—	CCP2IE	0000 -0-0	0000 -0-0
PIR2	OSFIF	C2IF	C1IF	LCDIF	—	LVDIF	—	CCP2IF	0000 -0-0	0000 -0-0
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx xxxx	uuuu uuuu
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111
VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

PIC16F913/914/916/917/946

TABLE 9-1: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
LCDCON	LCDEN	SLPEN	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	0000 0000
PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Asynchronous Transmission.

PIC16F913/914/916/917/946

9.2 AUSART Baud Rate Generator (BRG)

The Baud Rate Generator (BRG) is an 8-bit timer that is dedicated to the support of both the asynchronous and synchronous AUSART operation.

The SPBRG register determines the period of the free running baud rate timer. In Asynchronous mode the multiplier of the baud rate period is determined by the BRGH bit of the TXSTA register. In Synchronous mode, the BRGH bit is ignored.

Table 9-3 contains the formulas for determining the baud rate. Example 9-1 provides a sample calculation for determining the baud rate and baud rate error.

Typical baud rates and error values for various asynchronous modes have been computed for your convenience and are shown in Table 9-3. It may be advantageous to use the high baud rate (BRGH = 1), to reduce the baud rate error.

Writing a new value to the SPBRG register causes the BRG timer to be reset (or cleared). This ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

EXAMPLE 9-1: CALCULATING BAUD RATE ERROR

For a device with Fosc of 16 MHz, desired baud rate of 9600, Asynchronous mode:

$$\text{Desired Baud Rate} = \frac{F_{OSC}}{64(SPBRG + 1)}$$

Solving for SPBRG:

$$X = \frac{\frac{F_{OSC}}{\text{Desired Baud Rate}}}{64} - 1$$

$$= \frac{\frac{16000000}{9600}}{64} - 1$$

$$= [25.042] = 25$$

$$\text{Calculated Baud Rate} = \frac{16000000}{64(25 + 1)}$$

$$= 9615$$

$$\text{Error} = \frac{\text{Calc. Baud Rate} - \text{Desired Baud Rate}}{\text{Desired Baud Rate}}$$

$$= \frac{(9615 - 9600)}{9600} = 0.16\%$$

TABLE 9-3: BAUD RATE FORMULAS

Configuration Bits		AUSART Mode	Baud Rate Formula
SYNC	BRGH		
0	0	Asynchronous	Fosc/[64 (n+1)]
0	1	Asynchronous	Fosc/[16 (n+1)]
1	x	Synchronous	Fosc/[4 (n+1)]

Legend: x = Don't care, n = value of SPBRG register

TABLE 9-4: REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for the Baud Rate Generator.

PIC16F913/914/916/917/946

NOTES:

REGISTER 10-3: LCDSEn: LCD SEGMENT ENABLE REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEn	SEn	SEn	SEn	SEn	SEn	SEn	SEn
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

SEn: Segment Enable bits

1 = Segment function of the pin is enabled

0 = I/O function of the pin is enabled

REGISTER 10-4: LCDDATAx: LCD DATA REGISTERS

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

SEGx-COMy: Pixel On bits

1 = Pixel on (dark)

0 = Pixel off (clear)

10.4 LCD Multiplex Types

The LCD driver module can be configured into one of four multiplex types:

- Static (only COM0 is used)
- 1/2 multiplex (COM<1:0> are used)
- 1/3 multiplex (COM<2:0> are used)
- 1/4 multiplex (COM<3:0> are used)

The LMUX<1:0> bit setting of the LCDCON register decides the function of RB5, RA2 or either RA3 or RD0 pins (see Table 10-2 for details).

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, then the TRIS setting of that pin is overridden.

Note: On a Power-on Reset, the LMUX<1:0> bits of the LCDCON register are '11'.

TABLE 10-2: RA3/RD0, RA2, RB5 FUNCTION

Multiplex	LMUX<1:0>	RA3/RD0 ⁽¹⁾	RA2	RB5
Static	00	Digital I/O	Digital I/O	Digital I/O
1/2	01	Digital I/O	Digital I/O	COM1 Driver
1/3	10	Digital I/O	COM2 Driver	COM1 Driver
1/4	11	COM3 Driver	COM2 Driver	COM1 Driver

Note 1: RA3 for PIC16F913/916, RD0 for PIC16F914/917 and PIC16F946

10.5 Segment Enables

The LCDSEn registers are used to select the pin function for each segment pin. The selection allows each pin to operate as either an LCD segment driver or as one of the pin's alternate functions. To configure the pin as a segment pin, the corresponding bits in the LCDSEn registers must be set to '1'.

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. Any bit set in the LCDSEn registers overrides any bit settings in the corresponding TRIS register.

Note: On a Power-on Reset, these pins are configured as digital I/O.

10.6 Pixel Control

The LCDDATAx registers contain bits which define the state of each pixel. Each bit defines one unique pixel.

Register 10-4 shows the correlation of each bit in the LCDDATAx registers to the respective common and segment signals.

Any LCD pixel location not being used for display can be used as general purpose RAM.

10.7 LCD Frame Frequency

The rate at which the COM and SEG outputs change is called the LCD frame frequency.

TABLE 10-3: FRAME FREQUENCY FORMULAS

Multiplex	Frame Frequency =
Static	$\text{Clock source}/(4 \times 1 \times (\text{LP}<3:0> + 1))$
1/2	$\text{Clock source}/(2 \times 2 \times (\text{LP}<3:0> + 1))$
1/3	$\text{Clock source}/(1 \times 3 \times (\text{LP}<3:0> + 1))$
1/4	$\text{Clock source}/(1 \times 4 \times (\text{LP}<3:0> + 1))$

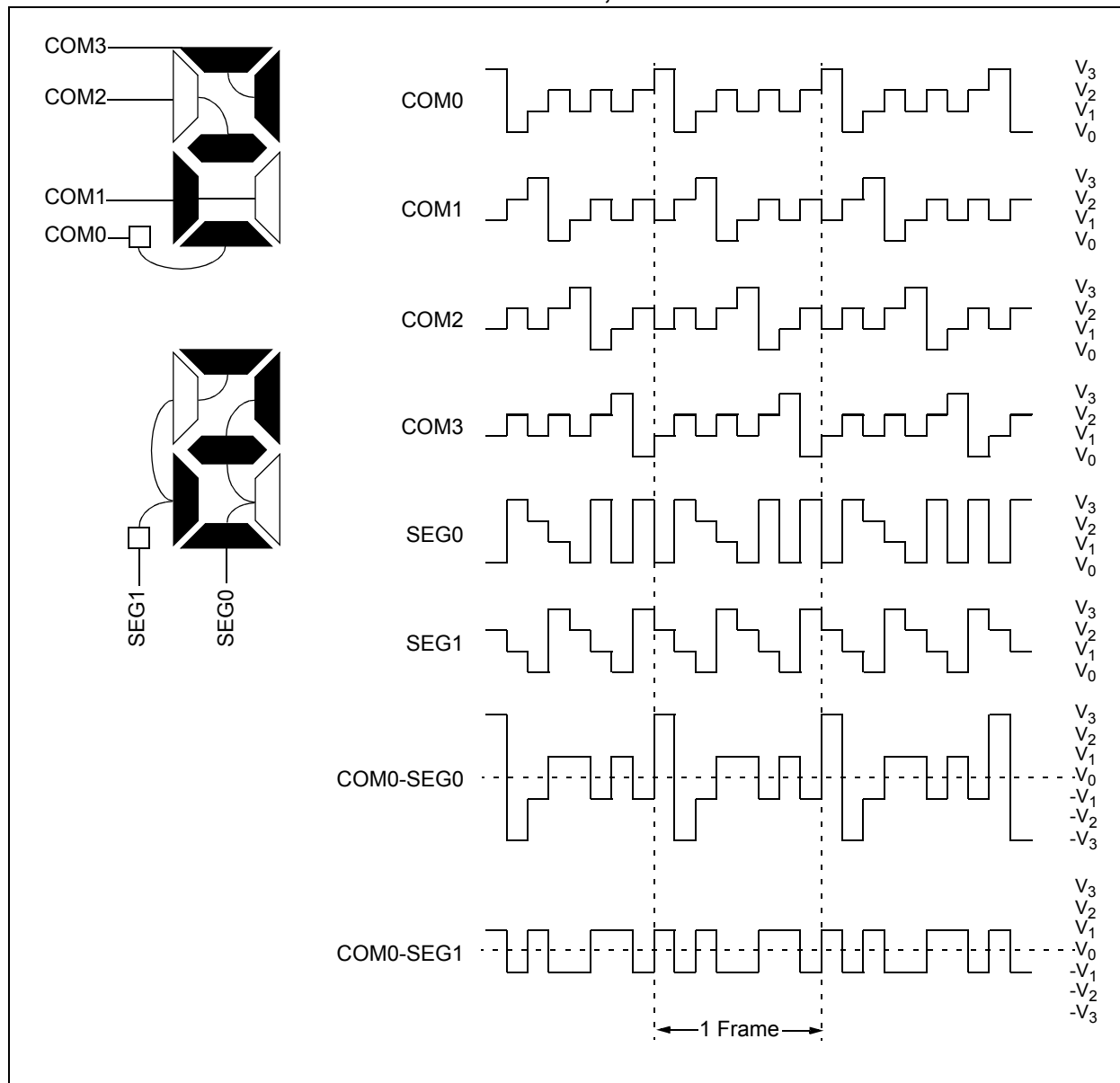
Note: Clock source is Fosc/8192, T1OSC/32 or LFINTOSC/32.

TABLE 10-4: APPROXIMATE FRAME FREQUENCY (IN Hz) USING Fosc @ 8 MHz, TIMER1 @ 32.768 kHz OR LFINTOSC

LP<3:0>	Static	1/2	1/3	1/4
2	85	85	114	85
3	64	64	85	64
4	51	51	68	51
5	43	43	57	43
6	37	37	49	37
7	32	32	43	32

PIC16F913/914/916/917/946

FIGURE 10-15: TYPE-A WAVEFORMS IN 1/4 MUX, 1/3 BIAS DRIVE



16.2.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register selects one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit of the PCON register enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 16-1 for the Configuration Word definition.

If VDD falls below VBOR for greater than parameter (TBOR) (see **Section 19.0 “Electrical Specifications”**), the Brown-out situation will reset the device. This will occur regardless of VDD slew rate. A Reset is not insured to occur if VDD falls below VBOR for less than parameter (TBOR).

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 16-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional 64 ms.

Note: The Power-up Timer is enabled by the PWRT $\overline{\text{E}}$ bit in the Configuration Word.

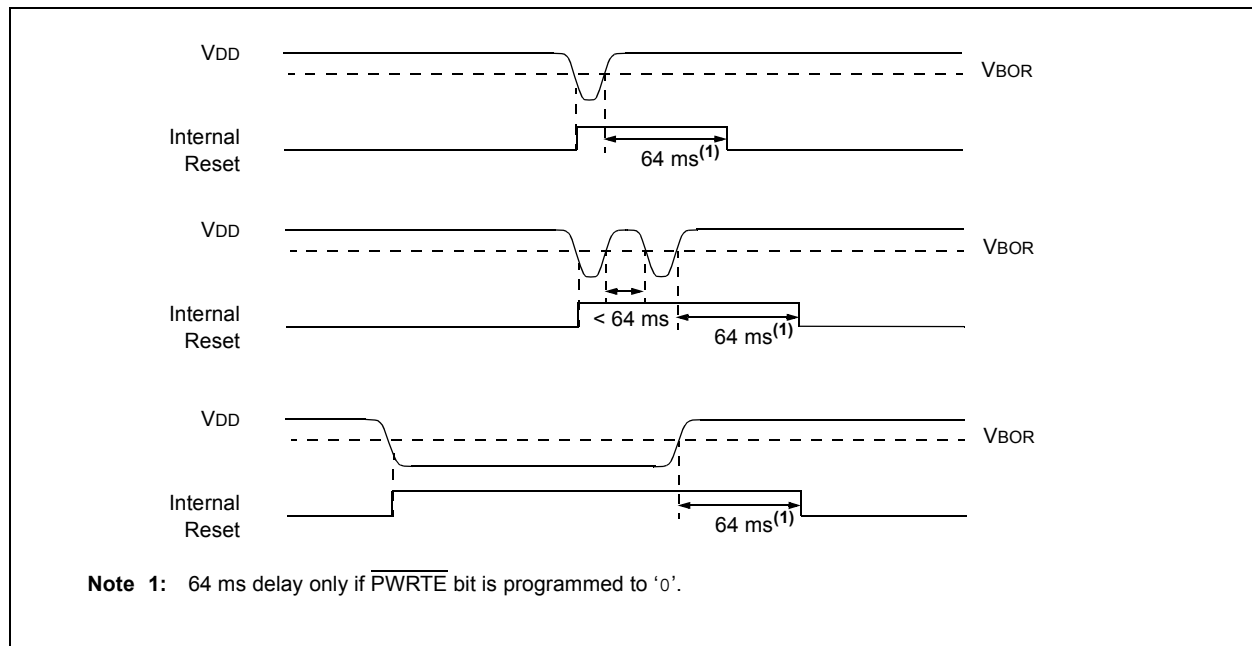
If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

16.2.5 BOR CALIBRATION

The PIC16F91X/946 stores the BOR calibration values in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the “PIC16F91X/946 Memory Programming Specification” (DS41244) and thus, does not require reprogramming.

Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See “PIC16F91X/946 Memory Programming Specification” (DS41244) for more information.

FIGURE 16-3: BROWN-OUT SITUATIONS



PIC16F913/914/916/917/946

16.3 Interrupts

The PIC16F91X/946 has multiple sources of interrupt:

- External Interrupt RB0/INT/SEG0
- TMR0 Overflow Interrupt
- PORTB Change Interrupts
- 2 Comparator Interrupts
- A/D Interrupt
- Timer1 Overflow Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- LCD Interrupt
- PLVD Interrupt
- USART Receive and Transmit interrupts
- CCP1 and CCP2 Interrupts
- Timer2 Interrupt

The Interrupt Control (INTCON), Peripheral Interrupt Request 1 (PIR1) and Peripheral Interrupt Request 2 (PIR2) registers record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON, PIE1 and PIE2 registers. GIE is cleared on Reset.

The Return from Interrupt instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- PORTB Change Interrupt
- TMR0 Overflow Interrupt

The peripheral interrupt flags are contained in the special registers, PIR1 and PIR2. The corresponding interrupt enable bit are contained in the special registers, PIE1 and PIE2.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- A/D Interrupt
- USART Receive and Transmit Interrupts
- Timer1 Overflow Interrupt
- CCP1 Interrupt
- SSP Interrupt
- Timer2 Interrupt

The following interrupt flags are contained in the PIR2 register:

- Fail-Safe Clock Monitor Interrupt
- Comparator 1 and 2 Interrupts
- LCD Interrupt
- PLVD Interrupt
- CCP2 Interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 16-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on how a module generates an interrupt, refer to the respective peripheral section.

Note: The ANSEL and CMCON0 registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. Also, if a LCD output function is active on an external interrupt pin, that interrupt function will be disabled.

16.3.1 RB0/INT/SEG0 INTERRUPT

External interrupt on RB0/INT/SEG0 pin is edge-triggered; either rising if the INTEDG bit of the OPTION register is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT/SEG0 pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The RB0/INT/SEG0 interrupt can wake-up the processor from Sleep if the INTE bit was set prior to going into Sleep. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up (0004h). See **Section 16.5 “Power-Down Mode (Sleep)”** for details on Sleep and Figure 16-10 for timing of wake-up from Sleep through RB0/INT/SEG0 interrupt.

16.3.2 TMR0 INTERRUPT

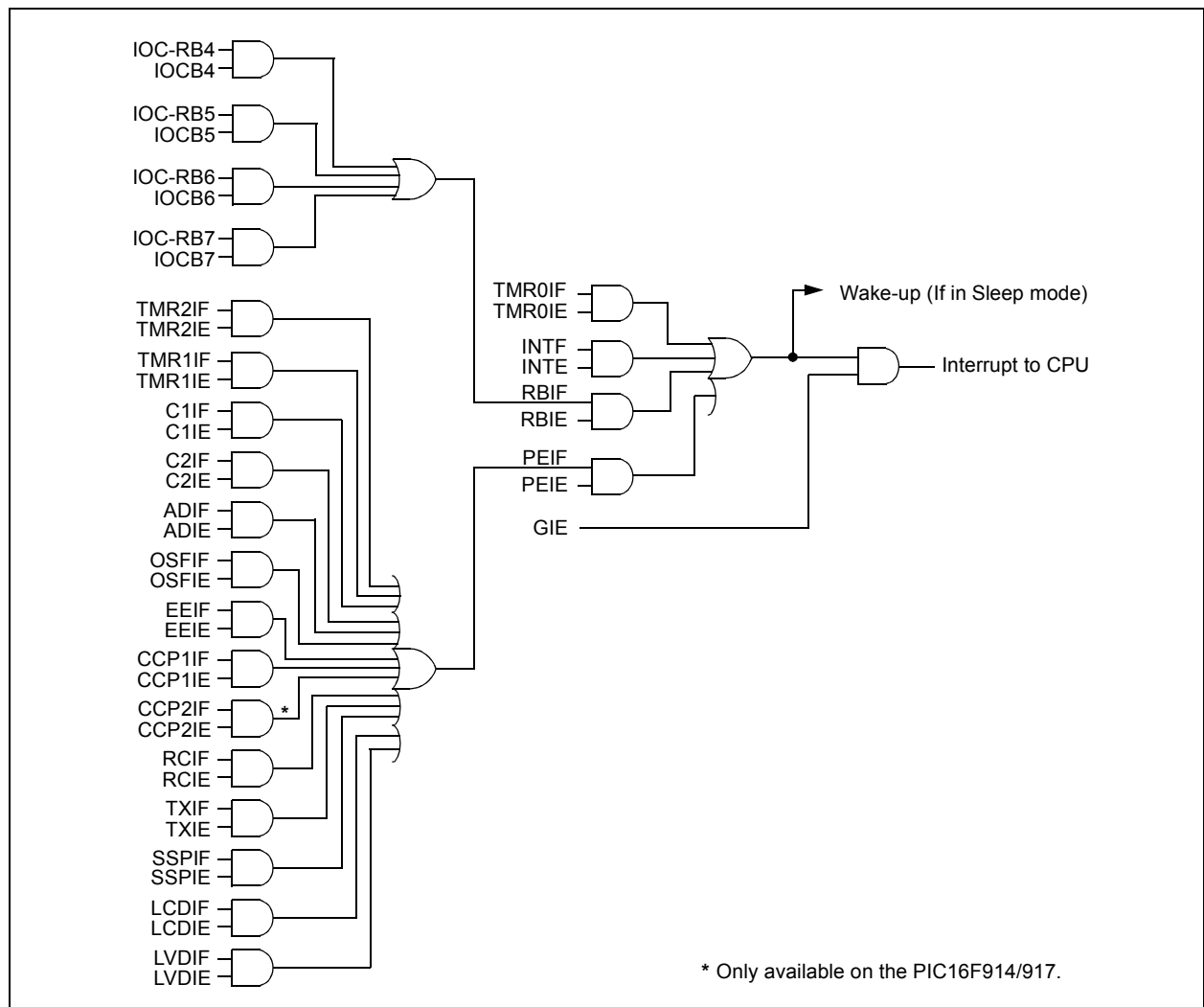
An overflow (FFh → 00h) in the TMR0 register will set the T0IF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing T0IE bit of the INTCON register. See **Section 5.0 “Timer0 Module”** for operation of the Timer0 module.

16.3.3 PORTB INTERRUPT

An input change on PORTB change sets the RBIF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing the RBIE bit of the INTCON register. Plus, individual pins can be configured through the IOCB register.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

FIGURE 16-7: INTERRUPT LOGIC



17.0 INSTRUCTION SET SUMMARY

The PIC16F913/914/916/917/946 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 17-1, while the various opcode fields are summarized in Table 17-1.

Table 17-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

17.1 Read-Modify-Write Operations

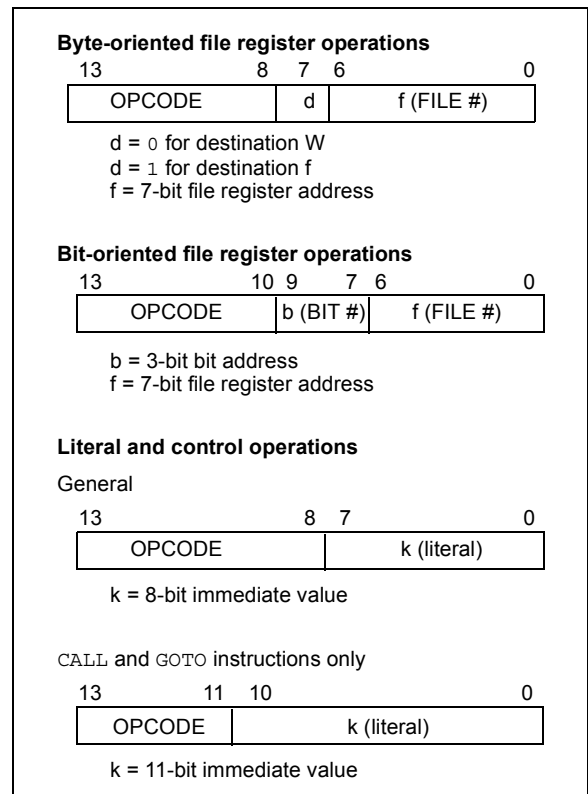
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a `CLRF PORTA` instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended consequence of clearing the condition that set the RBIF flag.

TABLE 17-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
C	Carry bit
DC	Digit carry bit
Z	Zero bit
PD	Power-down bit

FIGURE 17-1: GENERAL FORMAT FOR INSTRUCTIONS



PIC16F913/914/916/917/946

19.3 DC Characteristics: PIC16F913/914/916/917/946-I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial					
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
D020	Power-down Base Current(IPD) ⁽²⁾	—	0.05	1.2	μA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	1.5	μA	3.0	
		—	0.35	1.8	μA	5.0	
		—	150	500	nA	3.0	$-40^{\circ}\text{C} \leq T_A \leq +25^{\circ}\text{C}$
D021		—	1.0	2.2	μA	2.0	WDT Current ⁽¹⁾
		—	2.0	4.0	μA	3.0	
		—	3.0	7.0	μA	5.0	
D022A		—	42	60	μA	3.0	BOR Current ⁽¹⁾
		—	85	122	μA	5.0	
D022B		—	22	28	μA	2.0	PLVD Current
		—	25	35	μA	3.0	
		—	33	45	μA	5.0	
D023		—	32	45	μA	2.0	Comparator Current ⁽¹⁾ , both comparators enabled
		—	60	78	μA	3.0	
		—	120	160	μA	5.0	
D024		—	30	36	μA	2.0	CVREF Current ⁽¹⁾ (high range)
		—	45	55	μA	3.0	
		—	75	95	μA	5.0	
D025*		—	39	47	μA	2.0	CVREF Current ⁽¹⁾ (low range)
		—	59	72	μA	3.0	
		—	98	124	μA	5.0	
D026		—	2.0	5.0	μA	2.0	T1OSC Current ⁽¹⁾ , 32.768 kHz
		—	2.5	5.5	μA	3.0	
		—	3.0	7.0	μA	5.0	
D027		—	0.30	1.6	μA	3.0	A/D Current ⁽¹⁾ , no conversion in progress
		—	0.36	1.9	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

PIC16F913/914/916/917/946

19.7 Timing Parameter Symbolology

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T		
F	Frequency	T Time

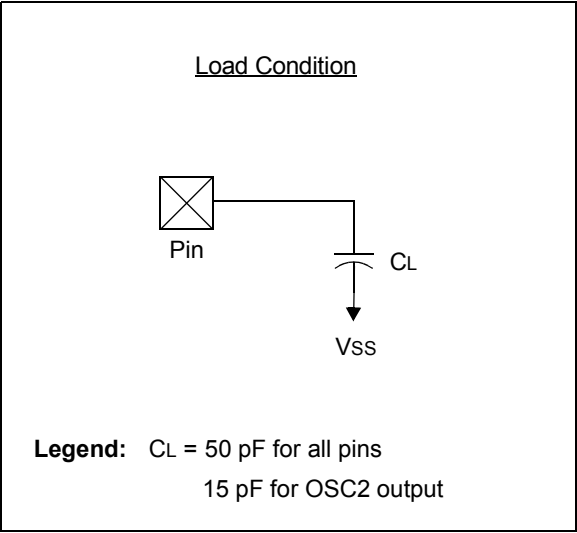
Lowercase letters (pp) and their meanings:

pp		
cc	CCP1	osc OSC1
ck	CLKOUT	rd \overline{RD}
cs	\overline{CS}	rw \overline{RD} or \overline{WR}
di	SDI	sc SCK
do	SDO	ss \overline{SS}
dt	Data in	t0 T0CKI
io	I/O port	t1 T1CKI
mc	\overline{MCLR}	wr \overline{WR}

Uppercase letters and their meanings:

S		
F	Fall	P Period
H	High	R Rise
I	Invalid (High-impedance)	V Valid
L	Low	Z High-impedance

FIGURE 19-3: LOAD CONDITIONS



PIC16F913/914/916/917/946

FIGURE 19-13: CAPTURE/COMPARE/PWM TIMINGS

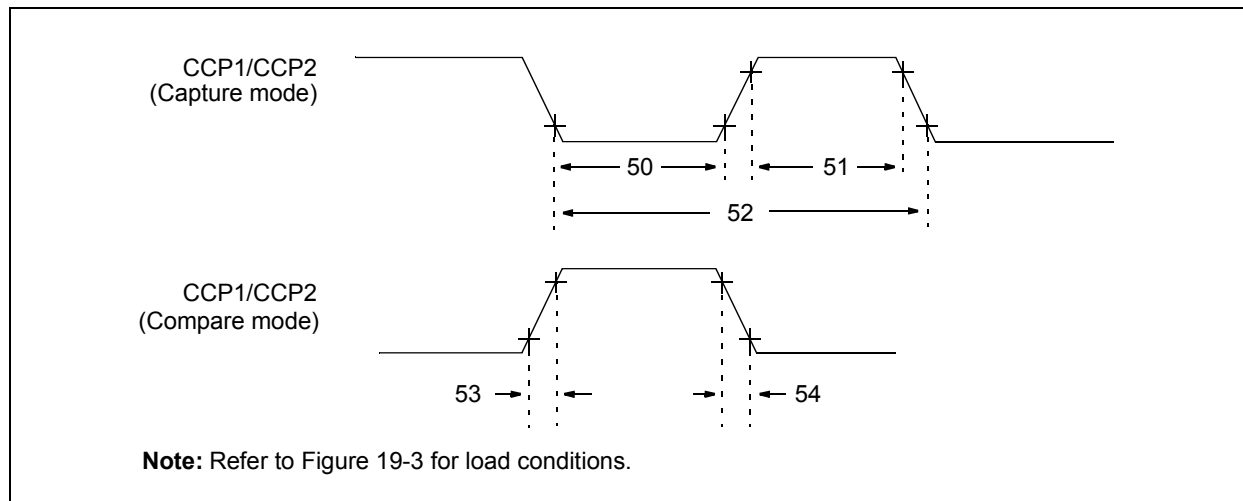


TABLE 19-12: CAPTURE/COMPARE/PWM (CCP) REQUIREMENTS

Param. No.	Sym.	Characteristic			Min.	Typ†	Max.	Units	Conditions
50*	TcCL	CCPx input low time	No Prescaler		0.5TCY + 5	—	—	ns	
			With Prescaler	3.0-5.5V	10	—	—	ns	
				2.0-5.5V	20	—	—	ns	
51*	TcCH	CCPx input high time	No Prescaler		0.5TCY + 5	—	—	ns	
			With Prescaler	3.0-5.5V	10	—	—	ns	
				2.0-5.5V	20	—	—	ns	
52*	TccP	CCPx input period			$\frac{3TCY + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCPx output fall time		3.0-5.5V	—	10	25	ns	
				2.0-5.5V	—	25	50	ns	
54*	TccF	CCPx output fall time		3.0-5.5V	—	10	25	ns	
				2.0-5.5V	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

PIC16F913/914/916/917/946

TABLE 19-15: I²C™ BUS START/STOP BITS REQUIREMENTS

Param No.	Symbol	Characteristic		Min.	Typ.	Max.	Units	Conditions
90*	TSU:STA	Start condition Setup time	400 kHz mode	600	—	—	ns	Only relevant for Repeated Start condition
91*	THD:STA	Start condition Hold time	400 kHz mode	600	—	—	ns	After this period, the first clock pulse is generated
92*	TSU:STO	Stop condition Setup time	400 kHz mode	600	—	—	ns	
93	THD:STO	Stop condition Hold time	400 kHz mode	600	—	—	ns	

* These parameters are characterized but not tested.

FIGURE 19-19: I²C™ BUS DATA TIMING

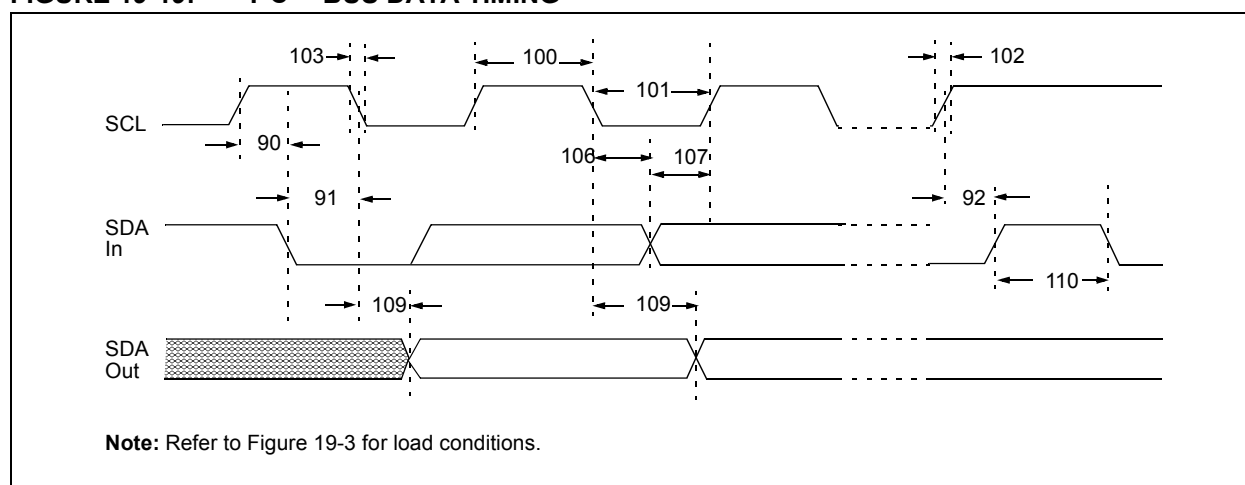


FIGURE 20-8: MAXIMUM I_{DD} vs. V_{DD} (EXTRC MODE)

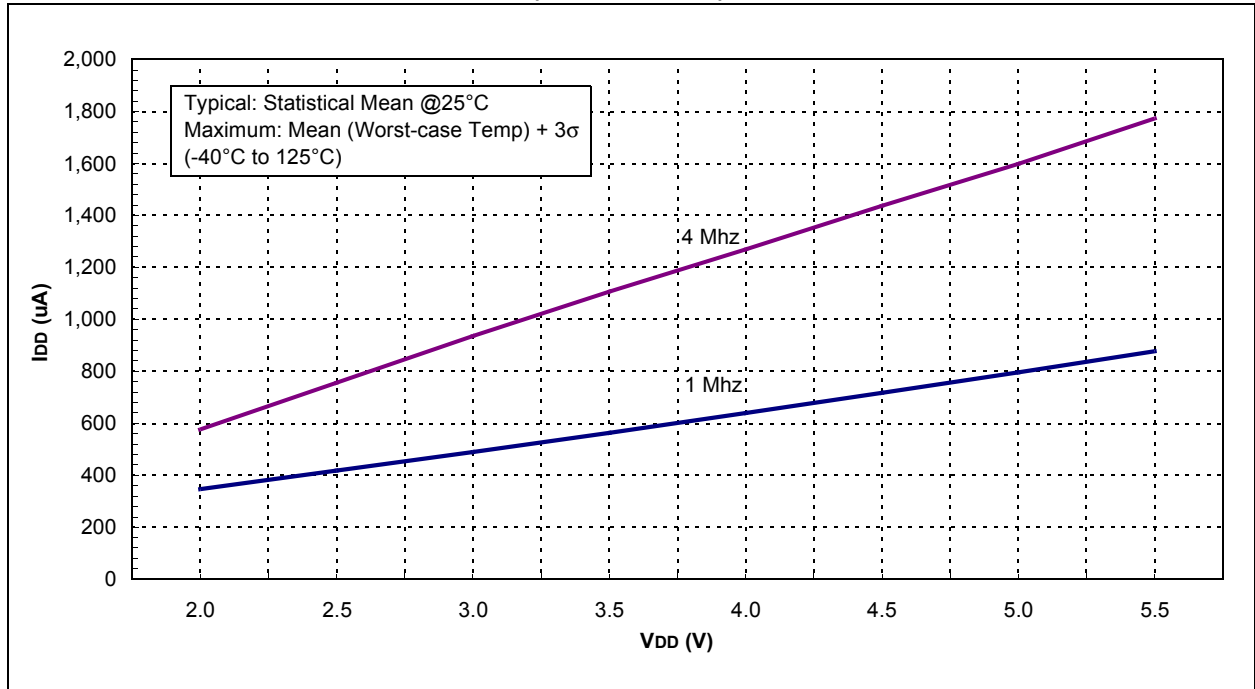
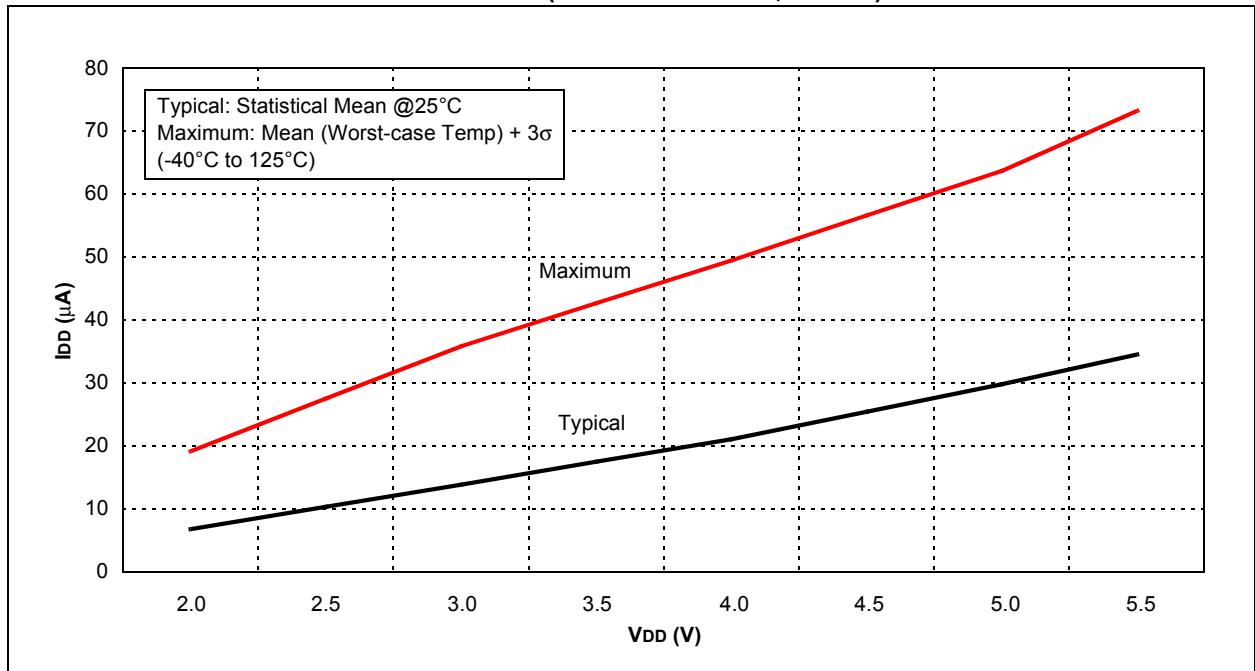


FIGURE 20-9: I_{DD} vs. V_{DD} OVER F_{osc} (LFINTOSC MODE, 31 kHz)



Registers.....	62
TRISC Register.....	62
TRISD	
Registers.....	71
TRISD Register.....	71
TRISE	
Registers.....	76
TRISE Register.....	76
TRISF	
Registers.....	81
TRISF Register.....	81
TRISG	
Registers.....	84
TRISG Register.....	84
Two-Speed Clock Start-up Mode.....	95
TXREG.....	123
TXSTA Register.....	130
BRGH Bit.....	132

U

UA.....	194
Update Address bit, UA.....	194
USART	
Synchronous Master Mode	
Requirements, Synchronous Receive.....	275
Requirements, Synchronous Transmission.....	275
Timing Diagram, Synchronous Receive.....	275
Timing Diagram, Synchronous Transmission.....	275

V

Voltage Reference. See Comparator Voltage	
Reference (CVREF)	
Voltage References	
Associated registers.....	119
VREF. SEE ADC Reference Voltage	

W

Wake-up Using Interrupts.....	236
Watchdog Timer (WDT).....	234
Associated Registers.....	235
Clock Source.....	234
Modes.....	234
Period.....	234
Specifications.....	269
WCOL bit.....	195
WDTCON Register.....	235
WPUB Register.....	55
Write Collision Detect bit (WCOL).....	195
WWW Address.....	325
WWW, On-Line Support.....	13