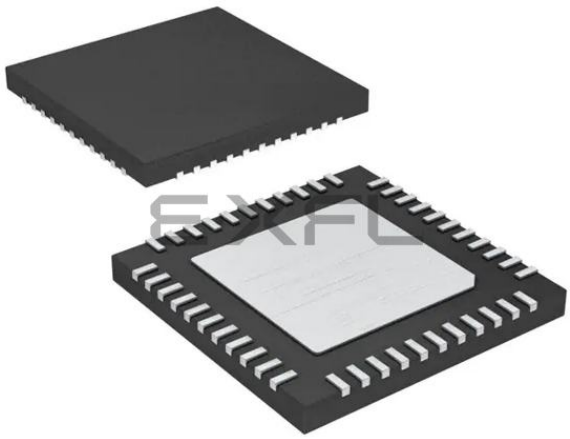

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Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	352 x 8
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Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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TABLE 1-1: PIC16F91X/946 PINOUT DESCRIPTIONS (CONTINUED)

Name	Function	Input Type	Output Type	Description
VSS	VSS	P	—	Ground reference for microcontroller.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels P = Power
HV = High Voltage XTAL = Crystal

Note 1: COM3 is available on RA3 for the PIC16F913/916 and on RD0 for the PIC16F914/917 and PIC16F946.
2: Pins available on PIC16F914/917 and PIC16F946 only.
3: Pins available on PIC16F946 only.
4: I^2C Schmitt trigger inputs have special input levels.

FIGURE 2-5: PIC16F946 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr. (1)	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h	TRISF	185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	LCDCON	107h	TRISG	187h
PORTD	08h	TRISD	88h	LCDPS	108h	PORTF	188h
PORTE	09h	TRISE	89h	LVDCON	109h	PORTG	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATL	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADRL	10Dh	EECON2(1)	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCTUNE	90h	LCDDATA0	110h	LCDDATA12	190h
TMR2	11h	ANSEL	91h	LCDDATA1	111h	LCDDATA13	191h
T2CON	12h	PR2	92h	LCDDATA2	112h	LCDDATA14	192h
SSPBUF	13h	SSPADD	93h	LCDDATA3	113h	LCDDATA15	193h
SSPCON	14h	SSPSTAT	94h	LCDDATA4	114h	LCDDATA16	194h
CCPR1L	15h	WPUB	95h	LCDDATA5	115h	LCDDATA17	195h
CCPR1H	16h	IOCB	96h	LCDDATA6	116h	LCDDATA18	196h
CCP1CON	17h	CMCON1	97h	LCDDATA7	117h	LCDDATA19	197h
RCSTA	18h	TXSTA	98h	LCDDATA8	118h	LCDDATA20	198h
TXREG	19h	SPBRG	99h	LCDDATA9	119h	LCDDATA21	199h
RCREG	1Ah		9Ah	LCDDATA10	11Ah	LCDDATA22	19Ah
CCPR2L	1Bh		9Bh	LCDDATA11	11Bh	LCDDATA23	19Bh
CCPR2H	1Ch	CMCON0	9Ch	LCDSE0	11Ch	LCDSE3	19Ch
CCP2CON	1Dh	VRCON	9Dh	LCDSE1	11Dh	LCDSE4	19Dh
ADRESH	1Eh	ADRESL	9Eh	LCDSE2	11Eh	LCDSE5	19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h – 7Fh	General Purpose Register 80 Bytes	A0h – EFh	General Purpose Register 80 Bytes	120h – 16Fh	General Purpose Register 80 Bytes	1A0h – 1EFh
accesses 70h-7Fh		accesses 70h-7Fh	F0h – FFh	accesses 70h-7Fh	170h – 17Fh	accesses 70h-7Fh	1F0h – 1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

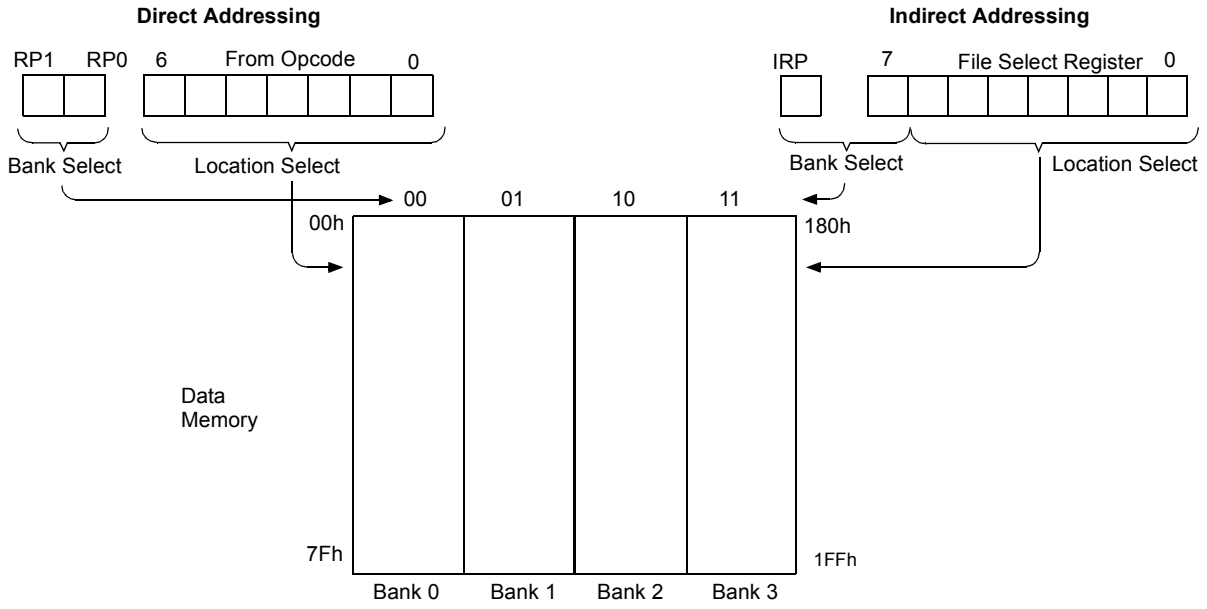
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit of the STATUS register, as shown in Figure 2-7.

A simple program to clear RAM location 020h-02Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: INDIRECT ADDRESSING

```
     MOVLW    020h   ;initialize pointer
     MOVWF    FSR    ;to RAM
     BANKISEL 020h
NEXT CLRF     INDF   ;clear INDF register
     INCF     FSR    ;inc pointer
     BTFSS    FSR,4  ;all done?
     GOTO     NEXT   ;no clear next
CONTINUE             ;yes continue
```

FIGURE 2-7: DIRECT/INDIRECT ADDRESSING PIC16F91X/946



Note: For memory map detail, see Figures 2-3 and 2-4.

REGISTER 3-4: PORTB: PORTB REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **RB<7:0>**: PORTB I/O Pin bits
1 = Port pin is >VIH min.
0 = Port pin is <VIL max.

REGISTER 3-5: TRISB: PORTB TRI-STATE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TRISB<7:0>:** PORTB Tri-State Control bits
1 = PORTB pin configured as an input (tri-stated)
0 = PORTB pin configured as an output

REGISTER 3-6: IOCB: PORTB INTERRUPT-ON-CHANGE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **IOCB<7:4>:** Interrupt-on-Change bits
1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

bit 3-0 **Unimplemented:** Read as '0'

3.4.3.8 RB7/ICSPDAT/ICDDAT/SEG13

Figure 3-13 shows the diagram for this pin. The RB7 pin is configurable to function as one of the following:

- a general purpose I/O
- an In-Circuit Serial Programming™ I/O
- an ICD data I/O
- an analog output for the LCD

FIGURE 3-13: BLOCK DIAGRAM OF RB7

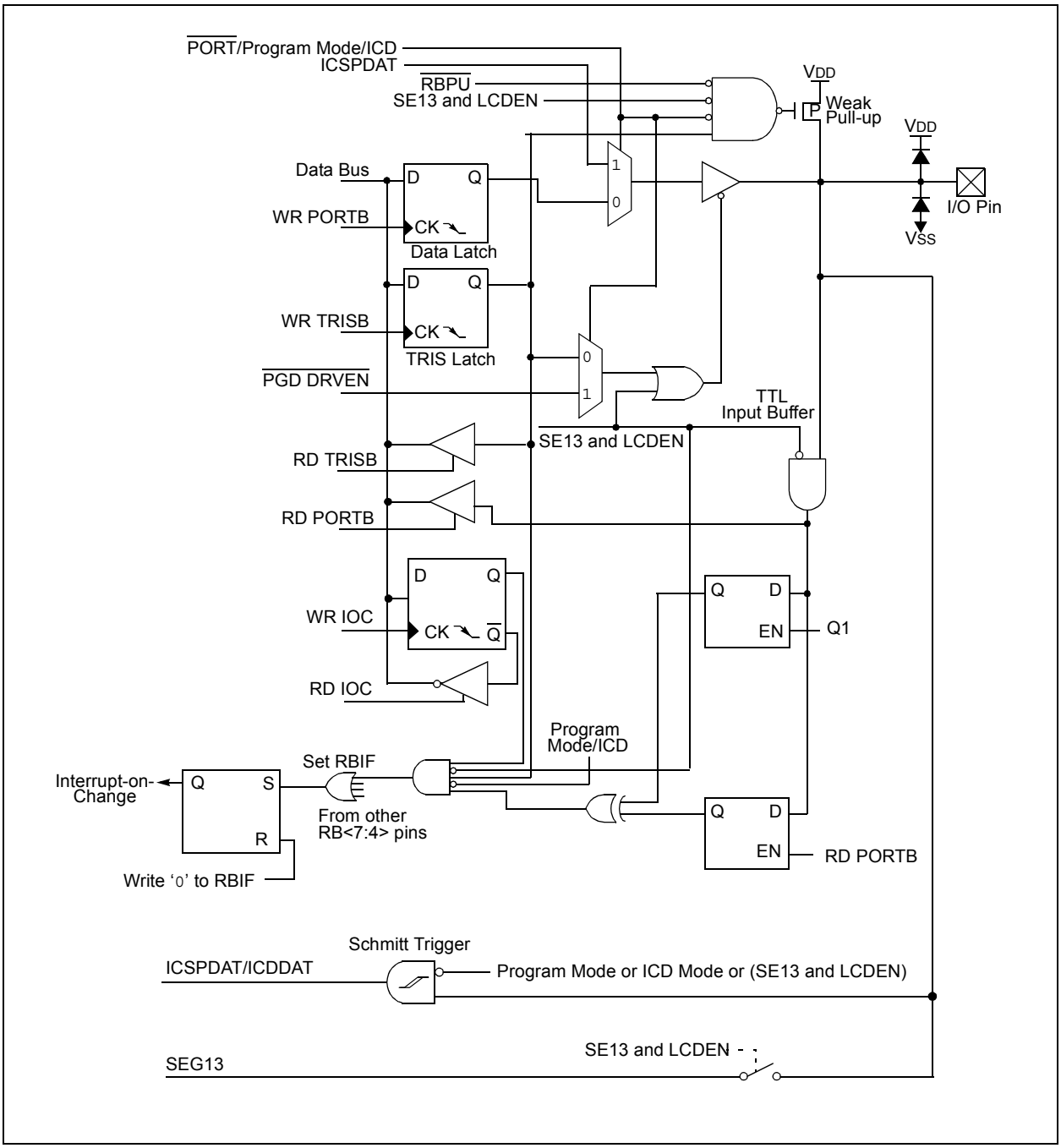


FIGURE 3-22: BLOCK DIAGRAM OF RD0

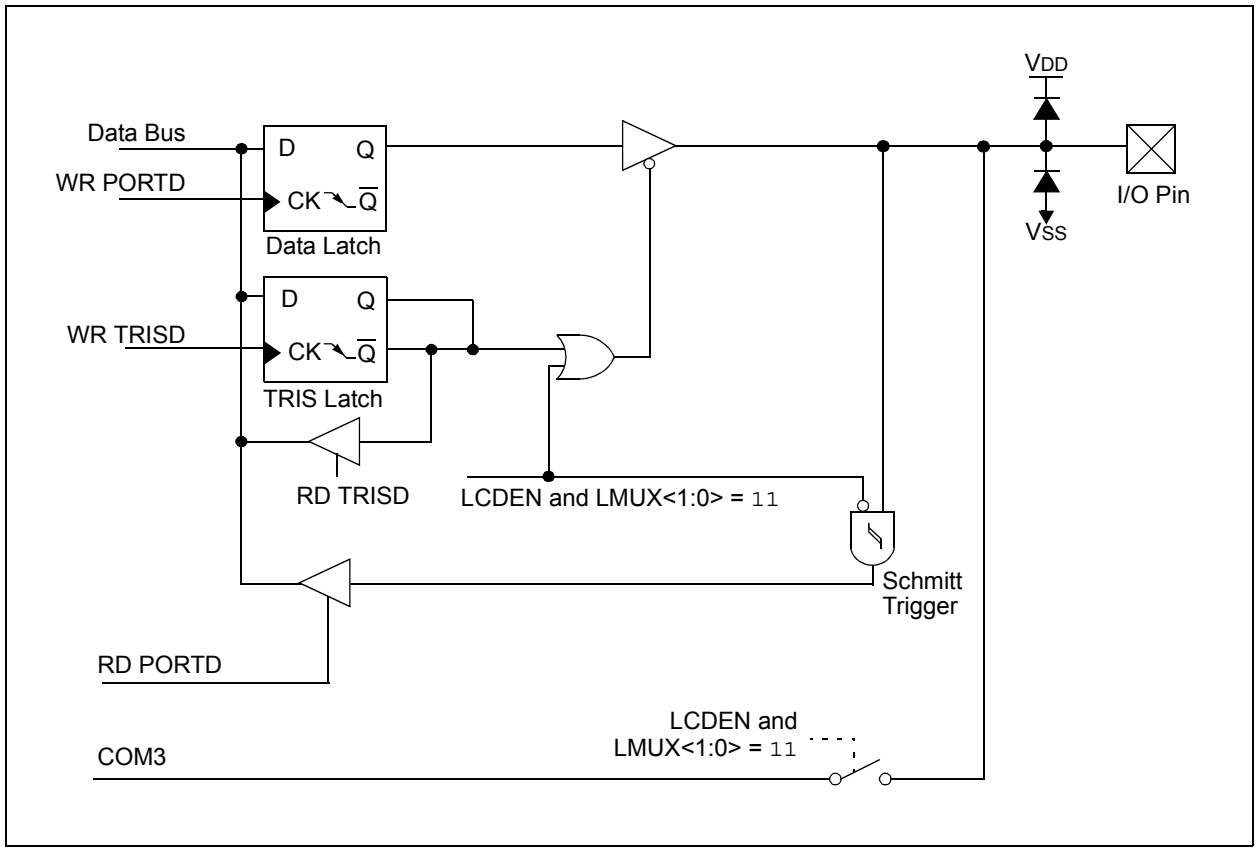


FIGURE 3-23: BLOCK DIAGRAM OF RD1

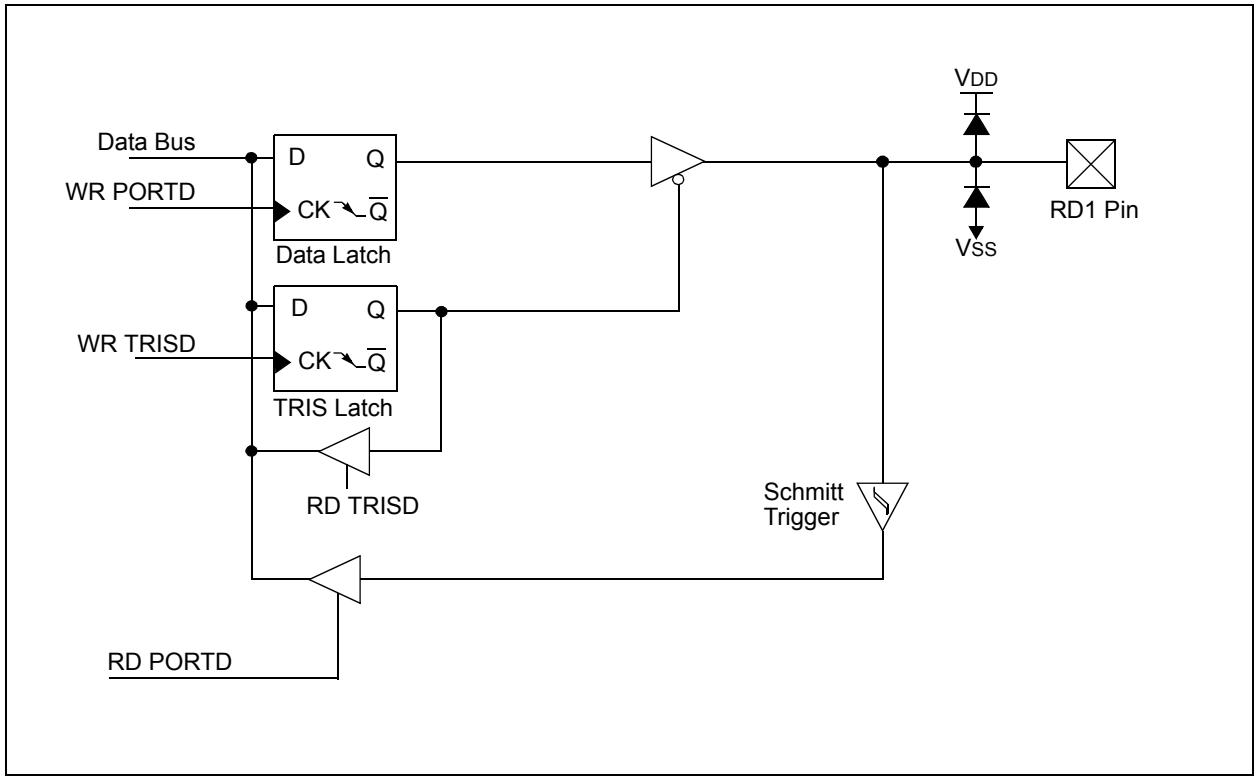


FIGURE 3-26: BLOCK DIAGRAM OF RE<2:0> (PIC16F914/917 AND PIC16F946 ONLY)

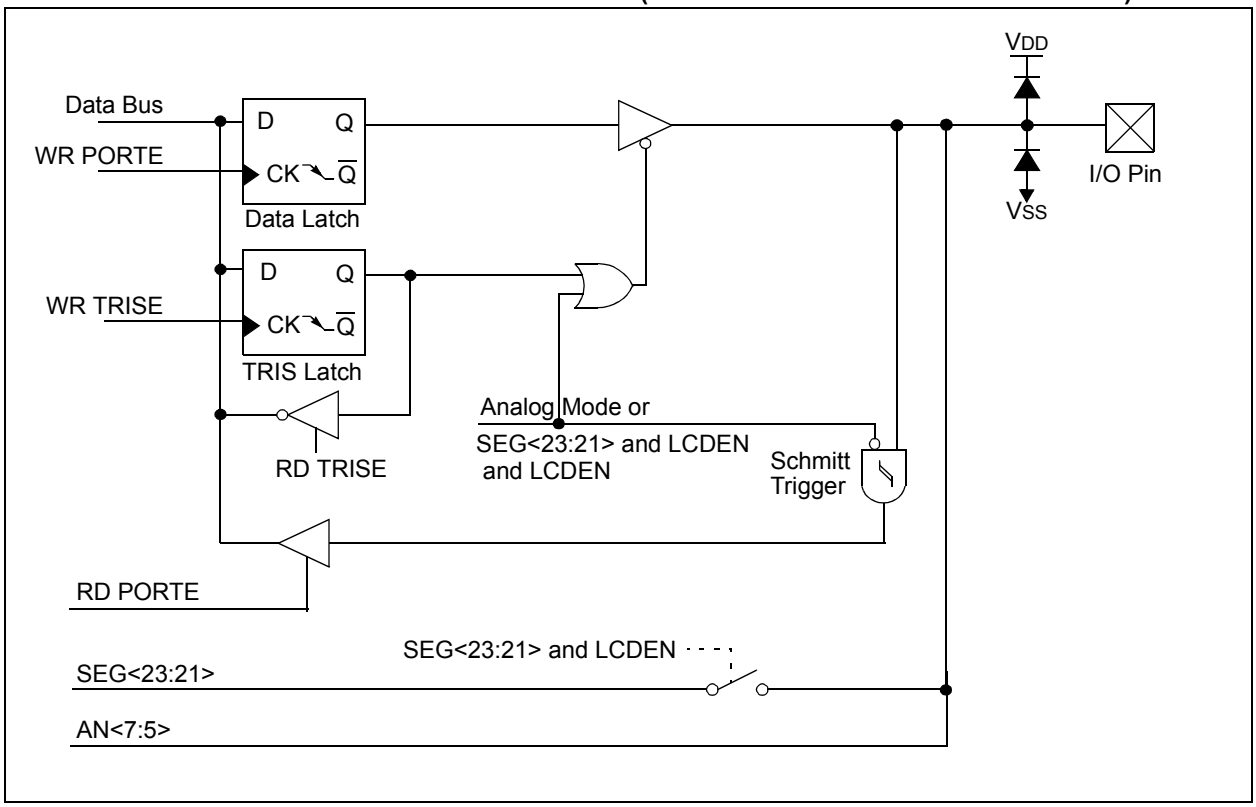
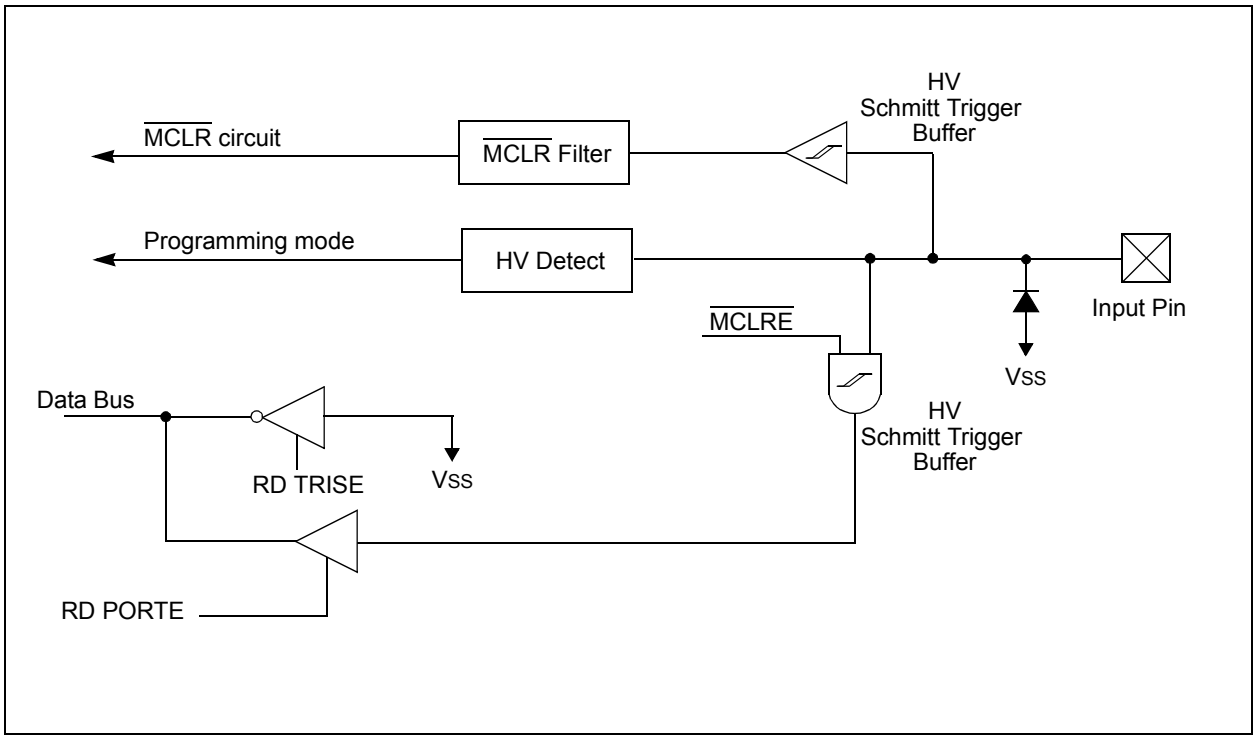


FIGURE 3-27: BLOCK DIAGRAM OF RE3



REGISTER 8-1: CMCON0: COMPARATOR CONFIGURATION REGISTER

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C2OUT:** Comparator 2 Output bit
When C2INV = 0:
1 = C2 VIN+ > C2 VIN-
0 = C2 VIN+ < C2 VIN-
When C2INV = 1:
1 = C2 VIN+ < C2 VIN-
0 = C2 VIN+ > C2 VIN-

bit 6 **C1OUT:** Comparator 1 Output bit
When C1INV = 0:
1 = C1 VIN+ > C1 VIN-
0 = C1 VIN+ < C1 VIN-
When C1INV = 1:
1 = C1 VIN+ < C1 VIN-
0 = C1 VIN+ > C1 VIN-

bit 5 **C2INV:** Comparator 2 Output Inversion bit
1 = C2 output inverted
0 = C2 output not inverted

bit 4 **C1INV:** Comparator 1 Output Inversion bit
1 = C1 Output inverted
0 = C1 Output not inverted

bit 3 **CIS:** Comparator Input Switch bit
When CM<2:0> = 010:
1 = C1IN+ connects to C1 VIN-
C2IN+ connects to C2 VIN-
0 = C1IN- connects to C1 VIN-
C2IN- connects to C2 VIN-
When CM<2:0> = 001:
1 = C1IN+ connects to C1 VIN-
0 = C1IN- connects to C1 VIN-
When CM<2:0> = 101: (16F91x/946)
1 = C2 VIN+ connects to fixed voltage reference
0 = C2 VIN+ connects to C2IN+

bit 2-0 **CM<2:0>:** Comparator Mode bits (See Figure 8-5)
000 = Comparators off. CxIN pins are configured as analog
001 = Three inputs multiplexed to two comparators
010 = Four inputs multiplexed to two comparators
011 = Two common reference comparators
100 = Two independent comparators
101 = One independent comparator
110 = Two comparators with outputs and common reference
111 = Comparators off. CxIN pins are configured as digital I/O

REGISTER 10-1: LCDCON: LIQUID CRYSTAL DISPLAY CONTROL REGISTER

R/W-0	R/W-0	R/C-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
LCDEN	$\overline{\text{SLPEN}}$	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
C = Only clearable bit	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
-n = Value at POR			

bit 7 **LCDEN:** LCD Driver Enable bit
1 = LCD driver module is enabled
0 = LCD driver module is disabled

bit 6 **$\overline{\text{SLPEN}}$:** LCD Driver Enable in Sleep mode bit
1 = LCD driver module is disabled in Sleep mode
0 = LCD driver module is enabled in Sleep mode

bit 5 **WERR:** LCD Write Failed Error bit
1 = LCDDATAx register written while the WA bit of the LCDPS register = 0 (must be cleared in software)
0 = No LCD write error

bit 4 **VLCDEN:** LCD Bias Voltage Pins Enable bit
1 = VLCD pins are enabled
0 = VLCD pins are disabled

bit 3-2 **CS<1:0>:** Clock Source Select bits
00 = FOSC/8192
01 = T1OSC (Timer1)/32
1x = LFINTOSC (31 kHz)/32

bit 1-0 **LMUX<1:0>:** Commons Select bits

LMUX<1:0>	Multiplex	Maximum Number of Pixels			Bias
		PIC16F913/916	PIC16F914/917	PIC16F946	
00	Static (COM0)	16	24	42	Static
01	1/2 (COM<1:0>)	32	48	84	1/2 or 1/3
10	1/3 (COM<2:0>)	48	72	126	1/2 or 1/3
11	1/4 (COM<3:0>)	60(1)	96	168	1/3

Note 1: On PIC16F913/916 devices, COM3 and SEG15 are shared on one pin, limiting the device from driving 64 pixels.

TABLE 10-6: REGISTERS ASSOCIATED WITH LCD OPERATION (CONTINUED)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
LCDSE2(2)	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000	uuuu uuuu
LCDSE3(3)	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	0000 0000	0000 0000
LCDSE4(3)	SE39	SE38	SE37	SE36	SE35	SE34	SE33	SE32	0000 0000	0000 0000
LCDSE5(3)	—	—	—	—	—	—	SE41	SE40	---- --00	---- --00
PIE2	OSFIE	C2IE	C1IE	LCDIE	—	LVDIE	—	CCP2IE	0000 -0-0	0000 -0-0
PIR2	OSFIF	C2IF	C1IF	LCDIF	—	LVDIF	—	CCP2IF	0000 -0-0	0000 -0-0
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the LCD module.
Note 1: These pins may be configured as port pins, depending on the oscillator mode selected.
2: PIC16F914/917 and PIC16F946 only.
3: PIC16F946 only.

REGISTER 12-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG1	VCFG0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **VCFG1:** Voltage Reference bit
1 = V_{REF-} pin
0 = V_{SS}

bit 5 **VCFG0:** Voltage Reference bit
1 = V_{REF+} pin
0 = V_{SS}

bit 4-2 **CHS<2:0>:** Analog Channel Select bits
000 = AN0
001 = AN1
010 = AN2
011 = AN3
100 = AN4
101 = AN5**(1)**
110 = AN6**(1)**
111 = AN7**(1)**

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

Note 1: Not available on 28-pin devices.

13.1.2 READING THE DATA EEPROM MEMORY

To read a data memory location, the user must write the address to the EEADRL register, clear the EEPGD control bit, and then set control bit RD of the EECON1 register. The data is available in the very next cycle, in the EEDATL register; therefore, it can be read in the next instruction. EEDATL will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 13-1: DATA EEPROM READ

```
BANKSEL EEADRL          ;
MOVF    DATA_EE_ADDR,W  ;Data Memory
MOVWF   EEADRL          ;Address to read
BANKSEL EECON1          ;
BCF     EECON1,EEPGD    ;Point to Data
                        ;memory
BSF     EECON1,RD       ;EE Read
BANKSEL EEDATL          ;
MOVF    EEDATL,W        ;W = EEPROM Data
```

13.1.3 WRITING TO THE DATA EEPROM MEMORY

To write an EEPROM data location, the user must first write the address to the EEADRL register and the data to the EEDATL register. Then the user must follow a specific sequence to initiate the write for each byte.

The write will not initiate if the sequence described below is not followed exactly (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. Interrupts should be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

The steps to write to EEPROM data memory are:

1. If step 10 is not implemented, check the WR bit to see if a write is in progress.
2. Write the address to EEADRL. Make sure that the address is not larger than the memory size of the device.
3. Write the 8-bit data value to be programmed in the EEDATL register.
4. Clear the EEPGD bit to point to EEPROM data memory.
5. Set the WREN bit to enable program operations.
6. Disable interrupts (if enabled).
7. Execute the special five instruction sequence:
   - Write 55h to EECON2 in two steps (first to W, then to EECON2)
   - Write AAh to EECON2 in two steps (first to W, then to EECON2)
   - Set the WR bit
8. Enable interrupts (if using interrupts).
9. Clear the WREN bit to disable program operations.
10. At the completion of the write cycle, the WR bit is cleared and the EEIF interrupt flag bit is set. (EEIF must be cleared by firmware.) If step 1 is not implemented, then firmware should check for EEIF to be set, or WR to clear, to indicate the end of the program cycle.

EXAMPLE 13-2: DATA EEPROM WRITE

```
        BANKSEL EECON1          ;
        BTFSC   EECON1,WR       ;Wait for write
        GOTO    $-1             ;to complete
        BANKSEL EEADRL          ;
        MOVF    DATA_EE_ADDR,W  ;Data Memory
        MOVWF   EEADRL          ;Address to write
        MOVF    DATA_EE_DATA,W  ;Data Memory Value
        MOVWF   EEDATL          ;to write
        BANKSEL EECON1          ;
        BCF     EECON1,EEPGD    ;Point to DATA
                                ;memory
        BSF     EECON1,WREN     ;Enable writes

        BCF     INTCON,GIE      ;Disable INTs.
Required
Sequence
        MOVLW   55h             ;
        MOVWF   EECON2          ;Write 55h
        MOVLW   AAh             ;
        MOVWF   EECON2          ;Write AAh
        BSF     EECON1,WR       ;Set WR bit to
                                ;begin write
        BSF     INTCON,GIE      ;Enable INTs.
        BCF     EECON1,WREN     ;Disable writes
```

14.12.1 ADDRESSING

Once the SSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of register SSPADD <7:1>. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

a) The SSPSR register value is loaded into the SSPBUF register.
b) The buffer full bit, BF is set.
c) An $\overline{ACK}$ pulse is generated.
d) SSP interrupt flag bit, SSPIF of the PIR1 register is set (interrupt is generated if enabled) on the falling edge of the ninth SCL pulse.

In 10-bit Address mode, two address bytes need to be received by the slave (Figure 14-8). The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/$\overline{W}$ (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address.

The sequence of events for 10-bit address is as follows, with steps 7-9 for slave-transmitter:

1. Receive first (high) byte of address (bits SSPIF, BF and bit UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with second (low) byte of address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of address (bits SSPIF, BF and UA are set).
5. Update the SSPADD register with the first (high) byte of address; if match releases SCL line, this will clear bit UA.
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive repeated Start condition.
8. Receive first (high) byte of address (bits SSPIF and BF are set).
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

TABLE 14-3: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received		SSPSR → SSPBUF	Generate $\overline{ACK}$ Pulse	Set bit SSPIF (SSP Interrupt occurs if enabled)
BF	SSPOV			
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

Note: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

15.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

The timer resources used by the module are shown in Table 15-1.

Additional information on CCP modules is available in the Application Note AN594, *"Using the CCP Modules"* (DS00594).

TABLE 15-1: CCP MODE – TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

TABLE 15-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time base
Capture	Compare	Same TMR1 time base
Compare	Compare	Same TMR1 time base
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt). The rising edges will be aligned.
PWM	Capture	None
PWM	Compare	None

Note: CCPRx and CCPx throughout this document refer to CCPR1 or CCPR2 and CCP1 or CCP2, respectively.

20.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 20-1: TYPICAL IDD vs. FOSC OVER VDD (EC MODE)

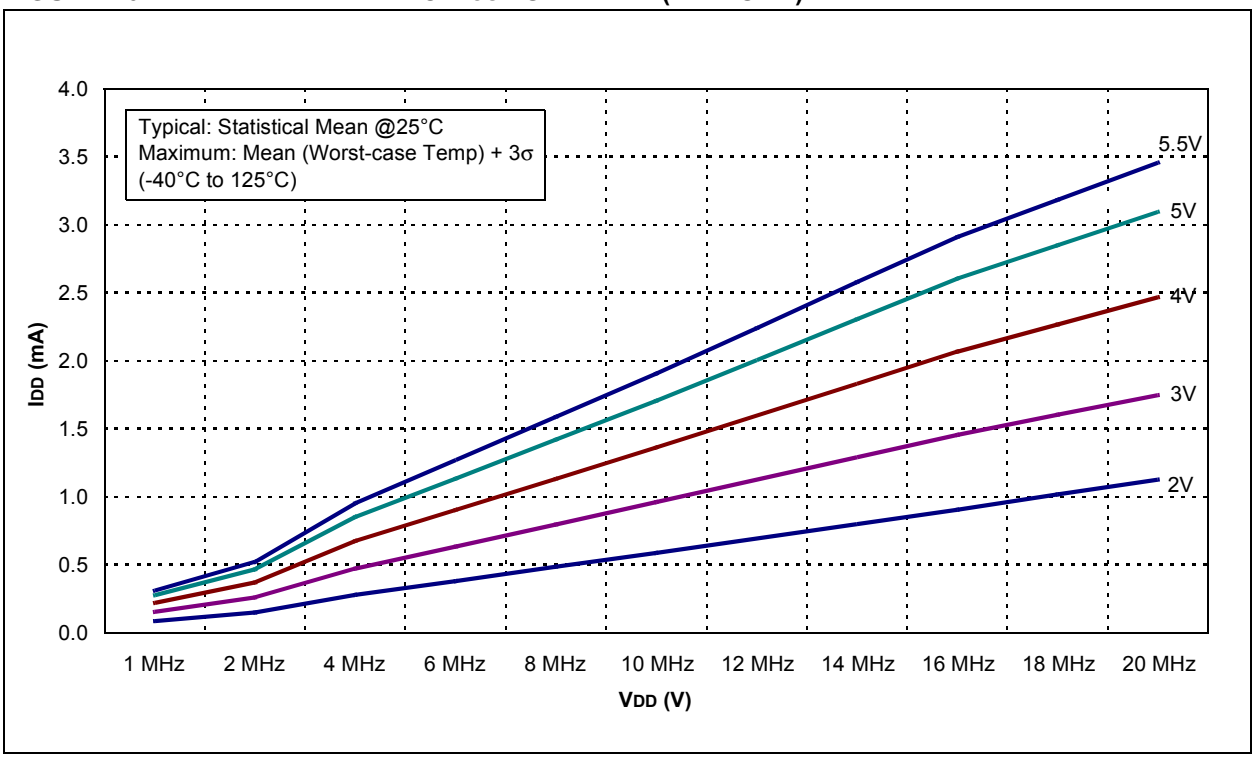


FIGURE 20-10: IDD vs. VDD (LP MODE)

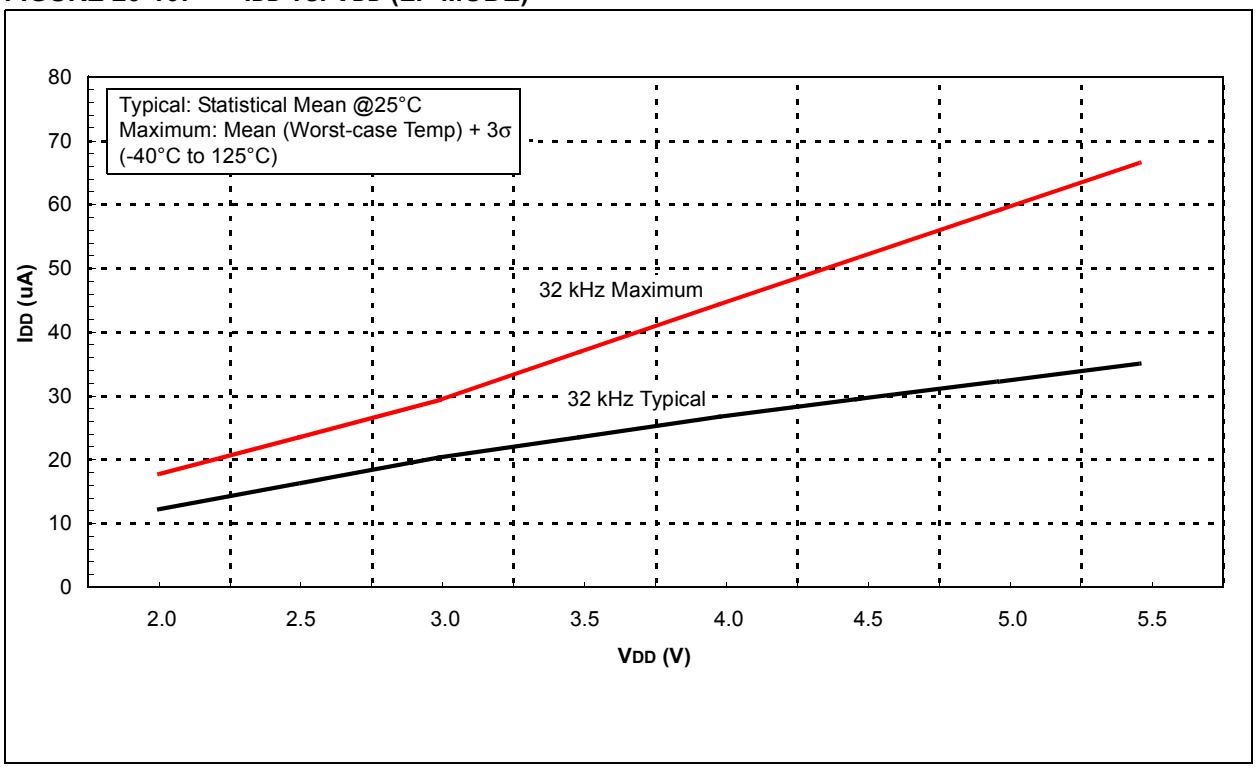


FIGURE 20-11: TYPICAL IDD vs. FOSC OVER VDD (HFINTOSC MODE)

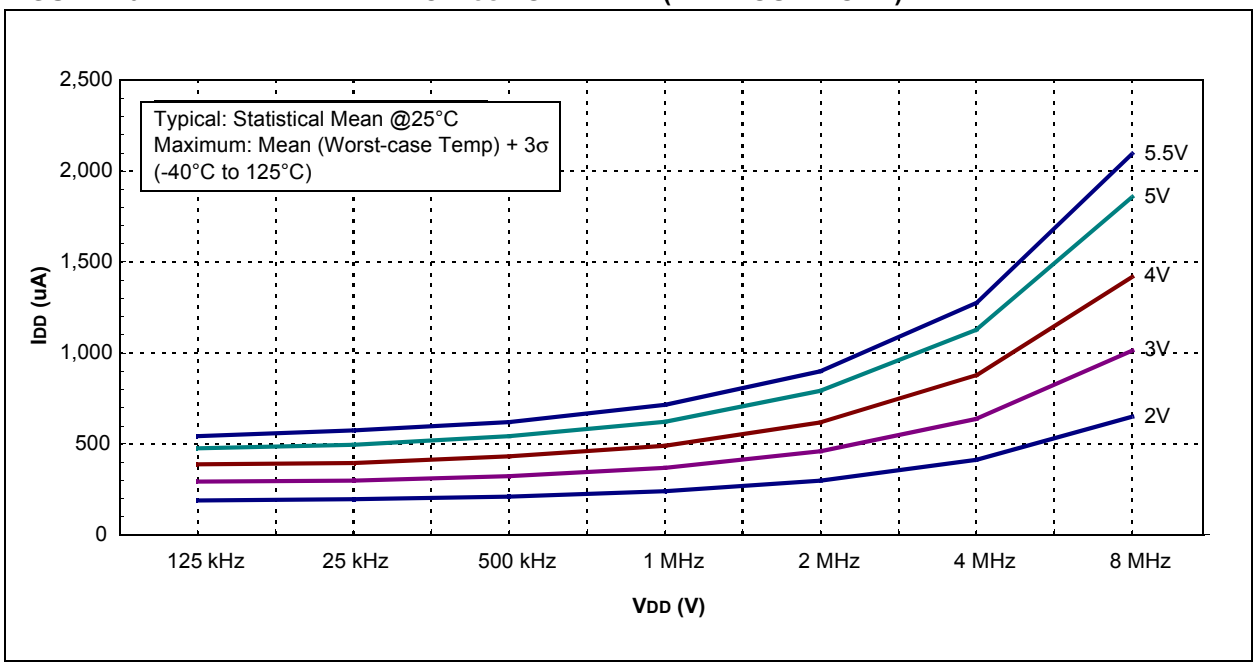


FIGURE 20-28: VOH vs. IOH OVER TEMPERATURE (VDD = 5.0V)

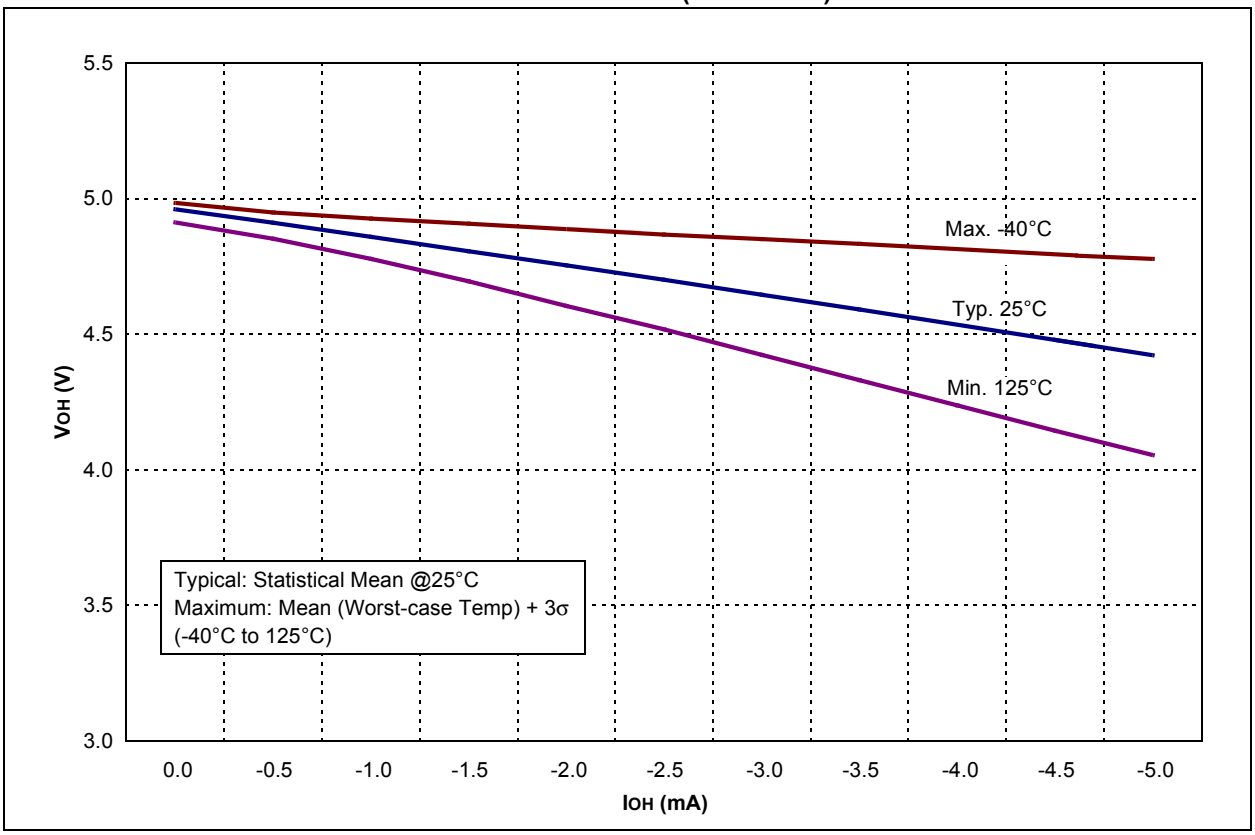


FIGURE 20-29: TTL INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

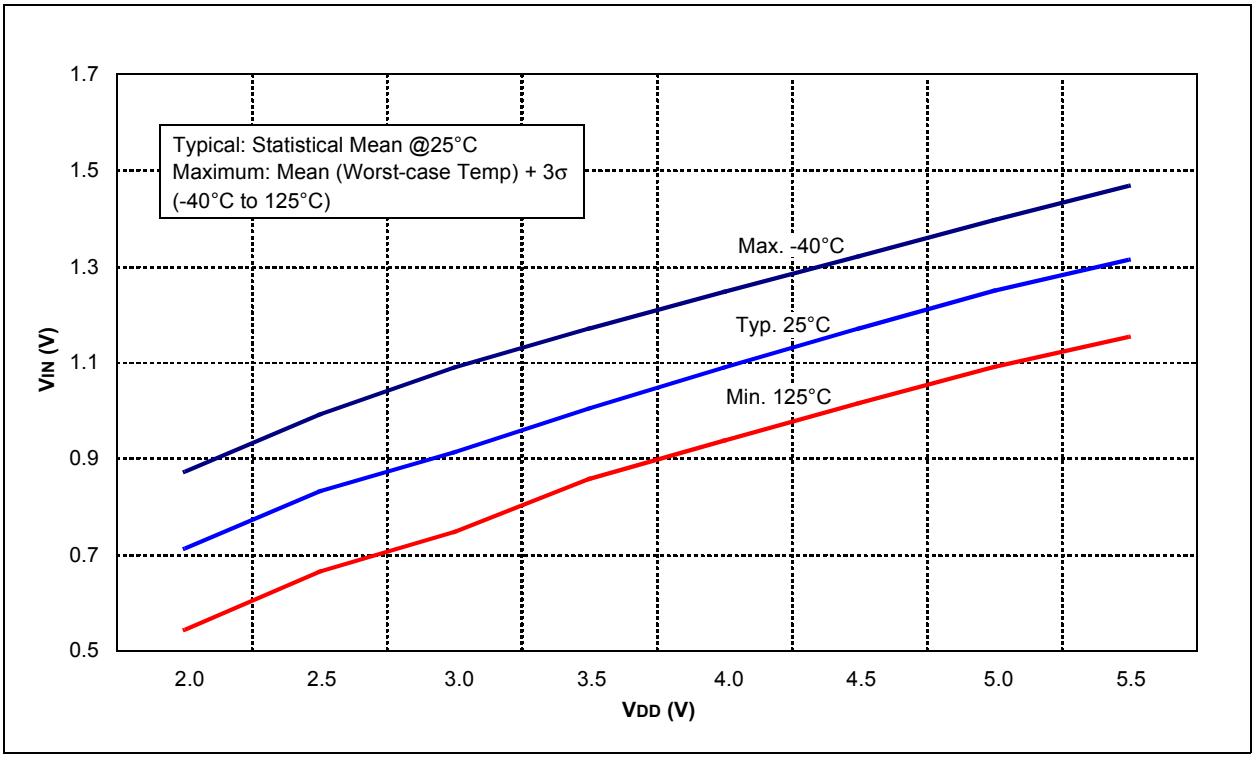


FIGURE 20-36: MAXIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

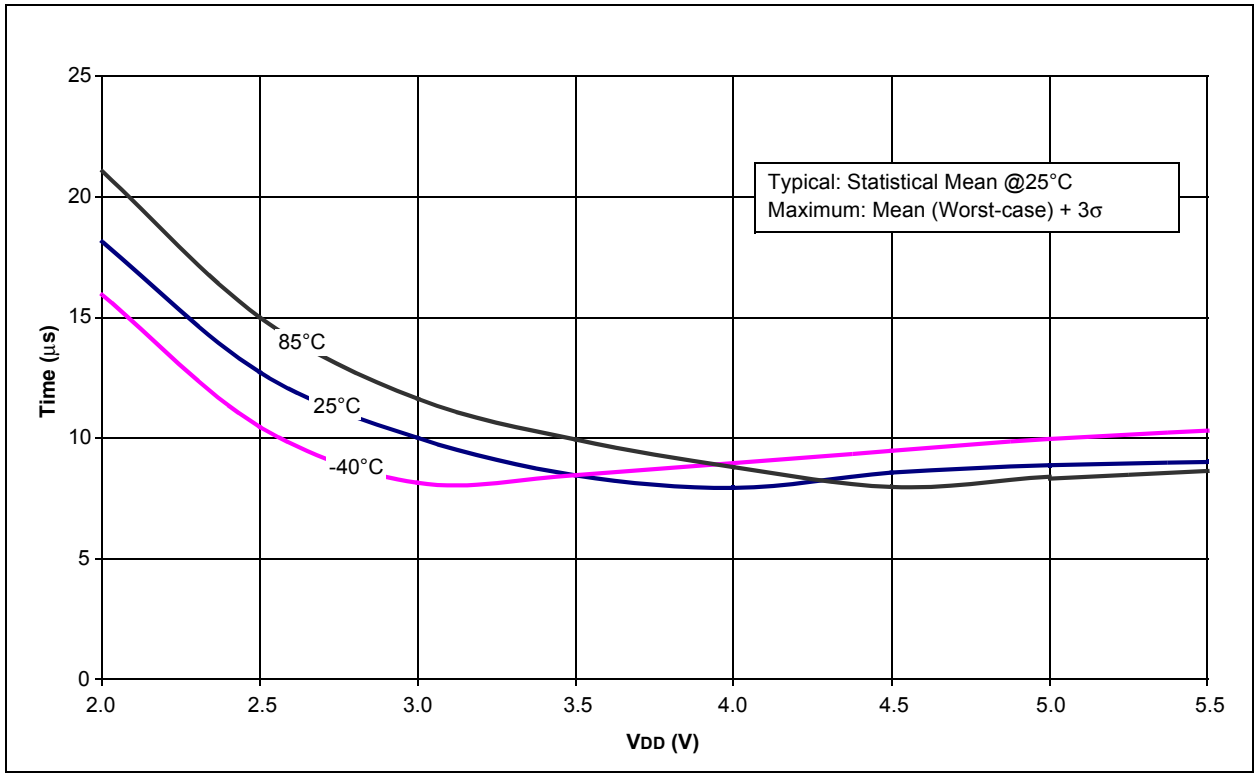
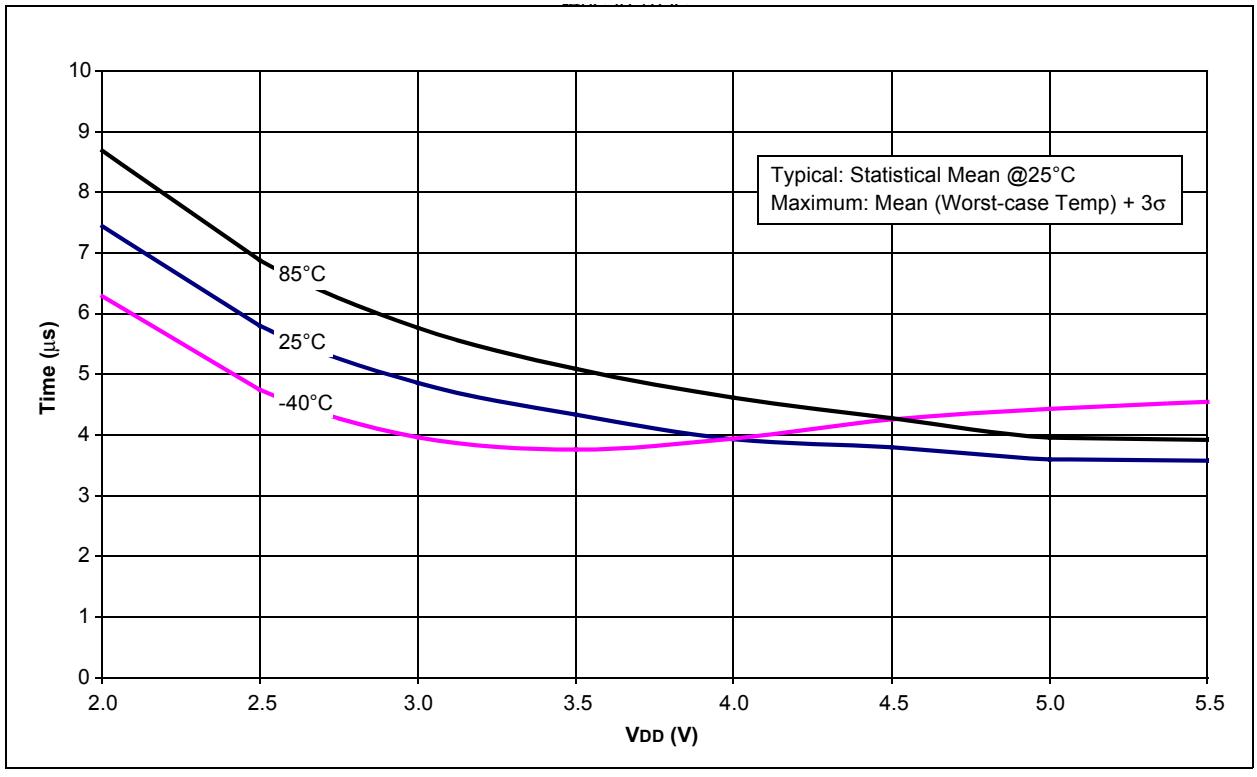


FIGURE 20-37: MINIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE



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