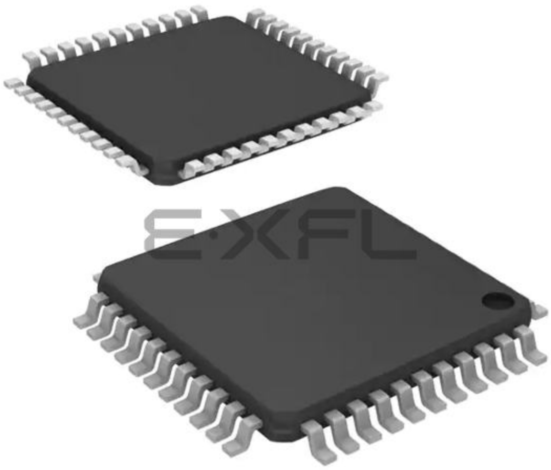


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f917t-i-pt

FIGURE 1-3: PIC16F946 BLOCK DIAGRAM

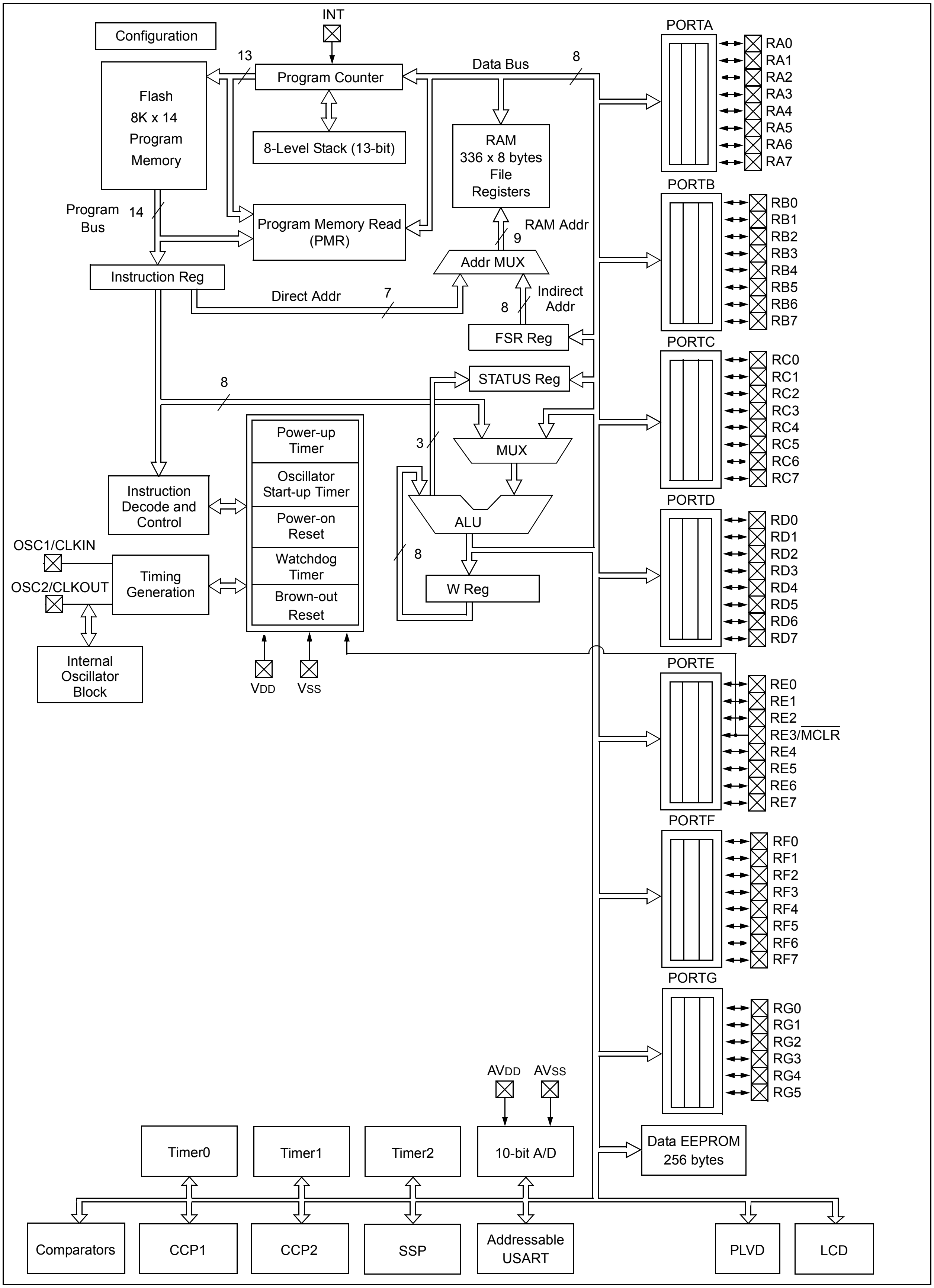


FIGURE 2-4: PIC16F914/917 SPECIAL FUNCTION REGISTERS

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr. (1)	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	LCDCON	107h		187h
PORTD	08h	TRISD	88h	LCDPS	108h		188h
PORTE	09h	TRISE	89h	LVDCON	109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATL	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADRL	10Dh	EECON2 (1)	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCTUNE	90h	LCDDATA0	110h	General Purpose Register (2) 96 Bytes	190h
TMR2	11h	ANSEL	91h	LCDDATA1	111h		
T2CON	12h	PR2	92h	LCDDATA2	112h		
SSPBUF	13h	SSPADD	93h	LCDDATA3	113h		
SSPCON	14h	SSPSTAT	94h	LCDDATA4	114h		
CCPR1L	15h	WPUB	95h	LCDDATA5	115h		
CCPR1H	16h	IOCB	96h	LCDDATA6	116h		
CCP1CON	17h	CMCON1	97h	LCDDATA7	117h		
RCSTA	18h	TXSTA	98h	LCDDATA8	118h		
TXREG	19h	SPBRG	99h	LCDDATA9	119h		
RCREG	1Ah		9Ah	LCDDATA10	11Ah		
CCPR2L	1Bh		9Bh	LCDDATA11	11Bh		
CCPR2H	1Ch	CMCON0	9Ch	LCDSE0	11Ch		
CCP2CON	1Dh	VRCON	9Dh	LCDSE1	11Dh		
ADRESH	1Eh	ADRESL	9Eh	LCDSE2	11Eh		
ADCON0	1Fh	ADCON1	9Fh		11Fh		
General Purpose Register 96 Bytes	20h	General Purpose Register 80 Bytes	A0h	General Purpose Register 80 Bytes	120h		
			EFh		16Fh		1EFh
		accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h	accesses 70h-7Fh	1F0h
	7Fh		FFh		17Fh		1FFh

Bank 0 | Bank 1 | Bank 2 | Bank 3

▢ Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: On the PIC16F914, unimplemented data memory locations, read as '0'.

3.0 I/O PORTS

The PIC16F913/914/916/917/946 family of devices includes several 8-bit PORT registers along with their corresponding TRIS registers and one four bit port:

- PORTA and TRISA
- PORTB and TRISB
- PORTC and TRISC
- PORTD and TRISD(1)
- PORTE and TRISE
- PORTF and TRISF(2)
- PORTG and TRISG(2)

Note 1:	PIC16F914/917 and PIC16F946 only.
2:	PIC16F946 only

PORTA, PORTB, PORTC and RE3/$\overline{\text{MCLR}}$/V_{PP} are implemented on all devices. PORTD and RE<2:0> (PORTE) are implemented only on the PIC16F914/917 and PIC16F946. RE<7:4> (PORTE), PORTF and PORTG are implemented only on the PIC16F946.

3.1 ANSEL Register

The ANSEL register (Register 3-1) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSEL bit high will cause all digital reads on the pin to be read as ‘0’ and allow analog functions on the pin to operate correctly.

The state of the ANSEL bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

REGISTER 3-1: ANSEL: ANALOG SELECT REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7(2)	ANS6(2)	ANS5(2)	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **ANS<7:0>**: Analog Select bits
Analog select between analog or digital function on pins AN<7:0>, respectively.
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

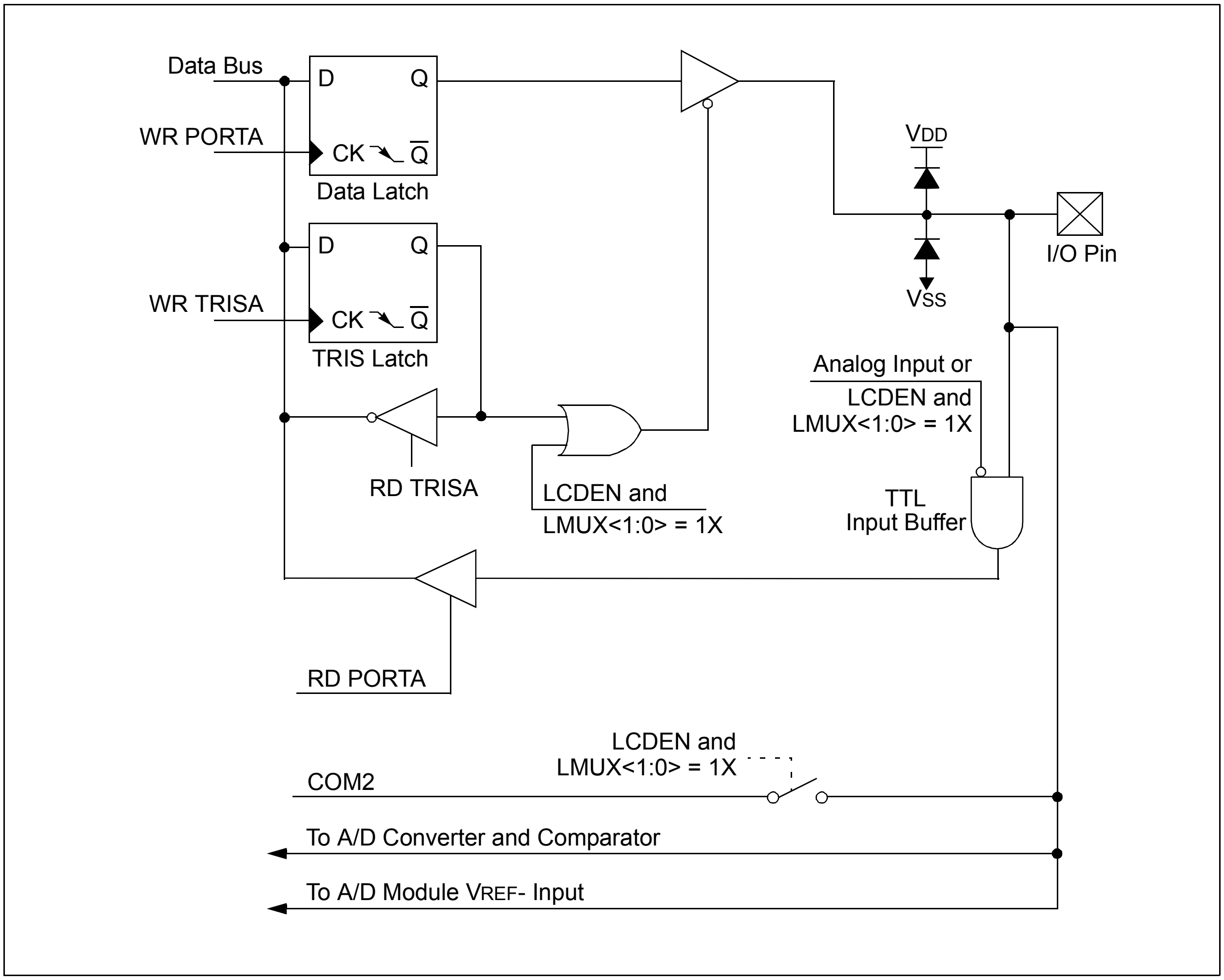
2: PIC16F914/PIC16F917/PIC16F946 only.

3.2.1.3 RA2/AN2/C2+/VREF-/COM2

Figure 3-3 shows the diagram for this pin. The RA2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog input for Comparator C2
- a voltage reference input for the ADC
- an analog output for the LCD

FIGURE 3-3: BLOCK DIAGRAM OF RA2

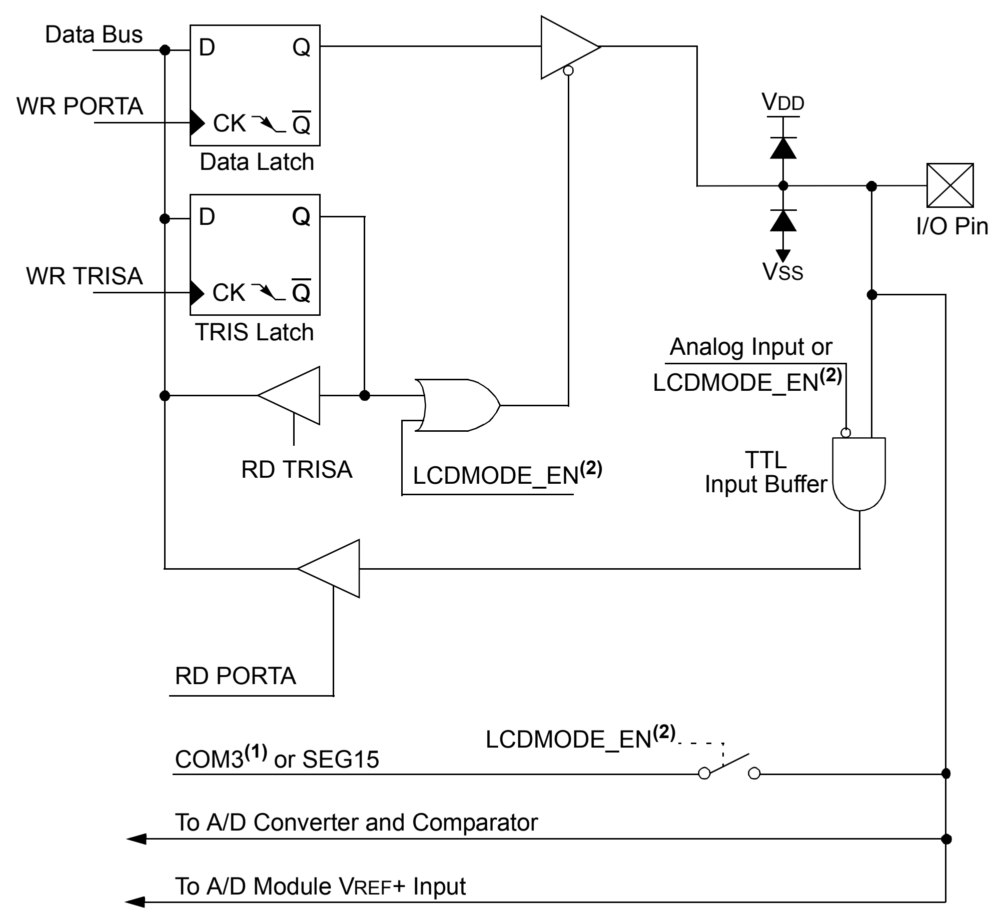


3.2.1.4 RA3/AN3/C1+/VREF+/COM3/SEG15

Figure 3-4 shows the diagram for this pin. The RA3 pin is configurable to function as one of the following:

- a general purpose input
- an analog input for the ADC
- an analog input from Comparator C1
- a voltage reference input for the ADC
- analog outputs for the LCD

FIGURE 3-4: BLOCK DIAGRAM OF RA3



Note 1: PIC16F913/916 only.

2: For the PIC16F913/916, the LCDMODE_EN = LCDEN and (SE15 or LMUX<1:0> = 11). For the PIC16F914/917 and PIC16F946, the LCDMODE_EN = LCDEN and SE15.

3.5 PORTC and TRISC Registers

PORTC is an 8-bit bidirectional port. PORTC is multiplexed with several peripheral functions. PORTC pins have Schmitt Trigger input buffers.

All PORTC pins have latch bits (PORTC register). They will modify the contents of the PORTC latch (when written); thus, modifying the value driven out on a pin if the corresponding TRISC bit is configured for output.

EXAMPLE 3-3: INITIALIZING PORTC

```
BANKSEL PORTC    ;
CLRF    PORTC    ;Init PORTC
BANKSEL TRISC    ;
MOVLW   0FFh     ;Set RC<7:0> as inputs
MOVWF   TRISC    ;
BANKSEL LCDCON   ;
CLRF    LCDCON   ;Disable VLCD<3:1>
                 ;inputs on RC<2:0>
```

REGISTER 3-8: PORTC: PORTC REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **RC<7:0>**: PORTC I/O Pin bits
1 = Port pin is >V_{IH} min.
0 = Port pin is <V_{IL} max.

REGISTER 3-9: TRISC: PORTC TRI-STATE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **TRISC<7:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

FIGURE 3-26: BLOCK DIAGRAM OF RE<2:0> (PIC16F914/917 AND PIC16F946 ONLY)

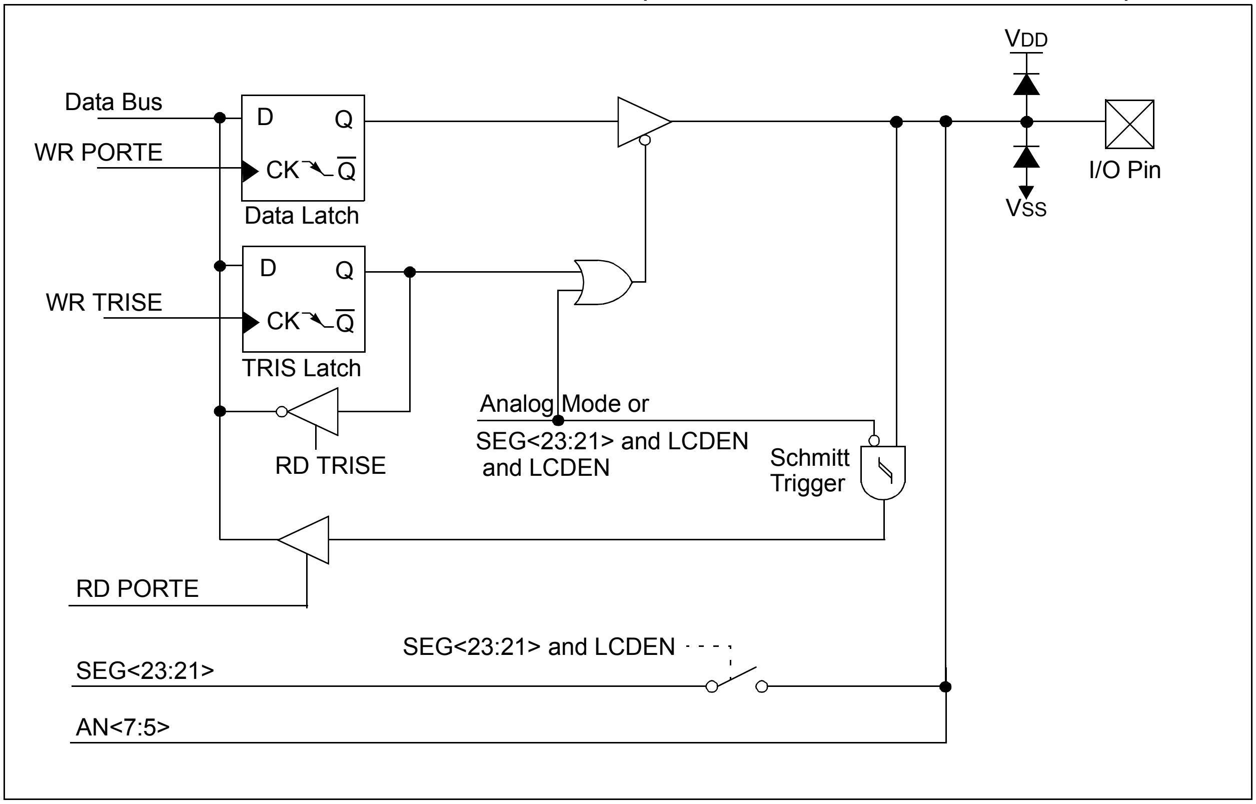
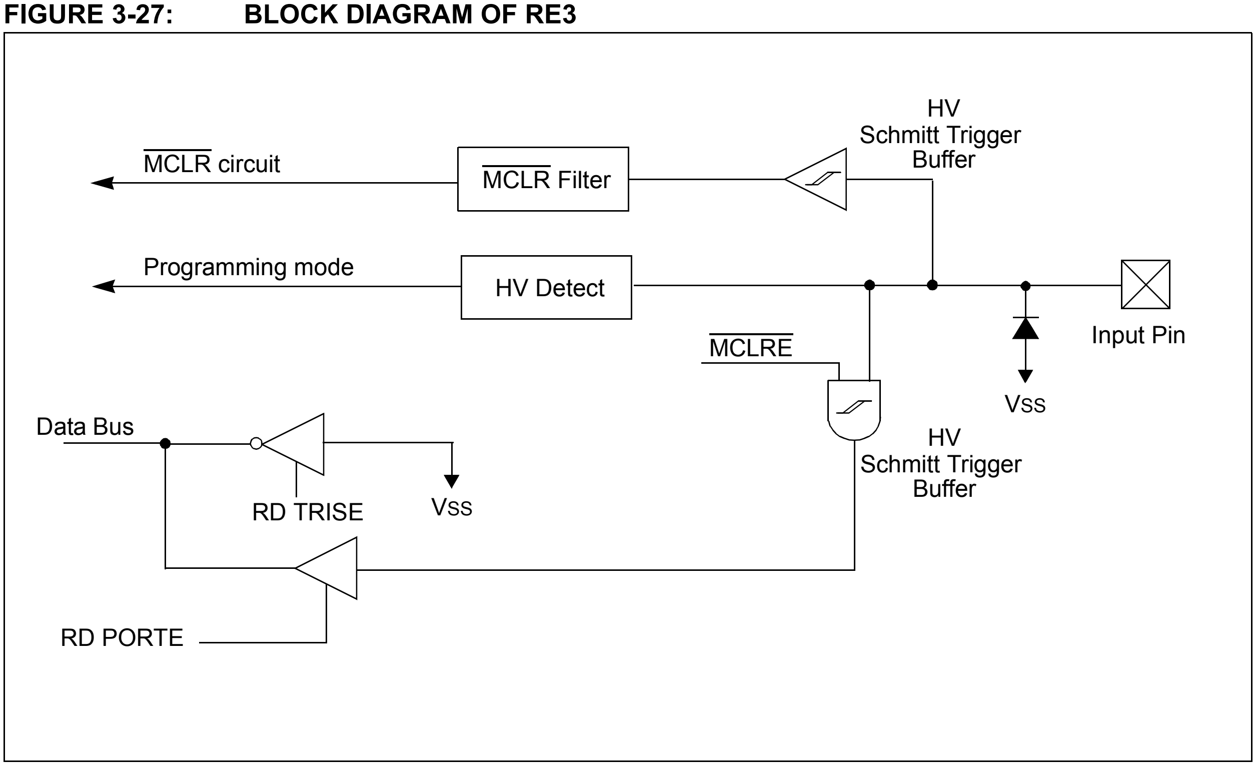


FIGURE 3-27: BLOCK DIAGRAM OF RE3



8.3 Comparator Control

The CMCON0 register (Register 8-1) provides access to the following comparator features:

- Mode selection
- Output state
- Output polarity
- Input switch

8.3.1 COMPARATOR OUTPUT STATE

Each comparator state can always be read internally via the associated CxOUT bit of the CMCON0 register. The comparator outputs are directed to the CxOUT pins when CM<2:0> = `110`. When this mode is selected, the TRIS bits for the associated CxOUT pins must be cleared to enable the output drivers.

8.3.2 COMPARATOR OUTPUT POLARITY

Inverting the output of a comparator is functionally equivalent to swapping the comparator inputs. The polarity of a comparator output can be inverted by setting the CxINV bits of the CMCON0 register. Clearing CxINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 8-1.

TABLE 8-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CxINV	CxOUT
$V_{IN-} > V_{IN+}$	0	0
$V_{IN-} < V_{IN+}$	0	1
$V_{IN-} > V_{IN+}$	1	1
$V_{IN-} < V_{IN+}$	1	0

Note: CxOUT refers to both the register bit and output pin.

8.3.3 COMPARATOR INPUT SWITCH

The inverting input of the comparators may be switched between two analog pins or an analog input pin and and the fixed voltage reference in the following modes:

- CM<2:0> = `001` (Comparator C1 only)
- CM<2:0> = `010` (Comparators C1 and C2)
- CM<2:0> = `101` (Comparator C2 only)

In the above modes, both pins remain in Analog mode regardless of which pin is selected as the input. The CIS bit of the CMCON0 register controls the comparator input switch.

8.4 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in **Section 19.0 "Electrical Specifications"** for more details.

8.5 Comparator Interrupt Operation

The comparator interrupt flag is set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 8-2 and Figure 8-3). One latch is updated with the comparator output level when the CMCON0 register is read. This latch retains the value until the next read of the CMCON0 register or the occurrence of a Reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. The mismatch condition will persist, holding the CxIF bit of the PIR2 register true, until either the CMCON0 register is read or the comparator output returns to the previous state.

Note:	A write operation to the CMCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.

Software will need to maintain information about the status of the comparator output to determine the actual change that has occurred.

The CxIF bit of the PIR2 register is the comparator interrupt flag. This bit must be reset in software by clearing it to '`0`'. Since it is also possible to write a '`1`' to this register, a simulated interrupt may be initiated.

The CxIE bit of the PIE2 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CxIF bit of the PIR2 register will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON0. This will end the mismatch condition. See Figures 8-6 and 8-7

b) Clear the CxIF interrupt flag.

A persistent mismatch condition will preclude clearing the CxIF interrupt flag. Reading CMCON0 will end the mismatch condition and allow the CxIF bit to be cleared.

9.0 ADDRESSABLE UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (AUSART)

The Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The AUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The AUSART module includes the following capabilities:

- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Sleep operation

Block diagrams of the AUSART transmitter and receiver are shown in Figure 9-1 and Figure 9-2.

FIGURE 9-1: AUSART TRANSMIT BLOCK DIAGRAM

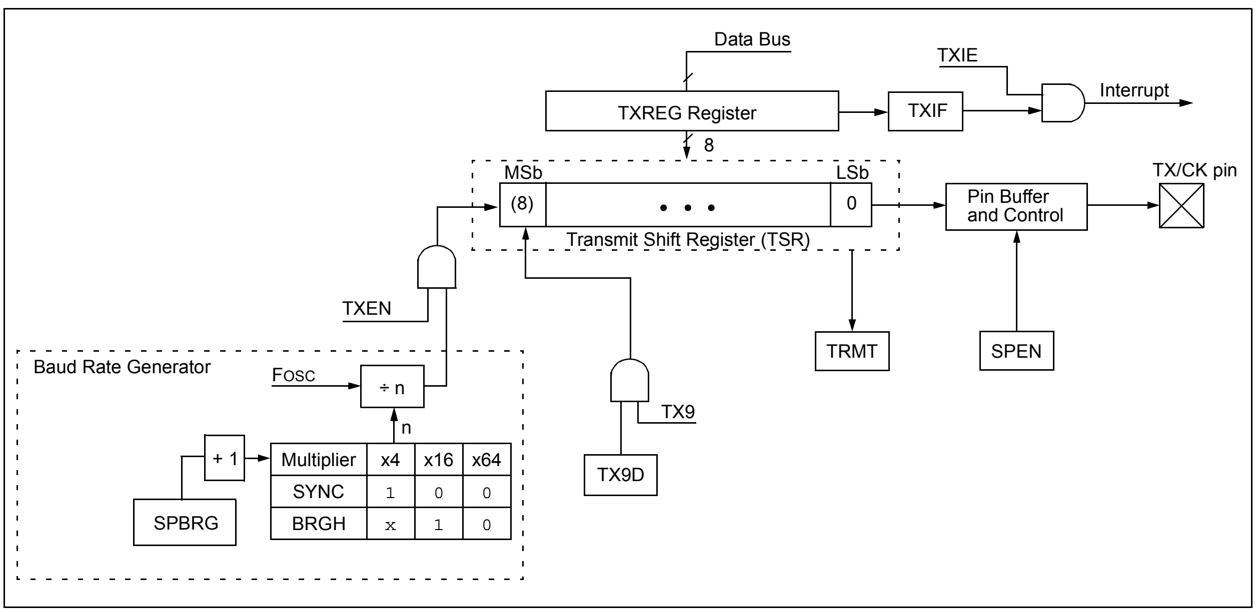
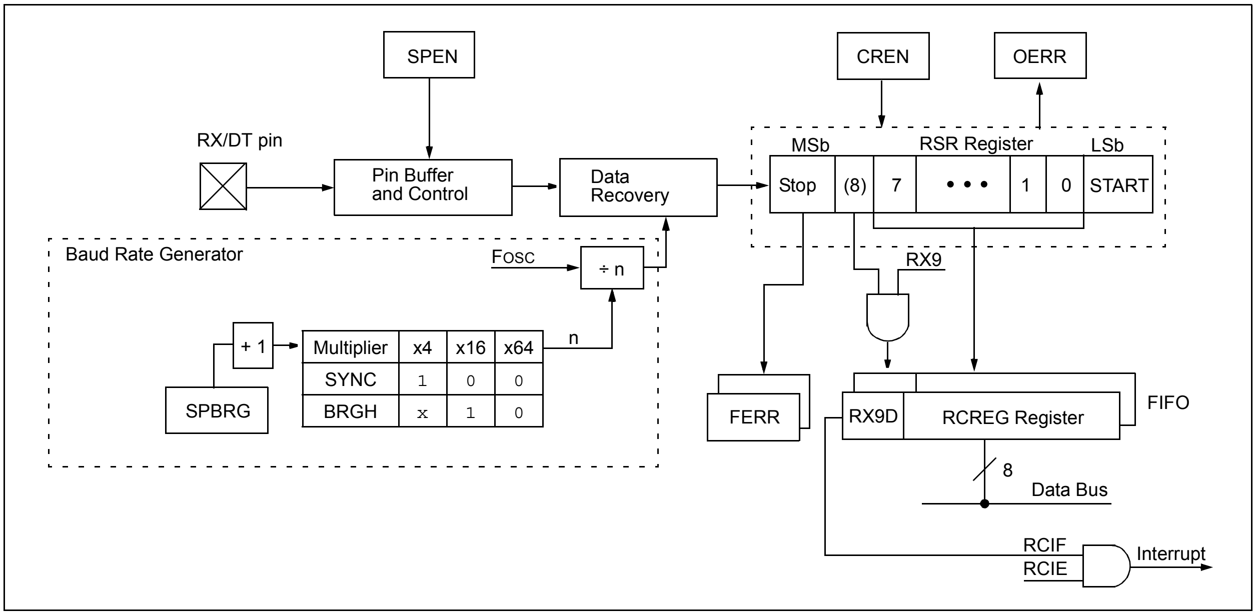


FIGURE 9-2: AUSART RECEIVE BLOCK DIAGRAM



The operation of the AUSART module is controlled through two registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)

These registers are detailed in Register 9-1 and Register 9-2 respectively.

9.3.2.3 AUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (**Section 9.3.1.4 "Synchronous Master Reception"**), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never Idle
- SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE interrupt enable bit of the PIE1 register is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

9.3.2.4 Synchronous Slave Reception Set-up:

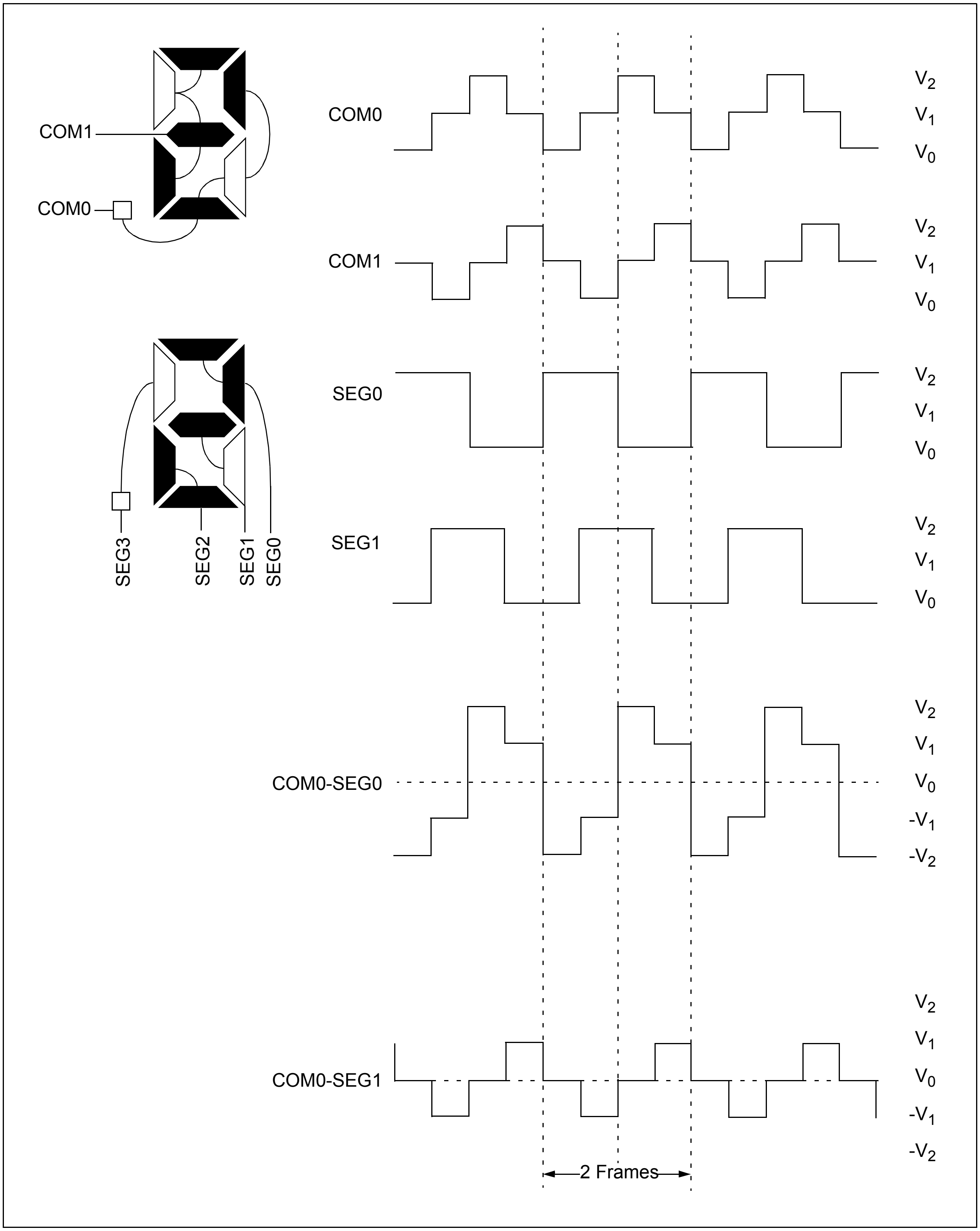
1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
3. If 9-bit reception is desired, set the RX9 bit.
4. Verify address detection is disabled by clearing the ADDEN bit of the RCSTA register.
5. Set the CREN bit to enable reception.
6. The RCIF bit of the PIR1 register will be set when reception is complete. An interrupt will be generated if the RCIE bit of the PIE1 register was set.
7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
8. Retrieve the 8 Least Significant bits from the receive FIFO by reading the RCREG register.
9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register.

TABLE 9-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
LCDCON	LCDEN	$\overline{\text{SLPEN}}$	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	0000 0000	0000 0000
PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCREG	AUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	0000 000X
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Reception.

FIGURE 10-8: TYPE-B WAVEFORMS IN 1/2 MUX, 1/2 BIAS DRIVE



REGISTER 14-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **SMP**: SPI Data Input Sample Phase bit
SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time (Microwire)
SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode
I²C™ mode:
This bit must be maintained clear

bit 6 **CKE**: SPI Clock Edge Select bit
SPI mode, CKP = 0:
1 = Data stable on rising edge of SCK (Microwire alternate)
0 = Data stable on falling edge of SCK
SPI mode, CKP = 1:
1 = Data stable on falling edge of SCK (Microwire default)
0 = Data stable on rising edge of SCK
I²C mode:
This bit must be maintained clear

bit 5 **D/$\overline{A}$**: DATA/$\overline{ADDRESS}$ bit (I²C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P**: Stop bit (I²C mode only)
This bit is cleared when the SSP module is disabled, or when the Start bit is detected last.
SSPEN is cleared.
1 = Indicates that a Stop bit has been detected last (this bit is ‘0’ on Reset)
0 = Stop bit was not detected last

bit 3 **S**: Start bit (I²C mode only)
This bit is cleared when the SSP module is disabled, or when the Stop bit is detected last.
SSPEN is cleared.
1 = Indicates that a Start bit has been detected last (this bit is ‘0’ on Reset)
0 = Start bit was not detected last

bit 2 **R/$\overline{W}$**: READ/$\overline{WRITE}$ bit Information (I²C mode only)
This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or $\overline{ACK}$ bit.
1 = Read
0 = Write

bit 1 **UA**: Update Address bit (10-bit I²C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0 **BF**: Buffer Full Status bit
Receive (SPI and I²C modes):
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty
Transmit (I²C mode only):
1 = Transmit in progress, SSPBUF is full
0 = Transmit complete, SSPBUF is empty

16.2.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register selects one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = `01`, the SBOREN bit of the PCON register enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 16-1 for the Configuration Word definition.

If VDD falls below VBOR for greater than parameter (TBOR) (see **Section 19.0 "Electrical Specifications"**), the Brown-out situation will reset the device. This will occur regardless of VDD slew rate. A Reset is not insured to occur if VDD falls below VBOR for less than parameter (TBOR).

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 16-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional 64 ms.

Note:	The Power-up Timer is enabled by the $\overline{\text{PWRTE}}$ bit in the Configuration Word.

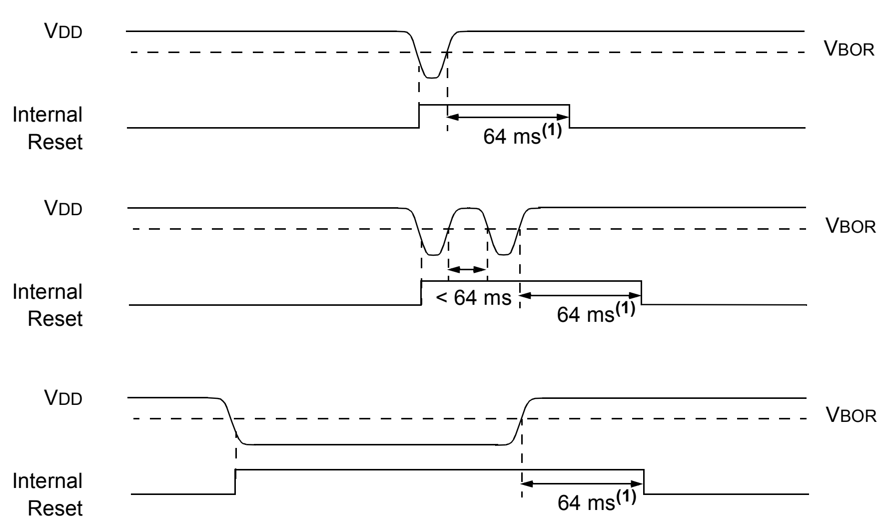
If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

16.2.5 BOR CALIBRATION

The PIC16F91X/946 stores the BOR calibration values in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the "*PIC16F91X/946 Memory Programming Specification"* (DS41244) and thus, does not require reprogramming.

Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F91X/946 Memory Programming Specification"* (DS41244) for more information.

FIGURE 16-3: BROWN-OUT SITUATIONS



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '`0`'.

TABLE 16-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset	• MCLR Reset • WDT Reset • Brown-out Reset(1)	• Wake-up from Sleep through interrupt • Wake-up from Sleep through WDT time-out
LCDDATA22(7)	19Ah	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA23(7)	19Bh	---- --xx	---- --uu	---- --uu
LCDSE3(7)	19Ch	0000 0000	uuuu uuuu	uuuu uuuu
LCDSE4(7)	19Dh	0000 0000	uuuu uuuu	uuuu uuuu
LCDSE5(7)	19Eh	---- --00	---- --uu	---- --uu
EECON1	18Ch	x--- x000	u--- q000	u--- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 16-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: PIC16F914/917 and PIC16F946 only.

7: PIC16F946 only.

TABLE 16-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	0001 1xxx	---1 --0x
MCLR Reset during normal operation	0000h	000u uuuu	---u --uu
MCLR Reset during Sleep	0000h	0001 0uuu	---u --uu
WDT Reset	0000h	0000 uuuu	---u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---u --uu
Brown-out Reset	0000h	0001 1uuu	---1 --10
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	---u --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

16.4 Watchdog Timer (WDT)

For PIC16F91X/946, the WDT has been modified from previous PIC16F devices. The new WDT is code and functionally compatible with previous PIC16F WDT modules and adds a 16-bit prescaler to the WDT. This allows the user to have a scaled value for the WDT and TMR0 at the same time. In addition, the WDT time-out value can be extended to 268 seconds. WDT is cleared under certain conditions described in Table 16-7.

16.4.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit does not reflect that the LFINTOSC is enabled.

The value of WDTCON is `‘---0 1000’` on all Resets. This gives a nominal time base of 16 ms, which is compatible with the time base generated with previous PIC16F microcontroller versions.

Note:	When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

A new prescaler has been added to the path between the INTOSC and the multiplexers used to select the path for the WDT. This prescaler is 16 bits and can be programmed to divide the INTOSC by 32 to 65536, giving the WDT a nominal range of 1 ms to 268s.

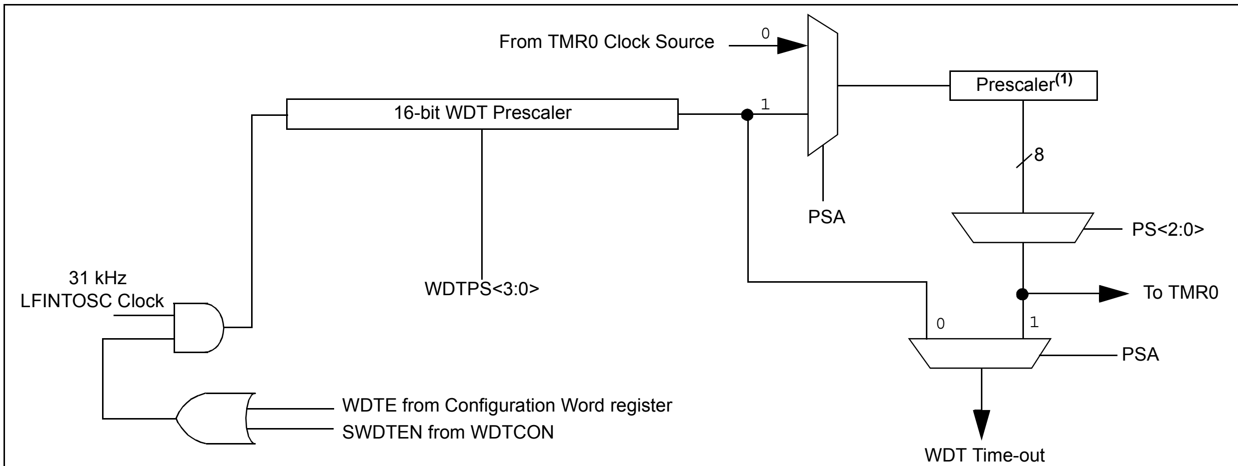
16.4.2 WDT CONTROL

The WDTE bit is located in the Configuration Word register. When set, the WDT runs continuously.

When the WDTE bit in the Configuration Word register is set, the SWDTEN bit of the WDTCON register has no effect. If WDTE is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits of the OPTION register have the same function as in previous versions of the PIC16F family of microcontrollers. See **Section 5.0 “Timer0 Module”** for more information.

FIGURE 16-9: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: This is the shared Timer0/WDT prescaler. See **Section 5.4 “Prescaler”** for more information.

TABLE 16-7: WDT STATUS

Conditions	WDT
WDTE = `0`	Cleared
`CLRWDT` Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

TABLE 17-2: PIC16F913/914/916/917/946 INSTRUCTION SET

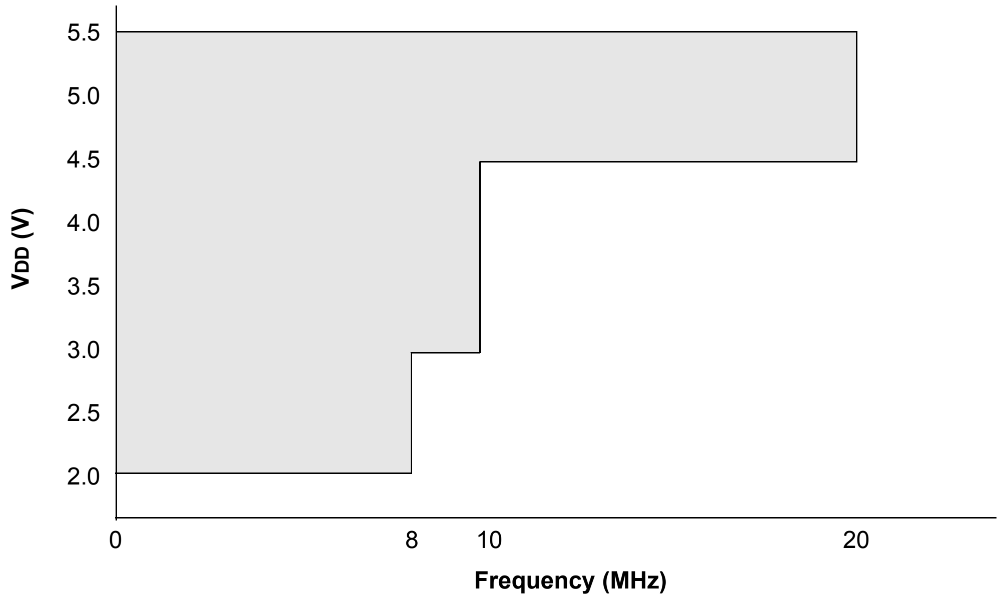
Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	**1, 2**
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	**1, 2**
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	**2**
CLRW	–	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	**1, 2**
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	**1, 2**
DECFSZ	f, d	Decrement f, Skip if 0	1**(2)**	00	1011	dfff	ffff		**1, 2, 3**
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	**1, 2**
INCFSZ	f, d	Increment f, Skip if 0	1**(2)**	00	1111	dfff	ffff		**1, 2, 3**
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	**1, 2**
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	**1, 2**
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	–	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	**1, 2**
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	**1, 2**
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	**1, 2**
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		**1, 2**
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	**1, 2**
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		**1, 2**
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		**1, 2**
BTFSC	f, b	Bit Test f, Skip if Clear	1 **(2)**	01	10bb	bfff	ffff		**3**
BTFSS	f, b	Bit Test f, Skip if Set	1 **(2)**	01	11bb	bfff	ffff		**3**
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	–	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	–	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	–	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	–	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF GPIO, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

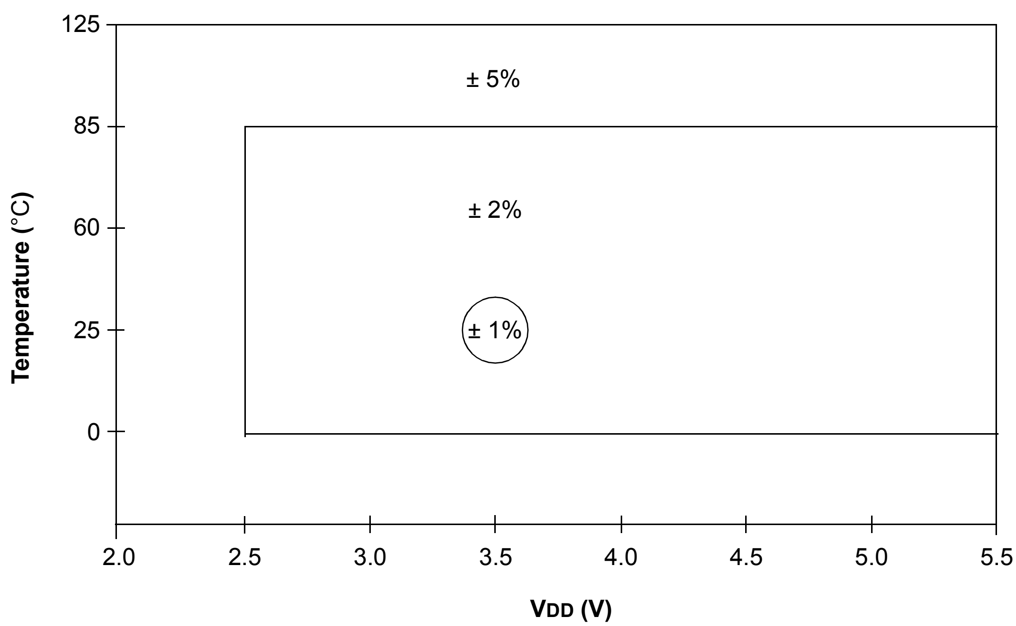
3: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

FIGURE 19-1: PIC16F913/914/916/917/946 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 19-2: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



MPLAB Integrated Development Environment Software .. 251
MPLAB PM3 Device Programmer 253
MPLAB REAL ICE In-Circuit Emulator System 253
MPLINK Object Linker/MPLIB Object Librarian 252

O

OPCODE Field Descriptions 241
OPTION Register 33
OPTION_REG Register 101
OSCCON Register 88
Oscillator
  Associated registers 98, 106
Oscillator Module 87
  EC 87
  HFINTOSC 87
  HS 87
  INTOSC 87
  INTOSCIO 87
  LFINTOSC 87
  LP 87
  RC 87
  RCIO 87
  XT 87
Oscillator Parameters 266
Oscillator Specifications 265
Oscillator Start-up Timer (OST)
  Specifications 269
Oscillator Switching
  Fail-Safe Clock Monitor 97
  Two-Speed Clock Start-up 95
OSCTUNE Register 92

P

P (Stop) bit 194
Packaging 305
  Marking 305, 306
  PDIP Details 307
Paging, Program Memory 40
PCL and PCLATH 40
  Computed GOTO 40
  Stack 40
PCON Register 39, 224
PICSTART Plus Development Programmer 254
PIE1 Register 35
PIE2 Register 36
Pin Diagram
  PIC16F913/916, 28-pin 4
  PIC16F914/917, 40-pin 2
  PIC16F914/917, 44-pin 7
  PIC16F946, 64-Pin 10
Pinout Description 18
PIR1 Register 37
PIR2 Register 38
PLVD
  Associated Registers 173
PORTA
  Additional Pin Functions
    ANSEL Register 43
  Associated Registers 52
  Pin Descriptions and Diagrams 45
  RA0 45
  RA1 46
  RA2 47
  RA3 48
  RA4 49
  RA5 50
  RA6 51
  RA7 52
  Registers 44
  Specifications 267
PORTA Register 44
PORTB
  Additional Pin Functions 53
    Weak Pull-up 53
  Associated Registers 61
  Interrupt-on-change 53
  Pin Descriptions and Diagrams 56
  RB0 56
  RB1 56
  RB2 56
  RB3 56
  RB4 57
  RB5 58
  RB6 59
  RB7 60
  Registers 53
PORTB Register 54
PORTC
  Associated Registers 70
  Pin Descriptions and Diagrams 63
  RC0 63
  RC1 63
  RC2 63
  RC3 65
  RC4 66
  RC5 67
  RC6 68
  RC7 69
  Registers 62
  Specifications 267
PORTC Register 62
PORTD
  Associated Registers 75
  Pin Descriptions and Diagrams 72
  RD0 72
  RD1 72
  RD2 72
  RD3 72
  RD4 72
  RD5 72
  RD6 72
  RD7 72
  Registers 71
PORTD Register 71
PORTE
  Associated Registers 80
  Pin Descriptions and Diagrams 77
  RE0 77
  RE1 77
  RE2 77
  RE3 77
  RE4 77
  RE5 77
  RE6 77
  RE7 77
  Registers 76
PORTE Register 76
PORTF
  Associated Registers 83
  Pin Descriptions and Diagrams 82
  Registers 81

Registers ... 62
TRISC Register ... 62
TRISD
Registers ... 71
TRISD Register ... 71
TRISE
Registers ... 76
TRISE Register ... 76
TRISF
Registers ... 81
TRISF Register ... 81
TRISG
Registers ... 84
TRISG Register ... 84
Two-Speed Clock Start-up Mode ... 95
TXREG ... 123
TXSTA Register ... 130
BRGH Bit ... 132

U

UA ... 194
Update Address bit, UA ... 194
USART
Synchronous Master Mode
Requirements, Synchronous Receive ... 275
Requirements, Synchronous Transmission ... 275
Timing Diagram, Synchronous Receive ... 275
Timing Diagram, Synchronous Transmission ... 275

V

Voltage Reference. *See* Comparator Voltage Reference (CVREF)
Voltage References
Associated registers ... 119
VREF. *SEE* ADC Reference Voltage

W

Wake-up Using Interrupts ... 236
Watchdog Timer (WDT) ... 234
Associated Registers ... 235
Clock Source ... 234
Modes ... 234
Period ... 234
Specifications ... 269
WCOL bit ... 195
WDTCON Register ... 235
WPUB Register ... 55
Write Collision Detect bit (WCOL) ... 195
WWW Address ... 325
WWW, On-Line Support ... 13