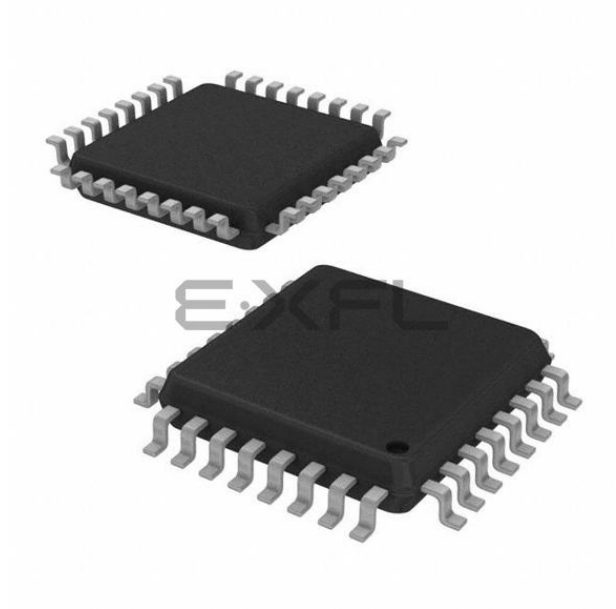

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8014mfae

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1.4 Architecture Block Diagram

The 56F8014's architecture is shown in **Figure 1-1**, **Figure 1-2**, and **Figure 1-3**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge, as well as showing the internal connections between each unit of the 56800E core. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. **Figure 1-3** details how the device's I/O pins are muxed. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2 Signal/Connection Descriptions** to see which signals are multiplexed with those of other peripherals.

1.5 Synchronize ADC with PWM

ADC conversion can be synchronized with the PWM module via Quad Timer channel 2 and 3 if needed. Internally, the PWM synch signal — which is generated at every PWM reload —can be connected to the timer channel 3 input, and the timer channel 2 and channel 3 outputs are connected to the ADC sync inputs. Timer channel 3 output is connected to SYNC0 and timer channel 2 is connected to SYNC1. The setting is controlled by the TC3_INP bit in the SIM Control Register; see **Section 6.3.1**.

SYNC0 is the master ADC sync input, used to trigger both ADCA and ADCB in sequence and parallel mode. SYNC1 is used to trigger ADCB in parallel independent mode, while SYNC0 is used to trigger ADCA. See *MC56F8000RM*, the 56F801X Peripheral Reference Manual, for additional information.

1.6 Multiple Frequency PWM Output

When both PWM channels of a complementary pair in software control mode and software control bits are set to 1, each complementary PWM signal pair — PWM 0 and 1; PWM 2 and 3; and PWM 4 and 5 — can select a PWM source from one of the following sources. This will enable each PWM pair and PWM2 to output PWM signals at different frequencies.

- External GPIO input:
  - GPIOB2 input can be used to drive PWM 0 and 1
  - GPIOB3 input can be used to drive PWM 2
  - GPIOB4 input can be used to drive PWM 4 and 5
- Quad Timer output:
  - Timer0 output can be used to drive PWM 0 and 1
  - Timer2 output can be used to drive PWM 2
  - Timer3 output can be used to drive PWM 4 and 5
- ADC conversion result:
  - Signal of over/under limit of ADC sample 0 can be used to drive PWM 0 and 1
  - Signal of over/under limit of ADC sample 1 can be used to drive PWM 2

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8014 are organized into functional groups, as detailed in **Table 2-1**. **Table 2-2** summarizes all device pins. In **Table 2-2**, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD} or V_{DDA})	2
Ground (V_{SS} or V_{SSA})	3
Supply Capacitors	1
Reset	1
Pulse Width Modulator (PWM) Ports[1]	5
Serial Peripheral Interface (SPI) Ports[2]	4
Analog-to-Digital Converter (ADC) Ports	8
Timer Module Ports[3]	2
Serial Communications Interface (SCI) Ports[4]	2
JTAG/Enhanced On-Chip Emulation (EOnCE)	4

1. Pins in this section can function as TMR and GPIO.
2. Pins in this section can function as TMR, I^2C, and GPIO.
3. Pins can function as PWM and GPIO.
4. Pins in this section can function as I^2C and GPIO.

Part 3 OCCS

3.1 Overview

This module provides the system clock, which uses it to generate the various chip clocks. This module also produces the oscillator clock signals, plus the ADC clock and high-speed peripheral clock.

The on-chip clock synthesis module allows product design using an internal relaxation oscillator to run 56F801X family parts at user-selectable frequencies up to 32MHz.

3.2 Features

The On-Chip Clock Synthesis (OCCS) module interfaces to the oscillator and PLL. The OCCS module features:

- Internal relaxation oscillator
- Ability to power down the internal relaxation oscillator
- Ability to put the internal relaxation oscillator into a standby mode
- 3-bit postscaler provides control for the PLL output
- Ability to power down the internal PLL
- Provides 2X system clock frequency, which operates at twice the system clock, to the System Integration Module (SIM) that is used to generate the various device clocks
- Provides 3X system clock, which operates at three times the system clock, to PWM and Timer
- Safety shutdown feature is available in the event that the PLL reference clock disappears
- Can be driven from an external clock source

The clock generation module provides the programming interface for both the PLL and internal relaxation oscillator.

3.3 Operating Modes

In 56F801X family parts, either an internal oscillator or an external frequency source can be used to provide a reference clock to the SIM.

The 2X system clock source output from the OCCS can be described by one of the following equations:

2X system frequency = oscillator frequency

2X system frequency = (oscillator frequency X 8) / (postscaler)

where:

postscaler = 1, 2, 4, 8, 16, or 32 PLL output divider

The SIM is responsible for further dividing these frequencies by two, which will insure a 50% duty cycle in the system clock output.

4.4 Data Map

Table 4-4 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:$FF FFFF X:$FF FF00	EOnCE 256 locations allocated
X:$FF FEFF X:$01 0000	RESERVED
X:$00 FFFF X:$00 F000	On-Chip Peripherals 4096 locations allocated
X:$00 EFFF X:$00 8800	RESERVED
X:$00 EFFF X:$00 0800	Reserved
X:$00 7FFF X:$00 0040	RESERVED
X:$00 07FF X:$00 0000	On-Chip Data RAM[2] 4KB

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Program space starting at P: $00 8000; see Figure 4-1.

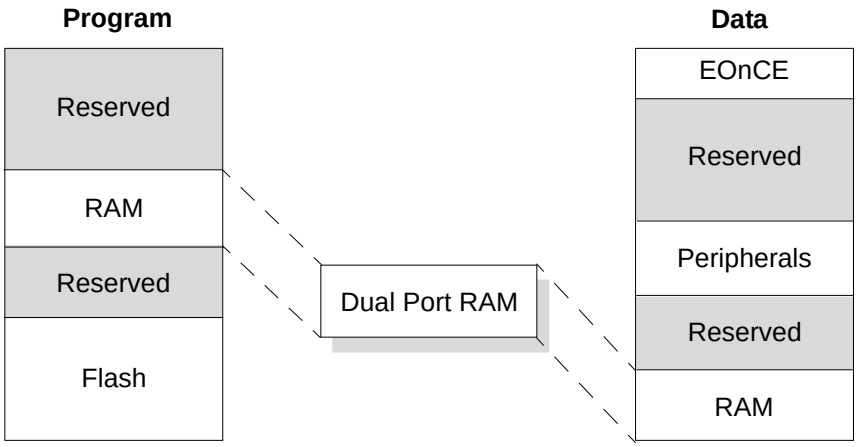


Figure 4-1 Dual Port RAM

4.5 EOnCE Memory Map

Figure 4-5 lists all EOnCE registers necessary to access or control the EOnCE.

Table 4-8 Pulse Width Modulator Registers Address Map (PWM_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
PWM_CTRL	$0	Control Register
PWM_FCTRL	$1	Fault Control Register
PWM_FLTACK	$2	Fault Status Acknowledge Register
PWM_OUT	$3	Output Control Register
PWM_CNTR	$4	Counter Register
PWM_CMOD	$5	Counter Modulo Register
PWM_VAL0	$6	Value Register 0
PWM_VAL1	$7	Value Register 1
PWM_VAL2	$8	Value Register 2
PWM_VAL3	$9	Value Register 3
PWM_VAL4	$A	Value Register 4
PWM_VAL5	$B	Value Register 5
PWM_DTIM0	$C	Dead Time Register 0
PWM_DTIM1	$D	Dead Time Register 1
PWM_DMAP1	$E	Disable Mapping Register 1
PWM_DMAP2	$F	Disable Mapping Register 2
PWM_CNFG	$10	Configure Register
PWM_CCTRL	$11	Channel Control Register
PWM_PORT	$12	Port Register
PWM_ICCTRL	$13	Internal Correction Control Register
PWM_SCTRL	$14	Source Control Register

Table 4-9 Interrupt Control Registers Address Map (ITCN_BASE = $00 F060)

Register Acronym	Address Offset	Register Description
ITCN_IPR0	$0	Interrupt Priority Register 0
ITCN_IPR1	$1	Interrupt Priority Register 1
ITCN_IPR2	$2	Interrupt Priority Register 2
ITCN_IPR3	$3	Interrupt Priority Register 3
ITCN_IPR4	$4	Interrupt Priority Register 4
ITCN_VBA	$5	Vector Base Address Register
ITCN_FIM0	$6	Fast Interrupt Match 0 Register
ITCN_FIVAL0	$7	Fast Interrupt Vector Address Low 0 Register
ITCN_FIVAH0	$8	Fast Interrupt Vector Address High 0 Register

5.5.3.4 SCI Transmitter Idle Interrupt Priority Level (SCI_TIDL IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.3.5 SCI Transmitter Empty Interrupt Priority Level (SCI_XMIT IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.3.6 SPI Transmitter Empty Interrupt Priority Level (SPI_XMIT IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.3.7 SPI Receiver Full Interrupt Priority Level (SPI_RCV IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

- SW Interrupt 0
- SW Interrupt LP

These interrupts are enabled at their fixed priority levels.

Part 6 System Integration Module (SIM)

6.1 Introduction

The SIM module is a system catchall for the glue logic that ties together the system-on-chip. It controls distribution of resets and clocks and provides a number of control features. The System Integration Module is responsible for the following functions:

- Reset sequencing
- Clock control & distribution
- Stop/Wait control
- System status registers
- Registers for software access to the JTAG ID of the chip
- Test registers
- Power control
- I/O pad multiplexing

These are discussed in more detail in the sections that follow.

6.2 Features

The SIM has the following features:

- Reset sequencing
  - Core and Peripheral Clock control & distribution
  - Stop/Wait mode control
  - System status
  - Power control
  - Control I/O multiplexing
- System bus clocks with pipeline hold-off support
- System clocks for non-pipelined interfaces
- Peripheral clocks for Quad Timer and PWM with high-speed (3X) option
- Power-saving clock gating for peripherals
- Three power modes (Run, Wait, Stop) to control power utilization
  - Stop mode shuts down the 56800E core, system clock, and peripheral clock
  - Wait mode shuts down the 56800E core and unnecessary system clock operation
  - Run mode supports full part operation
- Controls, with write protection, the enable/disable of 56800E core WAIT and STOP instructions

Table 6-3 Clock Operation in Power-Down Modes (Continued)

Mode	Core Clocks	Peripheral Clocks	Description
Wait	Core and memory clocks disabled	Peripheral clocks enabled	Core executes WAIT instruction to enter this mode. Typically used for power-conscious applications. Possible recoveries from Wait mode to Run mode are: 1. Any interrupt 2. Executing a Debug mode entry command during the 56800E core JTAG interface 2. Any reset (POR, external, software, COP)
Stop	Master clock generation in the OCCS remains operational, but the SIM disables the generation of system and peripheral clocks.		Core executes STOP instruction to enter this mode. Possible recoveries from Stop mode to Run mode are: 1. Interrupt from Timer channels that have been configured to operate in Stop mode (TCx_SD) 2. Interrupt for SCI configured to operate in Stop mode (SCI_SD) 3. Low-voltage interrupt 4. Executing a Debug mode entry command using the 56800E core JTAG interface 5. Any reset (POR, external, software, COP)
Standby	The OCCS generates the 2x System Clock at a reduced frequency (200 kHz). The PLL and high speed peripheral clocks are disabled and the high-speed peripheral option is not available. System and peripheral clocks operate at 100 kHz.		The user configures the OCCS and SIM to select the relaxation oscillator clock source (PRECS), shut down the PLL (PLLPD), put the relaxation oscillator in Standby mode (ROSB), and put the large regulator in Standby (LRSTDBY). The part is fully operational, but operating at a minimum frequency and power configuration. Recovery requires reversing the sequence used to enter this mode (allowing for PLL lock time).
Power-Down	Master clock generation in the OCCS is completely shut down. All system and peripheral clocks are disabled.		The user configures the OCCS and SIM to enter Standby mode as shown in the previous description, followed by powering down the oscillator (ROPD). The only possible recoveries from this mode are: 1. External reset 2. Power-on reset

The power modes provide additional means to disable clock domains, configure the voltage regulator, and configure clock generation to manage power utilization, as shown in **Table 6-3**. Run, Wait, and Stop modes provide means of enabling/disabling the peripheral and/or core clocking as a group. Stop disable controls are provided for selected peripherals in the control register so that these peripheral clocks can optionally continue to operate in Stop mode and generate interrupts which will return the part from Stop to Run mode. Standby mode provides normal operation but at very low speed and power utilization. It is possible to invoke Stop or Wait mode while in Standby mode for even greater levels of power reduction. A 200 kHz clock external clock can optionally be used in Standby mode to produce the required Standby 100 kHz system bus rate. Power-down mode, which selects the ROSC clock source but shuts it off, fully disables the part and minimizes its power utilization but is only recoverable via reset.

When the PLL is not selected and the system bus is operating at around 100 kHz, the large regulator can

be put into its Standby mode (LRSTDBY) to reduce the power utilization of that regulator.

All peripherals, except the COP/watchdog timer, run at the system clock (peripheral bus) frequency[1], which is the same as the main processor frequency in this architecture. The COP timer runs at MSTR_OSC / 1024. The maximum frequency of operation is SYS_CLK = 32MHz. The only exception is the Quad Timer and PWM, which can be configured to operate at three times the system bus rate using TCR and PCR controls, provided the PLL is active and selected.

6.6 Resets

The SIM supports four sources of reset, as shown in **Figure 6-15**. The two asynchronous sources are the external reset pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself by writing the SIM_CTRL register in **Section 6.3.1**, and the COP reset. The SIM uses these to generate resets for the internal logic. These are outlined in **Table 6-4**. The first column lists the four primary resets which are calculated. The JTAG circuitry is reset by the Power-On Reset. Columns two through five indicate which reset sources trigger these reset signals. The last column provides additional detail.

Table 6-4 Primary System Resets

	Reset Sources				
Reset Signal	**POR**	**External**	**Software**	**COP**	**Comments**
EXTENDED_POR	X				Stretched version of $\overline{\text{POR}}$. Relevant 64 Relaxation Oscillator Clock cycles after $\overline{\text{POR}}$ deasserts.
CLKGEN_RST	X	X	X	X	Released 32 Relaxation Oscillator Clock cycles after all reset sources have released.
PERIP_RST	X	X	X	X	Releases 32 Relaxation Oscillator Clock cycles after the CLKGEN_$\overline{\text{RST}}$ is released.
CORE_RST	X	X	X	X	Releases 32 SYS_CLK periods after PERIP_$\overline{\text{RST}}$ is released.

Figure 6-15 provides a graphic illustration of the details in **Table 6-4**. Note that the POR_Delay blocks use the Relaxation Oscillator Clock as their time base since other system clocks are inactive during this phase of reset.

1. The Quad Timer and PWM modules can be operated at three times the IPBus clock frequency.

in order to return to normal unsecured operation. Power-on reset will also reset both.

The user is responsible for directing the device to invoke the flash programming subroutine to reprogram the word $0000 into program memory location $00 1FF7. This is done by, for example, toggling a specific pin, or by downloading a user-defined key through serial interfaces.

Note: Flash contents can only be programmed for 1s to 0s.

7.3 Product Analysis

The recommended method of unsecuring a secured device for product analysis of field failures is via the method suggested in section 7.2.4. The customer would need to supply Technical Support with the details of the protocol to access the subroutines in flash. An alternative method for performing analysis on a secured device would be to mass-erase and reprogram the flash with the original code, but also either modify the security word or else not program the security word.

Part 8 General Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F801X Peripheral Reference Manual** and contains only chip-specific information. This information supercedes the generic information in the **56F801X Peripheral Reference Manual**.

8.2 Configuration

There are four GPIO ports defined on the 56F8014. The width of each port, the associated peripheral and reset functions are shown in **Table 8-1**. The specific mapping of GPIO port pins is shown in **Table 8-2**.

Table 8-1 GPIO Ports Configuration

GPIO Port	Available Pins in 56F8014	Peripheral Function	Reset Function
A	6	PWM, Reset	GPIO, except GPIOA7
B	8	SPI, SCI, Timer	GPIO
C	8	ADC	Analog
D	4	JTAG	JTAG

Table 8-2 GPIO External Signals Map (Continued)
Pins in shaded rows are not available in 56F8014

GPIO Function	Peripheral Function	LQFP Package Pin	Notes
GPIOB6	RXD / SDA / CLKIN	32	SIM register SIM_GPS is used to select between RXD and SDA. CLKIN functionality is enabled using the PLL Control Register within the OCCS block. Defaults to B6
GPIOB7	TXD / SCL	2	SIM register SIM_GPS is used to select between TXD and SCL Defaults to B7
GPIOC0	ANA0	13	Defaults to ANA0
GPIOC1	ANA1	12	Defaults to ANA1
GPIOC2	ANA2 / V_{REFH}	11	Defaults to ANA2
GPIOC3	ANA3	10	Defaults to ANA3
GPIOC4	ANB0	4	Defaults to ANB0
GPIOC5	ANB1	5	Defaults to ANB1
GPIOC6	ANB2 / V_{REFL}	6	Defaults to ANB2
GPIOC7	ANB3	7	Defaults to ANB3
GPIOD0	TDI	29	Defaults to TDI
GPIOD1	TDO	31	Defaults to TDO
GPIOD2	TCK	15	Defaults to TCK
GPIOD3	TMS	30	Defaults to TMS

8.3 Reset Values

Tables **4-16** through **4-19** detail registers for the 56F8014; Figures **8-1** through **8-4** summarize register maps and reset values.

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOD_PUPEN	R	0	0	0	0	0	0	0	0	0	0	0	0	PU			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$1	GPIOD_DATA	R	0	0	0	0	0	0	0	0	0	0	0	0	D			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOD_DDIR	R	0	0	0	0	0	0	0	0	0	0	0	0	DD			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOD_PEREN	R	0	0	0	0	0	0	0	0	0	0	0	0	PE			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$4	GPIOD_IASSRT	R	0	0	0	0	0	0	0	0	0	0	0	0	IA			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOD_IEN	R	0	0	0	0	0	0	0	0	0	0	0	0	IEN			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOD_IEPOL	R	0	0	0	0	0	0	0	0	0	0	0	0	IEPOL			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOD_IPEND	R	0	0	0	0	0	0	0	0	0	0	0	0	IPR			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOD_IEDGE	R	0	0	0	0	0	0	0	0	0	0	0	0	IES			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOD_PPOUTM	R	0	0	0	0	0	0	0	0	0	0	0	0	OEN			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$A	GPIOD_RDATA	R	0	0	0	0	0	0	0	0	0	0	0	0	RAW DATA			
		W																
		RS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOD_DRIVE	R	0	0	0	0	0	0	0	0	0	0	0	0	DRIVE			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved

Figure 8-4 GPIOD Register Map Summary

Part 9 Joint Test Action Group (JTAG)

9.1 56F8014 Information

Please contact your Freescale sales representative or authorized distributor for device/package-specific BSDL information.

The $\overline{\text{TRST}}$ pin is not available in this package. The pin is tied to V_{DD} in the package.

The JTAG state machine is reset during POR and can also be reset via a soft reset by holding TMS high for five rising edges of TCK, as described in the **56F8000 Peripheral User Manual**.

Part 10 Specifications

10.1 General Characteristics

The 56F8014 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels, combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40ºC to 125ºC ambient temperature over the following supply ranges:
$V_{SS} = V_{SS}A = 0V$, $V_{DD} = V_{DDA} = 3.0–3.6V$, $CL \leq 50pF$, $f_{OP} = 32MHz$

5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. See **Section 12.1** for more details on thermal design considerations.

Table 10-4 Recommended Operating Conditions

(V_{REFL} = 0V, V_{SSA} = 0V, V_{SS} = 0V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}		3	3.3	3.6	V
ADC Supply voltage	V_{DDA}		3	3.3	3.6	V
ADC High Voltage Reference	V_{REFH}		3	—	V_{DDA}	V
Voltage difference V_{DD_IO} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS_IO} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 8 0	—	 32 32	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2	—	5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3	—	0.8	V
Output Source Current High (at V_{OH} min.) When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —	 — —	 -4 -8	mA
Output Source Current Low (at V_{OL} max.) When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —	 — —	 4 8	mA
Ambient Operating Temperature (Automotive)	T_A		-40	—	125	°C
Ambient Operating Temperature (Industrial)	T_A		-40	—	105	°C
Flash Endurance (Automotive) (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000	—	—	Cycles
Flash Endurance (Industrial) (Program Erase Cycles)	N_F	T_A = -40°C to 105°C	10,000	—	—	Cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15	—	—	Years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	Years

Note: Total chip source or sink current cannot exceed 50mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC analog inputs

10.12 Inter-Integrated Circuit Interface (I^2C) Timing

Table 10-17 I^2C Timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0		0.6		µs
LOW period of the SCL clock	t_{LOW}	4.7		1.25		µs
HIGH period of the SCL clock	t_{HIGH}	4.0		0.6		µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7		0.6		µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	0[1]	0.9[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250		100[3]		ns
Rise time of both SDA and SCL signals	t_r		1000	$2 + 0.1C_b$[4]	300	ns
Fall time of both SDA and SCL signals	t_f		300	$2 + 0.1C_b$[4]	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0		0.6		µs
Bus free time between STOP and START condition	t_{BUF}	4.7		1.3		µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0.0	50	ns

1. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
2. The maximum $t_{HD;\ DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT}$ > = 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
4. C_b = total capacitance of the one bus line in pF.

10.14 Analog-to-Digital Converter (ADC) Parameters

Table 10-19 ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	5.33	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC power-up time[2]	t_{ADPU}	—	6	13	t_{AIC} cycles[3]
Recovery from auto standby	t_{REC}	—	0	1	t_{AIC} cycles[3]
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy					
Integral non-linearity[4] (Full input signal range)	INL	—	+/- 3	+/- 5	LSB[5]
Differential non-linearity	DNL	—	+/- .6	+/- 1	LSB[5]
Monotonicity	GUARANTEED				
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 4	+/- 9	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 6	+/- 12	mV
Gain Error (transfer gain)	E_{GAIN}	—	.998 to 1.002	1.01 to .99	—
ADC Inputs[6] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0	—	µA
Input injection current[7], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See **Figure 10-17**	—	pF
Input impedance	X_{IN}	—	See **Figure 10-17**	—	Ohms
AC Specifications					
Signal-to-noise ratio	SNR	60	65		dB
Total Harmonic Distortion	THD	60	64		dB
Spurious Free Dynamic Range	SFDR	61	66		dB
Signal-to-noise plus distortion	SINAD	58	62		dB
Effective Number Of Bits	ENOB	—	10.0		Bits

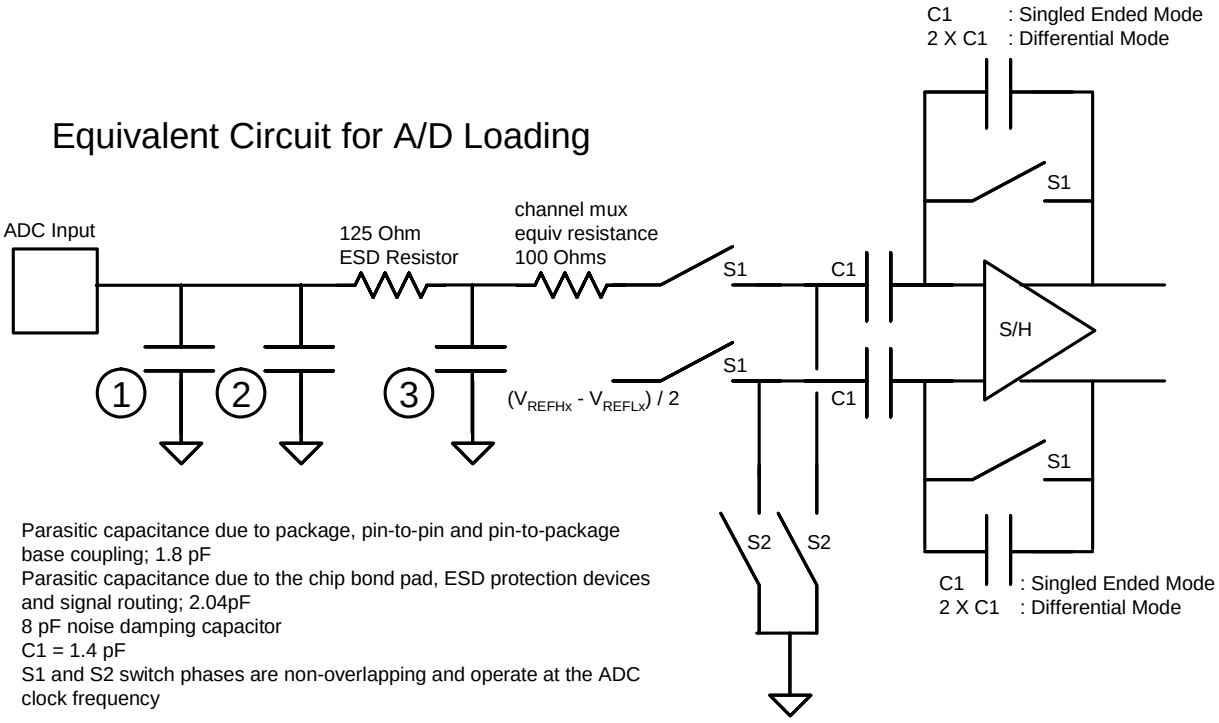
1. All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2. Includes power-up of ADC and V_{REF}
3. ADC clock cycles
4. INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

5. LSB = Least Significant Bit = 0.806mV
6. Pin groups are detailed following **Table 10-1**.
7. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC.

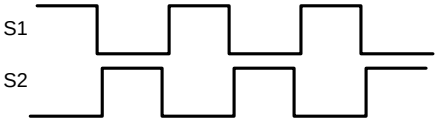
10.15 Equivalent Circuit for ADC Inputs

Figure 10-17 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8 pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. 8 pF noise damping capacitor
4. C1 = 1.4 pF
5. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency



6. Equivalent input impedance, when the input is selected = $\frac{1}{(ADC\ Clock\ Rate)\times 1.4\times 10^{-12}} + 100ohm + 125ohm$

1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. Equivalent resistance for the channel select mux; 100 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pf
5. Equivalent input impedance, when the the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times 1.4 \times 10^{-12}}$

Figure 10-17 Equivalent Circuit for A/D Loading

10.16 Power Consumption

See **Section 10.1** for a list of IDD requirements for the 56F8014. This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]

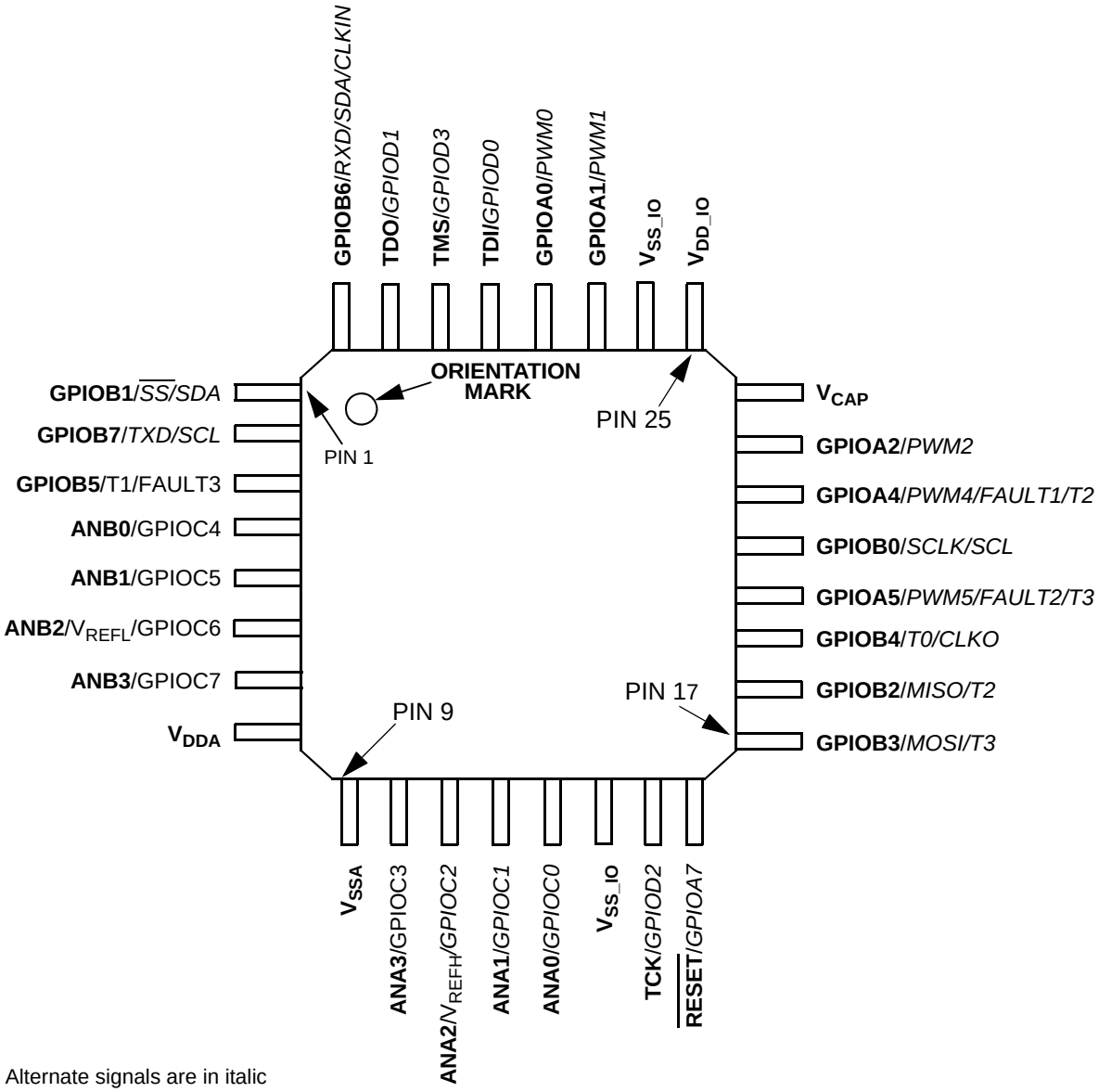
+B: internal [state-dependent component]

Please see http://www.freescale.com for the most current mechanical drawing.

Part 11 Packaging

11.1 56F8014 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8014. This device comes in a 32-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline for the 32-pin LQFP, **Figure 11-2** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 32-pin LQFP.



Note: Alternate signals are in italic

Figure 11-1 Top View, 56F8014 32-Pin LQFP Package