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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8014vfae

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1.4 Architecture Block Diagram

The 56F8014's architecture is shown in **Figure 1-1**, **Figure 1-2**, and **Figure 1-3**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge, as well as showing the internal connections between each unit of the 56800E core. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. **Figure 1-3** details how the device's I/O pins are muxed. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2 Signal/Connection Descriptions** to see which signals are multiplexed with those of other peripherals.

1.5 Synchronize ADC with PWM

ADC conversion can be synchronized with the PWM module via Quad Timer channel 2 and 3 if needed. Internally, the PWM synch signal — which is generated at every PWM reload —can be connected to the timer channel 3 input, and the timer channel 2 and channel 3 outputs are connected to the ADC sync inputs. Timer channel 3 output is connected to SYNC0 and timer channel 2 is connected to SYNC1. The setting is controlled by the TC3_INP bit in the SIM Control Register; see **Section 6.3.1**.

SYNC0 is the master ADC sync input, used to trigger both ADCA and ADCB in sequence and parallel mode. SYNC1 is used to trigger ADCB in parallel independent mode, while SYNC0 is used to trigger ADCA. See *MC56F8000RM*, the 56F801X Peripheral Reference Manual, for additional information.

1.6 Multiple Frequency PWM Output

When both PWM channels of a complementary pair in software control mode and software control bits are set to 1, each complementary PWM signal pair — PWM 0 and 1; PWM 2 and 3; and PWM 4 and 5 — can select a PWM source from one of the following sources. This will enable each PWM pair and PWM2 to output PWM signals at different frequencies.

- External GPIO input:
  - GPIOB2 input can be used to drive PWM 0 and 1
  - GPIOB3 input can be used to drive PWM 2
  - GPIOB4 input can be used to drive PWM 4 and 5
- Quad Timer output:
  - Timer0 output can be used to drive PWM 0 and 1
  - Timer2 output can be used to drive PWM 2
  - Timer3 output can be used to drive PWM 4 and 5
- ADC conversion result:
  - Signal of over/under limit of ADC sample 0 can be used to drive PWM 0 and 1
  - Signal of over/under limit of ADC sample 1 can be used to drive PWM 2

(Continued from Figure 1-2)

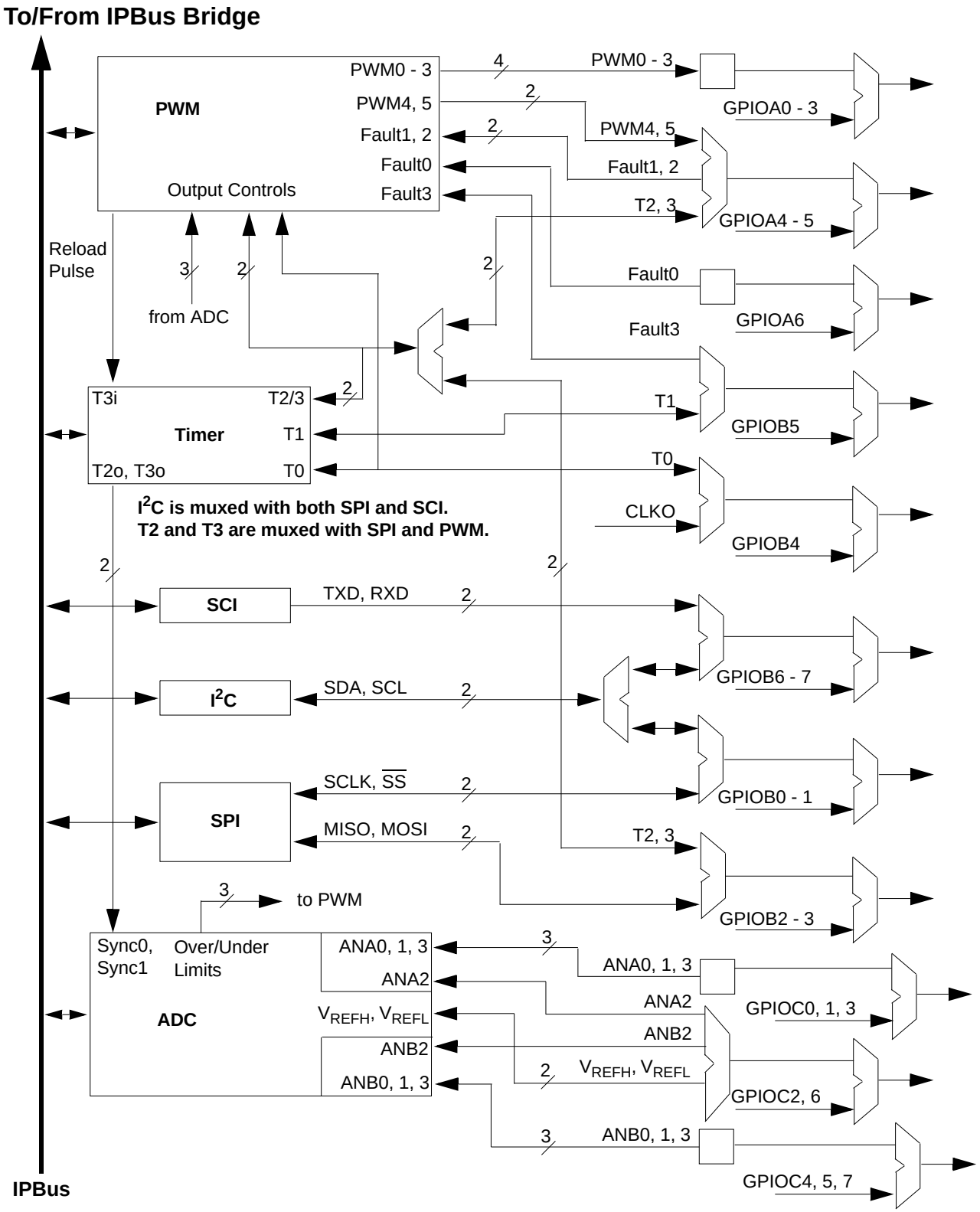

Figure 1-3 56F8014 Peripheral I/O Pin-Out

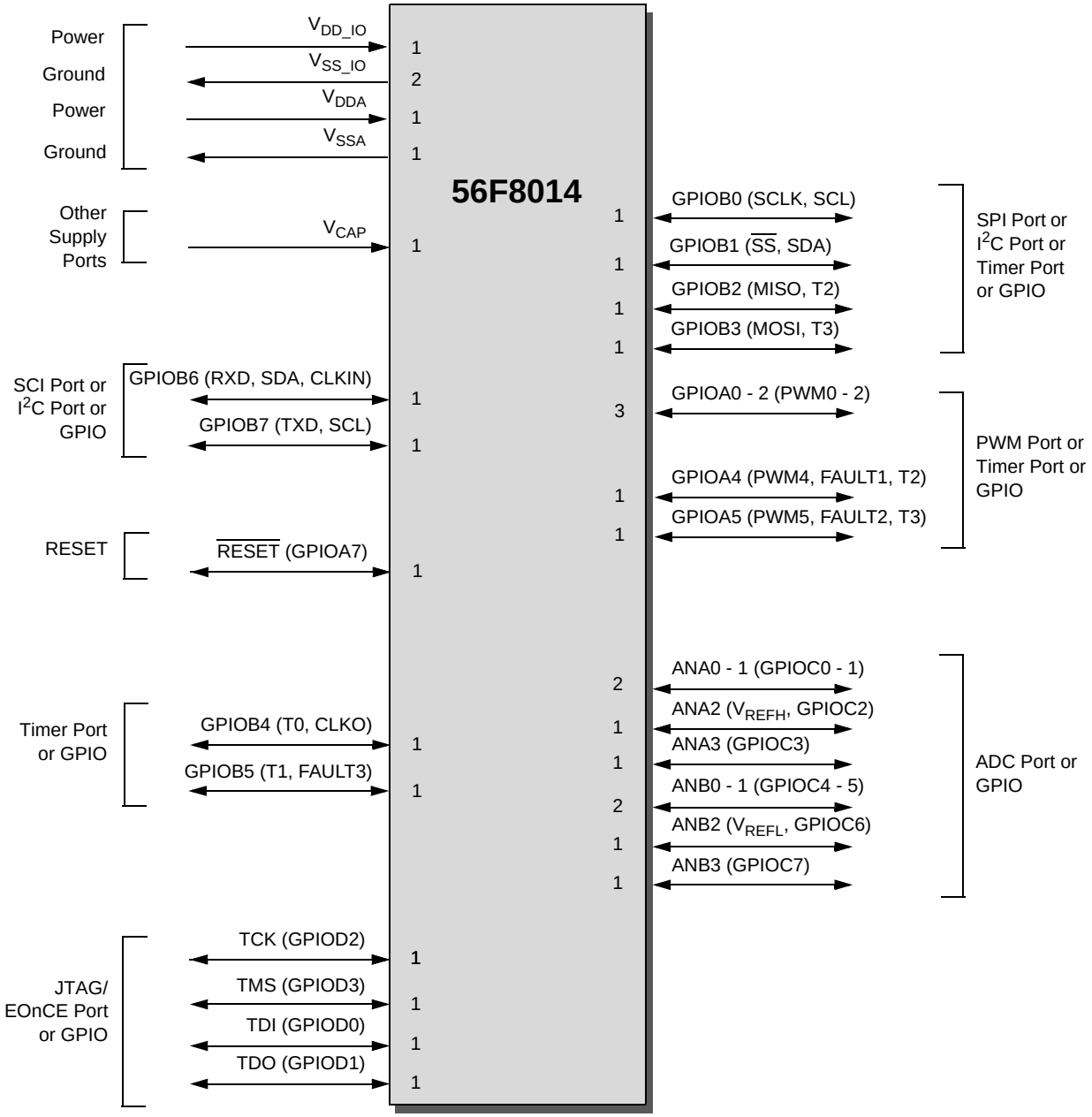

Figure 2-1 56F8014 Signals Identified by Functional Group (32-Pin LQFP)

Table 4-9 Interrupt Control Registers Address Map (Continued) (ITCN_BASE = $00 F060)

Register Acronym	Address Offset	Register Description
ITCN_FIM1	$9	Fast Interrupt Match 1 Register
ITCN_FIVAL1	$A	Fast Interrupt Vector Address Low 1 Register
ITCN_FIVAH1	$B	Fast Interrupt Vector Address High 1 Register
ITCN_IRQP 0	$C	IRQ Pending Register 0
ITCN_IRQP 1	$D	IRQ Pending Register 1
ITCN_IRQP 2	$E	IRQ Pending Register 2
		Reserved
ITCN_ICTRL	$12	Interrupt Control Register
		Reserved

Table 4-10 Analog-to-Digital Converter Registers Address Map (ADC_BASE = $00 F080)

Register Acronym	Address Offset	Register Description
ADC_CTRL1	$0	Control Register 1
ADC_CTRL2	$1	Control Register 2
ADC_ZXCTRL	$2	Zero Crossing Control Register
ADC_CLIST 1	$3	Channel List Register 1
ADC_CLIST 2	$4	Channel List Register 2
ADC_SDIS	$5	Sample Disable Register
ADC_STAT	$6	Status Register
ADC_LIMSTAT	$7	Limit Status Register
ADC_ZXSTAT	$8	Zero Crossing Status Register
ADC_RSLT0	$9	Result Register 0
ADC_RSLT1	$A	Result Register 1
ADC_RSLT2	$B	Result Register 2
ADC_RSLT3	$C	Result Register 3
ADC_RSLT4	$D	Result Register 4
ADC_RSLT5	$E	Result Register 5
ADC_RSLT6	$F	Result Register 6
ADC_RSLT7	$10	Result Register 7
ADC_LOLIM0	$11	Low Limit Register 0
ADC_LOLIM1	$12	Low Limit Register 1
ADC_LOLIM2	$13	Low Limit Register 2
ADC_LOLIM3	$14	Low Limit Register 3
ADC_LOLIM4	$15	Low Limit Register 4
ADC_LOLIM5	$16	Low Limit Register 5

Table 4-12 Serial Peripheral Interface Registers Address Map (SPI_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
SPI_SCTRL	$0	Status and Control Register
SPI_DSCTRL	$1	Data Size and Control Register
SPI_DRCV	$2	Data Receive Register
SPI_DXMIT	$3	Data Transmit Register

Table 4-13 I^2C Registers Address Map (I2C_BASE = $00 F0D0)

Register Acronym	Address Offset	Register Description
I2C_ADDR	$0	Address Register
I2C_FDIV	$1	Frequency Divider Register
I2C_CTRL	$2	Control Register
I2C_STAT	$3	Status Register
I2C_DATA	$4	Data Register
I2C_NFILT	$5	Noise Filter Register

Table 4-14 Computer Operating Properly Registers Address Map (COP_BASE = $00 F0E0)

Register Acronym	Address Offset	Register Description
COP_CTRL	$0	Control Register
COP_TOUT	$1	Time-Out Register
COP_CNTR	$2	Counter Register

Table 4-15 Clock Generation Module Registers Address Map (OCCS_BASE = $00 F0F0)

Register Acronym	Address Offset	Register Description
OCCS_CTRL	$0	Control Register
OCCS_DIVBY	$1	Divide-By Register
OCCS_STAT	$2	Status Register
		Reserved
OCCS_SHUTDN	$4	Shutdown Register
OCCS_OCTRL	$5	Oscillator Control Register

Table 4-18 GPIOC Registers Address Map (GPIOC_BASE = $00 F120)

Register Acronym	Address Offset	Register Description
GPIOC_PUPEN	$0	Pull-up Enable Register
GPIOC_DATA	$1	Data Register
GPIOC_DDIR	$2	Data Direction Register
GPIOC_PEREN	$3	Peripheral Enable Register
GPIOC_IASSRT	$4	Interrupt Assert Register
GPIOC_IEN	$5	Interrupt Enable Register
GPIOC_IEPOL	$6	Interrupt Edge Polarity Register
GPIOC_IPEND	$7	Interrupt Pending Register
GPIOC_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOC_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOC_RDATA	$A	Raw Data Register
GPIOC_DRIVE	$B	Drive Strength Control Register

Table 4-19 GPIOD Registers Address Map (GPIOD_BASE = $00 F130)

Register Acronym	Address Offset	Register Description
GPIOD_PUPEN	$0	Pull-up Enable Register
GPIOD_DATA	$1	Data Register
GPIOD_DDIR	$2	Data Direction Register
GPIOD_PEREN	$3	Peripheral Enable Register
GPIOD_IASSRT	$4	Interrupt Assert Register
GPIOD_IEN	$5	Interrupt Enable Register
GPIOD_IEPOL	$6	Interrupt Edge Polarity Register
GPIOD_IPEND	$7	Interrupt Pending Register
GPIOD_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOD_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOD_RDATA	$A	Raw Data Register
GPIOD_DRIVE	$B	Drive Strength Control Register

5.4 Block Diagram

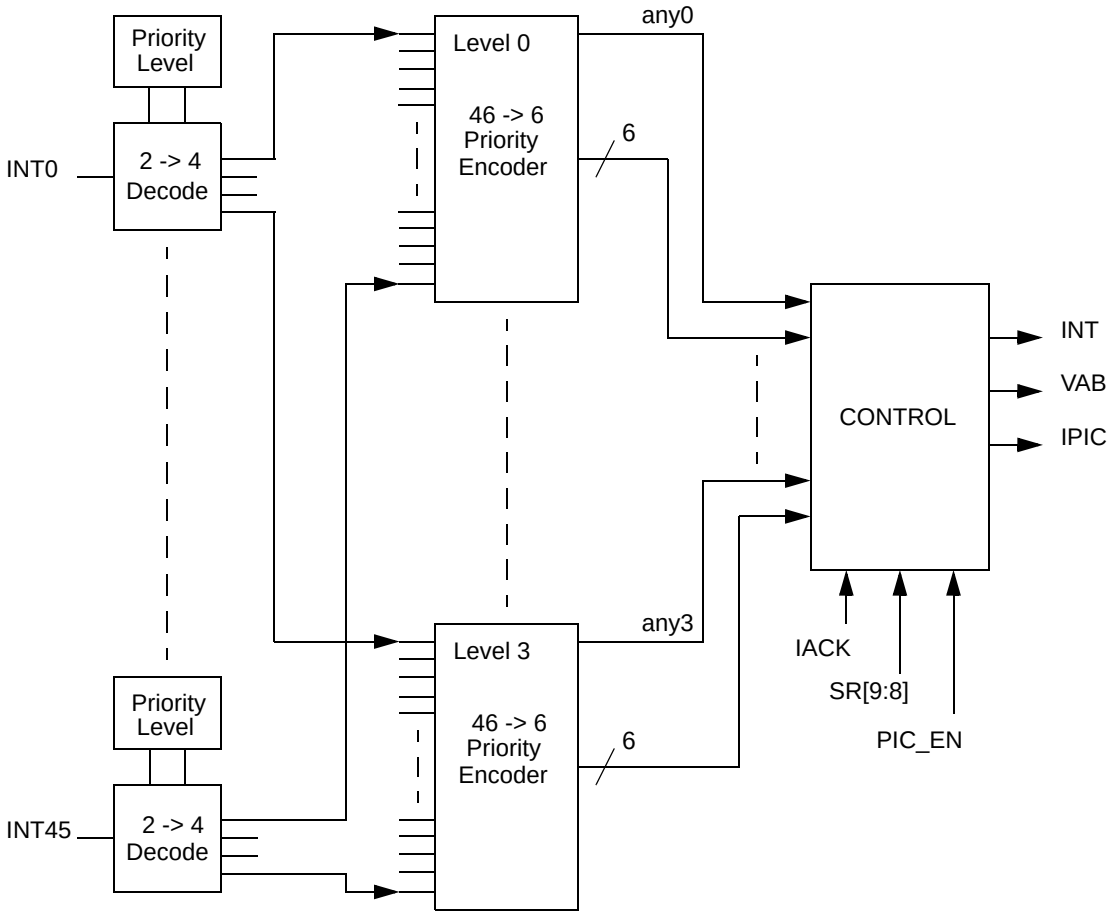

Figure 5-1 Interrupt Controller Block Diagram

5.5 Register Descriptions

A register address is the sum of a base address and an address offset. The base address is defined at the system level and the address offset is defined at the module level. The ITCN module has 16 registers.

Table 5-2 ITCN Register Summary (ITCN_BASE = $00 F060)

Register Acronym	Base Address +	Register Name	Section Location
IPR0	$0	Interrupt Priority Register 0	5.5.1
IPR1	$1	Interrupt Priority Register 1	5.5.2
IPR2	$2	Interrupt Priority Register 2	5.5.3

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	LVI IPL		0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL		BKPT_U IPL		STPCNT IPL	
		W																
$1	IPR1	R	GPIOB IPL		GPIOC IPL		GPIOD IPL		0	0	FM_CBE IPL		FM_CC IPL		FM_ERR IPL		PLL IPL	
		W																
$2	IPR2	R	SCI_RCV IPL		SCI_RERR IPL		0	0	SCI_TIDL IPL		SCI_XMIT IPL		SPI_XMIT IPL		SPI_RCV IPL		GPIOA IPL	
		W																
$3	IPR3	R	ADCA_CC IPL		TMR_3 IPL		TMR_2 IPL		TMR_1 IPL		TMR_0 IPL		I2C_ADDR IPL		0	0	0	0
		W																
$4	IPR4	R	0	0	0	0	0	0	0	0	PWM_F IPL		PWM_RL IPL		ADC_ZC_LE IPL		ADCB_CC IPL	
		W																
$5	VBA	R	0	0	VECTOR_BASE_ADDRESS													
		W																
$6	FIM0	R	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0					
		W																
$7	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$8	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$9	FIM1	R	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1					
		W																
$A	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$B	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W																
$C	IRQP0	R	PENDING[16:2]															1
		W																
$D	IRQP1	R	PENDING[32:17]															
		W																
$E	IRQP2	R	1	1	1	PENDING[45:33]												
		W																
	Reserved																	
$12	ICTRL	R	INT	IPIC		VAB							INT_DIS	1	1	1	0	0
		W																
	Reserved																	

= Reserved

Figure 5-2 ITCN Register Map Summary

5.5.1 Interrupt Priority Register 0 (IPR0)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	LVI IPL		0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL		BKPT_U IPL		STPCNT IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-3 Interrupt Priority Register 0 (IPR0)

5.5.16.1 Interrupt (INT)—Bit 15

This *read-only* bit reflects the state of the interrupt to the 56800E core.

- 0 = No interrupt is being sent to the 56800E core
- 1 = An interrupt is being sent to the 56800E core

5.5.16.2 Interrupt Priority Level (IPIC)—Bits 14–13

These *read-only* bits reflect the state of the new interrupt priority level bits being presented to the 56800E core. These bits indicate the priority level needed for a new IRQ to interrupt the current interrupt being sent to the 56800E core. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

- 00 = Required nested exception priority levels are 0, 1, 2, or 3
- 01 = Required nested exception priority levels are 1, 2, or 3
- 10 = Required nested exception priority levels are 2 or 3
- 11 = Required nested exception priority level is 3

Table 5-3 Interrupt Priority Encoding

IPIC_VALUE[1:0]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priority 2 or 3	Priority 3

5.5.16.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows the vector number (VAB[6:0]) used at the time the last IRQ was taken. In the case of a Fast Interrupt, it shows the lower address bits of the jump address. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

5.5.16.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

- 1 = Clocks to the Quad Timer module are enabled

6.3.9.6 Reserved—Bit 5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.9.7 SCI IPBus Clock Enable (SCI)—Bit 4

- 0 = The clock is not provided to the SCI module (the SCI module is disabled)
- 1 = Clocks to the SCI module are enabled

6.3.9.8 Reserved—Bit 3

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.9.9 SPI Clock Enable (SPI)—Bit 2

- 0 = The clock is not provided to the SPI module (the SPI module is disabled)
- 1 = Clocks to the SPI module are enabled

6.3.9.10 Reserved—Bit 1

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.9.11 PWM Clock Enable (PWM)—Bit 0

- 0 = The clock is not provided to the PWM module (the PWM module is disabled)
- 1 = Clocks to the PWM module are enabled

6.3.10 I/O Short Address Location Register (SIM_IOSAHI and SIM_IOSALO)

The I/O Short Address Location registers are used to specify the memory referenced via the I/O short address mode. The I/O short address mode allows the instruction to specify the lower six bits of address; the upper address bits are not directly controllable. This register set allows limited control of the full address, as shown in **Figure 6-12**.

Table 6-3 Clock Operation in Power-Down Modes (Continued)

Mode	Core Clocks	Peripheral Clocks	Description
Wait	Core and memory clocks disabled	Peripheral clocks enabled	Core executes WAIT instruction to enter this mode. Typically used for power-conscious applications. Possible recoveries from Wait mode to Run mode are: 1. Any interrupt 2. Executing a Debug mode entry command during the 56800E core JTAG interface 2. Any reset (POR, external, software, COP)
Stop	Master clock generation in the OCCS remains operational, but the SIM disables the generation of system and peripheral clocks.		Core executes STOP instruction to enter this mode. Possible recoveries from Stop mode to Run mode are: 1. Interrupt from Timer channels that have been configured to operate in Stop mode (TCx_SD) 2. Interrupt for SCI configured to operate in Stop mode (SCI_SD) 3. Low-voltage interrupt 4. Executing a Debug mode entry command using the 56800E core JTAG interface 5. Any reset (POR, external, software, COP)
Standby	The OCCS generates the 2x System Clock at a reduced frequency (200 kHz). The PLL and high speed peripheral clocks are disabled and the high-speed peripheral option is not available. System and peripheral clocks operate at 100 kHz.		The user configures the OCCS and SIM to select the relaxation oscillator clock source (PRECS), shut down the PLL (PLLPD), put the relaxation oscillator in Standby mode (ROSB), and put the large regulator in Standby (LRSTDBY). The part is fully operational, but operating at a minimum frequency and power configuration. Recovery requires reversing the sequence used to enter this mode (allowing for PLL lock time).
Power-Down	Master clock generation in the OCCS is completely shut down. All system and peripheral clocks are disabled.		The user configures the OCCS and SIM to enter Standby mode as shown in the previous description, followed by powering down the oscillator (ROPD). The only possible recoveries from this mode are: 1. External reset 2. Power-on reset

The power modes provide additional means to disable clock domains, configure the voltage regulator, and configure clock generation to manage power utilization, as shown in **Table 6-3**. Run, Wait, and Stop modes provide means of enabling/disabling the peripheral and/or core clocking as a group. Stop disable controls are provided for selected peripherals in the control register so that these peripheral clocks can optionally continue to operate in Stop mode and generate interrupts which will return the part from Stop to Run mode. Standby mode provides normal operation but at very low speed and power utilization. It is possible to invoke Stop or Wait mode while in Standby mode for even greater levels of power reduction. A 200 kHz clock external clock can optionally be used in Standby mode to produce the required Standby 100 kHz system bus rate. Power-down mode, which selects the ROSC clock source but shuts it off, fully disables the part and minimizes its power utilization but is only recoverable via reset.

When the PLL is not selected and the system bus is operating at around 100 kHz, the large regulator can

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOA_PUPEN	R	0	0	0	0	0	0	0	0	PU							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$1	GPIOA_DATA	R	0	0	0	0	0	0	0	0	D							
		W																
		RS	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
$2	GPIOA_DDIR	R	0	0	0	0	0	0	0	0	DD							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOA_PEREN	R	0	0	0	0	0	0	0	0	PE							
		W																
		RS	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
$4	GPIOA_IASSRT	R	0	0	0	0	0	0	0	0	IA							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOA_IEN	R	0	0	0	0	0	0	0	0	IEN							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOA_IEPOL	R	0	0	0	0	0	0	0	0	IEPOL							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOA_IPEND	R	0	0	0	0	0	0	0	0	IPR							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOA_IEDGE	R	0	0	0	0	0	0	0	0	IES							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOA_PPOUTM	R	0	0	0	0	0	0	0	0	OEN							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$A	GPIOA_RDATA	R	0	0	0	0	0	0	0	0	RAW DATA							
		W																
		RS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOA_DRIVE	R	0	0	0	0	0	0	0	0	DRIVE							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-1 GPIOA Register Map Summary

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOD_PUPEN	R	0	0	0	0	0	0	0	0	0	0	0	0	PU			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$1	GPIOD_DATA	R	0	0	0	0	0	0	0	0	0	0	0	0	D			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOD_DDIR	R	0	0	0	0	0	0	0	0	0	0	0	0	DD			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOD_PEREN	R	0	0	0	0	0	0	0	0	0	0	0	0	PE			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$4	GPIOD_IASSRT	R	0	0	0	0	0	0	0	0	0	0	0	0	IA			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOD_IEN	R	0	0	0	0	0	0	0	0	0	0	0	0	IEN			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOD_IEPOL	R	0	0	0	0	0	0	0	0	0	0	0	0	IEPOL			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOD_IPEND	R	0	0	0	0	0	0	0	0	0	0	0	0	IPR			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOD_IEDGE	R	0	0	0	0	0	0	0	0	0	0	0	0	IES			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOD_PPOUTM	R	0	0	0	0	0	0	0	0	0	0	0	0	OEN			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$A	GPIOD_RDATA	R	0	0	0	0	0	0	0	0	0	0	0	0	RAW DATA			
		W																
		RS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOD_DRIVE	R	0	0	0	0	0	0	0	0	0	0	0	0	DRIVE			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved

Figure 8-4 GPIOD Register Map Summary

Part 9 Joint Test Action Group (JTAG)

9.1 56F8014 Information

Please contact your Freescale sales representative or authorized distributor for device/package-specific BSDL information.

The $\overline{\text{TRST}}$ pin is not available in this package. The pin is tied to V_{DD} in the package.

The JTAG state machine is reset during POR and can also be reset via a soft reset by holding TMS high for five rising edges of TCK, as described in the **56F8000 Peripheral User Manual**.

Part 10 Specifications

10.1 General Characteristics

The 56F8014 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels, combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40ºC to 125ºC ambient temperature over the following supply ranges:
$V_{SS} = V_{SS}A = 0V$, $V_{DD} = V_{DDA} = 3.0–3.6V$, $CL \leq 50pF$, $f_{OP} = 32MHz$

Table 10-7 Power-On Reset Low-Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3V supply[1]	$V_{EI3.3}$	2.60	2.7	—	V
Low-Voltage Interrupt for 2.5V supply[2]	$V_{E12.5}$	2.05	2.15	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset[3]	POR	—	1.8	1.9	V

1. When V_{DD} drops below $V_{EI3.3}$, an interrupt is generated.
2. When V_{DD} drops below $V_{EI32.5}$, an interrupt is generated.
3. Power-On Reset occurs whenever the internally regulated 2.5V digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 2.15V or the 3.3V 1/O voltage is below 2.7V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

10.2.1 Voltage Regulator Specifications

The 56F8014 has two on-chip regulators. One supplies the PLL and relaxation oscillator. It has no external pins and therefore has no external characteristics which must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5 V to the 56F8014's core logic. This regulator requires an external 2.2 µF, or greater, capacitor for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in **Table 10-8**.

Table 10-8. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Input Voltage	V_{IN}	3.0	—	3.6	V
Output Voltage	V_{OUT}	2.25	2.5	2.75	V
Short Circuit Current	I_{SS}	—	450	650	mA
Short Circuit Tolerance (output shorted to ground)	T_{RSC}	—	—	30	Minutes

10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-2**.

10.14 Analog-to-Digital Converter (ADC) Parameters

Table 10-19 ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	5.33	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC power-up time[2]	t_{ADPU}	—	6	13	t_{AIC} cycles[3]
Recovery from auto standby	t_{REC}	—	0	1	t_{AIC} cycles[3]
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy					
Integral non-linearity[4] (Full input signal range)	INL	—	+/- 3	+/- 5	LSB[5]
Differential non-linearity	DNL	—	+/- .6	+/- 1	LSB[5]
Monotonicity	GUARANTEED				
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 4	+/- 9	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 6	+/- 12	mV
Gain Error (transfer gain)	E_{GAIN}	—	.998 to 1.002	1.01 to .99	—
ADC Inputs[6] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0	—	µA
Input injection current[7], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See **Figure 10-17**	—	pF
Input impedance	X_{IN}	—	See **Figure 10-17**	—	Ohms
AC Specifications					
Signal-to-noise ratio	SNR	60	65		dB
Total Harmonic Distortion	THD	60	64		dB
Spurious Free Dynamic Range	SFDR	61	66		dB
Signal-to-noise plus distortion	SINAD	58	62		dB
Effective Number Of Bits	ENOB	—	10.0		Bits

1. All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2. Includes power-up of ADC and V_{REF}
3. ADC clock cycles
4. INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

+C: internal [dynamic component]

+D: external [dynamic component]

+E: external [static]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

C, the internal [dynamic component], is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic component], reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 10-20 I/O Loading Coefficients at 10MHz

	Intercept	Slope
8mA drive	1.3	0.11mW / pF
4mA drive	1.15mW	0.11mW / pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. **Table 10-20** provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases:

$$TotalPower = \Sigma((\text{Intercept} + \text{Slope}*\text{Cload})*\text{frequency}/10\text{MHz})$$

where:

- Summation is performed over all output pins with capacitive loads
- TotalPower is expressed in mW
- Cload is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

Table 11-1 56F8014 32-Pin LQFP Package Identification by Pin Number[1]

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	**GPIOB1** *$\overline{SS}$,SDA*	9	**V_{SSA}**	17	**GPIOB3** *MOSI,T3*	25	**V_{DD_IO}**
2	**GPIOB7** *TXD,SCL*	10	**ANA3** *GPIOC3*	18	**GPIOB2** *MISO,T2*	26	**V_{SS_IO}**
3	**GPIOB5** *T1,FAULT3*	11	**ANA2** *V_{REFH},GPIOC2*	19	**GPIOB4** *T0,CLKO*	27	**GPIOA1** *PWM1*
4	**ANB0** *GPIOC4*	12	**ANA1** *GPIOC1*	20	**GPIOA5** *PWM5,FAULT2,T3*	28	**GPIOA0** *PWM0*
5	**ANB1** *GPIOC5*	13	**ANA0** *GPIOC0*	21	**GPIOB0** *SCLK/,CL*	29	**TDI** *GPIOD0*
6	**ANB2** *V_{REFL},GPIOC6*	14	**V_{SS_IO}**	22	**GPIOA4** *PWM4/FAULT1/T2*	30	**TMS** *GPIOD3*
7	**ANB3** *GPIOC7*	15	**TCK** *GPIOD2*	23	**GPIOA2** *PWM2*	31	**TDO** *GPIOD1*
8	**V_{DDA}**	16	**$\overline{RESET}$** *GPIOA7*	24	**V_{CAP}**	32	**GPIOB6** *RXD,SDA,CLKIN*

1.Alternate signals are in iltalic

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Technical Information Center, CH370
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Chandler, Arizona 85224
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Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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MC56F8014
Rev. 11
05/2008