### Understanding **Embedded - CPLDs (Complex Programmable Logic Devices)**

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 10 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | 8 |
| Number of Macrocells | 32 |
| Number of Gates | 1000 |
| Number of I/O | 32 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-2032ve-110lj44 |

# ispLSI® 2032VE Device Datasheet

June 2010

# Select Devices Discontinued!

Product Change Notification (PCN) #09-10 has been issued to discontinue select devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

| Product Line | Ordering Part Number | Product Status | Reference PCN |
|---|---|---|---|
| ispLSI 2032VE | ispLSI 2032VE-110LJ44 | Active / Orderable | |
| | ispLSI 2032VE-135LJ44 | | |
| | ispLSI 2032VE-180LJ44 | | |
| | ispLSI 2032VE-225LJ44 | | |
| | ispLSI 2032VE-110LT44 | | |
| | ispLSI 2032VE-135LT44 | | |
| | ispLSI 2032VE-180LT44 | | |
| | ispLSI 2032VE-225LT44 | | |
| | ispLSI 2032VE-300LT44 | | |
| | ispLSI 2032VE-180LT44I | | |
| | ispLSI 2032VE-110LT48 | | |
| | ispLSI 2032VE-135LT48 | | |
| | ispLSI 2032VE-180LT48 | | |
| | ispLSI 2032VE-225LT48 | | |
| | ispLSI 2032VE-300LT48 | | |
| | ispLSI 2032VE-110LB49 | **Discontinued** | PCN#09-10 |
| | ispLSI 2032VE-135LB49 | | |
| | ispLSI 2032VE-180LB49 | | |
| | ispLSI 2032VE-225LB49 | | |
| | ispLSI 2032VE-300LB49 | | |
| | ispLSI 2032VE-110LTN44 | Active / Orderable | |
| | ispLSI 2032VE-135LTN44 | | |
| | ispLSI 2032VE-180LTN44 | | |
| | ispLSI 2032VE-300LTN44 | | |
| | ispLSI 2032VE-180LTN44I | | |
| | ispLSI 2032VE-110LTN48 | | |
| | ispLSI 2032VE-135LTN48 | | |
| | ispLSI 2032VE-180LTN48 | | |
| | ispLSI 2032VE-300LTN48 | | |

# Lattice Semiconductor Corporation

# isplLSI® 2032VE

## 3.3V In-System Programmable High Density SuperFAST™ PLD

## Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - **1000 PLD Gates**
  - **32 I/O Pins, Two Dedicated Inputs**
  - **32 Registers**
  - **High Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
  - **100% Functional, JEDEC and Pinout Compatible with ispLSI 2032V Devices**

- **3.3V LOW VOLTAGE 2032 ARCHITECTURE**
  - **Interfaces With Standard 5V TTL Devices**

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - $f_{max}$ = 300 MHz Maximum Operating Frequency
  - $t_{pd}$ = 3.0 ns Propagation Delay
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
  - **Unused Product Term Shutdown Saves Power**

- **IN-SYSTEM PROGRAMMABLE**
  - **3.3V In-System Programmability Using Boundary Scan Test Access Port (TAP)**
  - **Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR or Bus Arbitration Logic**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**

- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**

- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAs**
  - **Enhanced Pin Locking Capability**
  - **Three Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
  - **Lead-Free Package Options**

## Functional Block Diagram



0139Bisp/2000
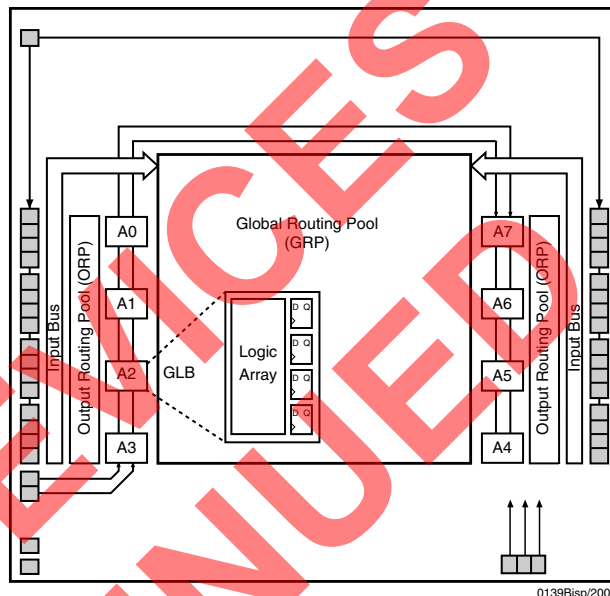
## Description

The ispLSI 2032VE is a High Density Programmable Logic Device that can be used in both 3.3V and 5V systems. The device contains 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032VE features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2032VE offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2032VE device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (see Figure 1). There are a total of eight GLBs in the ispLSI 2032VE device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

## Functional Block Diagram

**Figure 1. ispLSI 2032VE Functional Block Diagram**



Note: *Y1 and RESET are multiplexed on the same pin

0139B/2032VE
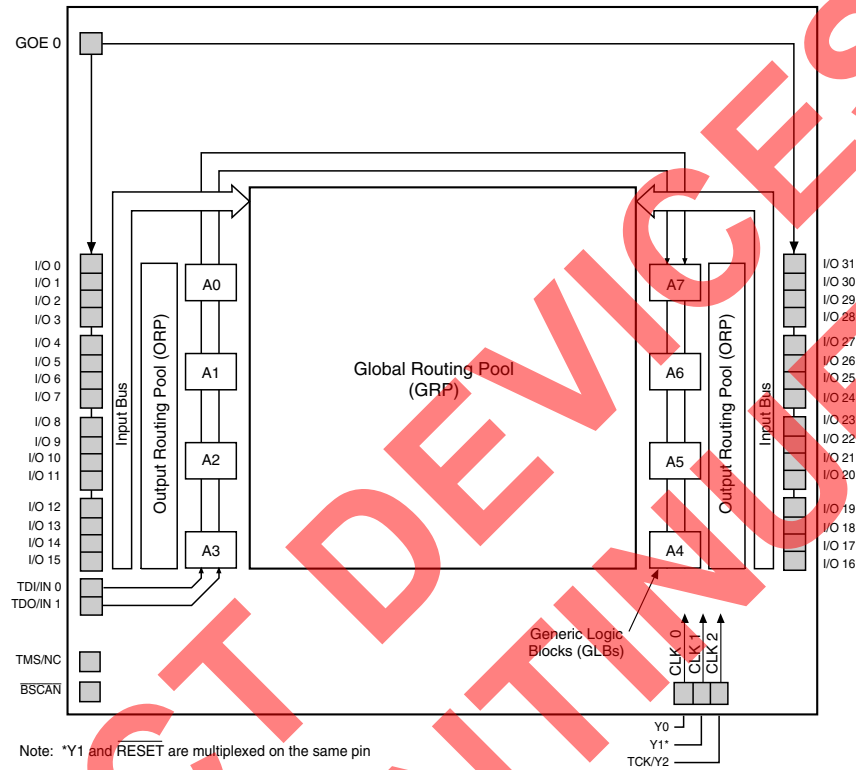
The device also has 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. Device pins can be safely driven to 5 Volt signal levels to support mixed-voltage systems.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORPs. Each ispLSI 2032VE device contains one Megablock.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2032VE device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

### Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2032VE are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is the totem-pole configuration. The open-drain/totem-pole option is selectable through the Lattice design tools.

# Absolute Maximum Ratings [1]

Supply Voltage $V_{CC}$ .................................... -0.5 to +5.4V

Input Voltage Applied .............................. -0.5 to +5.6V

Off-State Output Voltage Applied ............ -0.5 to +5.6V

Storage Temperature ............................. -65 to +150°C

Case Temp. with Power Applied ............. -55 to 125°C

Max. Junction Temp. ($T_J$) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

# DC Recommended Operating Condition

| SYMBOL | PARAMETER | | | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Commercial | $T_A$ = 0°C to + 70°C | 3.0 | 3.6 | V |
| | | Industrial | $T_A$ = -40°C to + 85°C | 3.0 | 3.6 | V |
| $V_{IL}$ | Input Low Voltage | | | $V_{SS} - 0.5$ | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | 2.0 | 5.25 | V |

Table 2-0005/2032VE

# Capacitance ($T_A$=25°C, f=1.0 MHz)

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_1$ | Dedicated Input Capacitance | 8 | pf | $V_{CC}$ = 3.3V, $V_{IN}$ = 0.0V |
| $C_2$ | I/O Capacitance | 6 | pf | $V_{CC}$ = 3.3V, $V_{I/O}$ = 0.0V |
| $C_3$ | Clock Capacitance | 10 | pf | $V_{CC}$ = 3.3V, $V_Y$ = 0.0V |

Table 2-0006/2032VE

# Erase Reprogram Specifications

| PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|
| Erase/Reprogram Cycles | 10,000 | – | Cycles |

Table 2-0008A/2032VE

## Switching Test Conditions

| Input Pulse Levels | GND to 3.0V |
|---|---|
| Input Rise and Fall Time 10% to 90% | ≤ 1.5 ns |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| Output Load | See Figure 2 |

Table 2-0003/2032VE

3-state levels are measured 0.5V from steady-state active level.
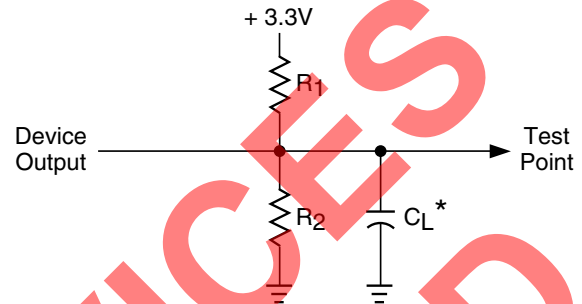
### Figure 2. Test Load



$^*C_L$ includes Test Fixture and Probe Capacitance.

0213A/2032VE

### Output Load Conditions (see Figure 2)

| TEST CONDITION | | R1 | R2 | CL |
|---|---|---|---|---|
| A | | 316Ω | 348Ω | 35pF |
| B | Active High | ∞ | 348Ω | 35pF |
| | Active Low | 316Ω | 348Ω | 35pF |
| C | Active High to Z at $V_{OH}$-0.5V | ∞ | 348Ω | 5pF |
| | Active Low to Z at $V_{OL}$+0.5V | 316Ω | 348Ω | 5pF |

Table 2-0004A/2032VE

## DC Electrical Characteristics

### Over Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITION | | MIN. | TYP.[3] | MAX. | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Voltage | $I_{OL}$= 8 mA | | – | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4 mA | | 2.4 | – | – | V |
| $I_{IL}$ | Input or I/O Low Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ (Max.) | | – | – | -10 | μA |
| $I_{IH}$ | Input or I/O High Leakage Current | ($V_{CC}$ - 0.2)V ≤ $V_{IN}$ ≤ $V_{CC}$ | | – | – | 10 | μA |
| | | $V_{CC}$ ≤ $V_{IN}$ ≤ 5.25V | | – | – | 10 | μA |
| $I_{IL-isp}$ | BSCAN Input Low Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ | | – | – | -150 | μA |
| $I_{IL-PU}$ | I/O Active Pull-Up Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ | | – | – | -150 | μA |
| $I_{OS}$[1] | Output Short Circuit Current | $V_{CC}$= 3.3V, $V_{OUT}$= 0.5V | | – | – | -100 | mA |
| $I_{CC}$[2, 4, 5] | Operating Power Supply Current | $V_{IL}$ = 0.0V, $V_{IH}$ = 3.0V $f_{CLOCK}$ = 1MHz | -300/-225 | – | 80 | – | mA |
| | | | Others | – | 65 | – | mA |

Table 2-0007/2032VE

1. One output at a time for a maximum duration of one second. $V_{OUT}$= 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using two 16-bit counters.
3. Typical values are at $V_{CC}$= 3.3V and $T_A$= 25°C.
4. Maximum $I_{CC}$ varies widely with specific device configuration and operating frequency. Refer to Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum $I_{CC}$.
5. Unused inputs at $V_{IL}$ = 0V.

## External Timing Parameters

### Over Recommended Operating Conditions

| PARAMETER | TEST[3] COND. | # | DESCRIPTION[1] | -300 MIN. | -300 MAX. | -225 MIN. | -225 MAX. | UNITS |
|---|---|---|---|---|---|---|---|---|
| $t_{pd1}$ | A | 1 | Data Propagation Delay, 4PT Bypass, ORP Bypass | – | 3.0 | – | 4.0 | ns |
| $t_{pd2}$ | A | 2 | Data Propagation Delay | – | 4.5 | – | 6.0 | ns |
| $f_{max}$ | A | 3 | Clock Frequency with Internal Feedback[2] | 300 | – | 225 | – | MHz |
| $f_{max}$ (Ext.) | – | 4 | Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$ | 208 | – | 154 | – | MHz |
| $f_{max}$ (Tog.) | – | 5 | Clock Frequency, Max. Toggle | 333 | – | 250 | – | MHz |
| $t_{su1}$ | – | 6 | GLB Reg. Setup Time before Clock, 4 PT Bypass | 2.0 | – | 2.5 | – | ns |
| $t_{co1}$ | A | 7 | GLB Reg. Clock to Output Delay, ORP Bypass | – | 2.0 | – | 3.0 | ns |
| $t_{h1}$ | – | 8 | GLB Reg. Hold Time after Clock, 4 PT Bypass | 0.0 | – | 0.0 | – | ns |
| $t_{su2}$ | – | 9 | GLB Reg. Setup Time before Clock | 2.8 | – | 3.5 | – | ns |
| $t_{co2}$ | A | 10 | GLB Reg. Clock to Output Delay | – | 2.5 | – | 4.0 | ns |
| $t_{h2}$ | – | 11 | GLB Reg. Hold Time after Clock | 0.0 | – | 0.0 | – | ns |
| $t_{r1}$ | A | 12 | Ext. Reset Pin to Output Delay, ORP Bypass | – | 4.5 | – | 5.0 | ns |
| $t_{rw1}$ | – | 13 | Ext. Reset Pulse Duration | 3.0 | – | 3.5 | – | ns |
| $t_{ptoeen}$ | B | 14 | Input to Output Enable | – | 5.0 | – | 7.0 | ns |
| $t_{ptoedis}$ | C | 15 | Input to Output Disable | – | 5.0 | – | 7.0 | ns |
| $t_{goeen}$ | B | 16 | Global OE Output Enable | – | 3.0 | – | 3.5 | ns |
| $t_{goedis}$ | C | 17 | Global OE Output Disable | – | 3.0 | – | 3.5 | ns |
| $t_{wh}$ | – | 18 | External Synchronous Clock Pulse Duration, High | 1.5 | – | 2.0 | – | ns |
| $t_{wl}$ | – | 19 | External Synchronous Clock Pulse Duration, Low | 1.5 | – | 2.0 | – | ns |

1. Unless noted otherwise, all parameters use a GRP load of 4, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

Table 2-0030A/2032VE
v.0.1

## External Timing Parameters

### Over Recommended Operating Conditions

| PARAMETER | TEST[3] COND. | # | DESCRIPTION[1] | -180 MIN. | -180 MAX. | -135 MIN. | -135 MAX. | -110 MIN. | -110 MAX. | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{pd1}$ | A | 1 | Data Propagation Delay, 4PT Bypass, ORP Bypass | – | 5.0 | – | 7.5 | – | 10.0 | ns |
| $t_{pd2}$ | A | 2 | Data Propagation Delay | – | 7.5 | – | 10.0 | – | 13.0 | ns |
| $f_{max}$ | A | 3 | Clock Frequency with Internal Feedback[2] | 180 | – | 135 | – | 111 | – | MHz |
| $f_{max}$ (Ext.) | – | 4 | Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$ | 118 | – | 100 | – | 77.0 | – | MHz |
| $f_{max}$ (Tog.) | – | 5 | Clock Frequency, Max. Toggle | 200 | – | 167 | – | 125 | – | MHz |
| $t_{su1}$ | – | 6 | GLB Reg. Setup Time before Clock, 4 PT Bypass | 3.0 | – | 4.0 | – | 5.5 | – | ns |
| $t_{co1}$ | A | 7 | GLB Reg. Clock to Output Delay, ORP Bypass | – | 4.0 | – | 4.5 | – | 5.0 | ns |
| $t_{h1}$ | – | 8 | GLB Reg. Hold Time after Clock, 4 PT Bypass | 0.0 | – | 0.0 | – | 0.0 | – | ns |
| $t_{su2}$ | – | 9 | GLB Reg. Setup Time before Clock | 4.0 | – | 5.5 | – | 7.5 | – | ns |
| $t_{co2}$ | A | 10 | GLB Reg. Clock to Output Delay | – | 5.0 | – | 5.5 | – | 6.5 | ns |
| $t_{h2}$ | – | 11 | GLB Reg. Hold Time after Clock | 0.0 | – | 0.0 | – | 0.0 | – | ns |
| $t_{r1}$ | A | 12 | Ext. Reset Pin to Output Delay, ORP Bypass | – | 6.0 | – | 9.0 | – | 12.5 | ns |
| $t_{rw1}$ | – | 13 | Ext. Reset Pulse Duration | 4.0 | – | 5.0 | – | 6.5 | – | ns |
| $t_{ptoeen}$ | B | 14 | Input to Output Enable | – | 10.0 | – | 12.0 | – | 14.5 | ns |
| $t_{ptoedis}$ | C | 15 | Input to Output Disable | – | 10.0 | – | 12.0 | – | 14.5 | ns |
| $t_{goeen}$ | B | 16 | Global OE Output Enable | – | 5.0 | – | 6.0 | – | 7.0 | ns |
| $t_{goedis}$ | C | 17 | Global OE Output Disable | – | 5.0 | – | 6.0 | – | 7.0 | ns |
| $t_{wh}$ | – | 18 | External Synchronous Clock Pulse Duration, High | 2.5 | – | 3.0 | – | 4.0 | – | ns |
| $t_{wl}$ | – | 19 | External Synchronous Clock Pulse Duration, Low | 2.5 | – | 3.0 | – | 4.0 | – | ns |

1. Unless noted otherwise, all parameters use a GRP load of 4, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

Table 2-0030B/2032VE
v.0.1

6

## Internal Timing Parameters[1]

### Over Recommended Operating Conditions

| PARAMETER | #[2] | DESCRIPTION | -300 | | -225 | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| **Inputs** | | | | | | | |
| $t_{io}$ | 20 | Input Buffer Delay | – | 0.4 | – | 0.6 | ns |
| $t_{din}$ | 21 | Dedicated Input Delay | – | 1.0 | – | 1.3 | ns |
| **GRP** | | | | | | | |
| $t_{grp}$ | 22 | GRP Delay | – | 0.6 | – | 0.7 | ns |
| **GLB** | | | | | | | |
| $t_{4ptbpc}$ | 23 | 4 Product Term Bypass Path Delay (Combinatorial) | – | 0.9 | – | 1.2 | ns |
| $t_{4ptbpr}$ | 24 | 4 Product Term Bypass Path Delay (Registered) | – | 1.1 | – | 1.2 | ns |
| $t_{1ptxor}$ | 25 | 1 Product Term/XOR Path Delay | – | 1.9 | – | 2.2 | ns |
| $t_{20ptxor}$ | 26 | 20 Product Term/XOR Path Delay | – | 1.9 | – | 2.2 | ns |
| $t_{xoradj}$ | 27 | XOR Adjacent Path Delay [3] | – | 1.9 | – | 2.2 | ns |
| $t_{gbp}$ | 28 | GLB Register Bypass Delay | – | 0.0 | – | 0.0 | ns |
| $t_{gsu}$ | 29 | GLB Register Setup Time before Clock | 0.5 | – | 0.8 | – | ns |
| $t_{gh}$ | 30 | GLB Register Hold Time after Clock | 1.5 | – | 1.7 | – | ns |
| $t_{gco}$ | 31 | GLB Register Clock to Output Delay | – | 0.3 | – | 0.7 | ns |
| $t_{gro}$ | 32 | GLB Register Reset to Output Delay | – | 1.3 | – | 1.3 | ns |
| $t_{ptre}$ | 33 | GLB Product Term Reset to Register Delay | – | 2.5 | – | 3.2 | ns |
| $t_{ptoe}$ | 34 | GLB Product Term Output Enable to I/O Cell Delay | – | 3.0 | – | 4.2 | ns |
| $t_{ptck}$ | 35 | GLB Product Term Clock Delay | 0.4 | 2.3 | 0.5 | 2.8 | ns |
| **ORP** | | | | | | | |
| $t_{orp}$ | 36 | ORP Delay | – | 0.6 | – | 1.3 | ns |
| $t_{orpbp}$ | 37 | ORP Bypass Delay | – | 0.1 | – | 0.3 | ns |
| **Outputs** | | | | | | | |
| $t_{ob}$ | 38 | Output Buffer Delay | – | 1.0 | – | 1.2 | ns |
| $t_{sl}$ | 39 | Output Slew Limited Delay Adder | – | 2.0 | – | 2.0 | ns |
| $t_{oen}$ | 40 | I/O Cell OE to Output Enabled | – | 1.0 | – | 1.5 | ns |
| $t_{odis}$ | 41 | I/O Cell OE to Output Disabled | – | 1.0 | – | 1.5 | ns |
| $t_{goe}$ | 42 | Global Output Enable | – | 2.0 | – | 2.0 | ns |
| **Clocks** | | | | | | | |
| $t_{gy0}$ | 43 | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 0.6 | 0.6 | 0.8 | 0.8 | ns |
| $t_{gy1/2}$ | 44 | Clock Delay, Y1 or Y2 to Global GLB Clock Line | 0.8 | 0.8 | 1.0 | 1.0 | ns |
| **Global Reset** | | | | | | | |
| $t_{gr}$ | 45 | Global Reset to GLB | – | 2.1 | – | 2.2 | ns |

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036A/2032VE
v.0.1

## Internal Timing Parameters[1]

### Over Recommended Operating Conditions

| PARAMETER | #[2] | DESCRIPTION | -180 MIN. | -180 MAX. | -135 MIN. | -135 MAX. | -110 MIN. | -110 MAX. | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **Inputs** | | | | | | | | | |
| $t_{io}$ | 20 | Input Buffer Delay | – | 0.8 | – | 0.8 | – | 1.3 | ns |
| $t_{din}$ | 21 | Dedicated Input Delay | – | 1.5 | – | 1.7 | – | 2.5 | ns |
| **GRP** | | | | | | | | | |
| $t_{grp}$ | 22 | GRP Delay | – | 0.7 | – | 0.9 | – | 1.2 | ns |
| **GLB** | | | | | | | | | |
| $t_{4ptbpc}$ | 23 | 4 Product Term Bypass Path Delay (Combinatorial) | – | 1.8 | – | 3.9 | – | 4.8 | ns |
| $t_{4ptbpr}$ | 24 | 4 Product Term Bypass Path Delay (Registered) | – | 2.1 | – | 2.9 | – | 3.4 | ns |
| $t_{1ptxor}$ | 25 | 1 Product Term/XOR Path Delay | – | 3.1 | – | 4.4 | – | 5.4 | ns |
| $t_{20ptxor}$ | 26 | 20 Product Term/XOR Path Delay | – | 3.1 | – | 4.4 | – | 5.4 | ns |
| $t_{xoradj}$ | 27 | XOR Adjacent Path Delay [3] | – | 3.1 | – | 4.4 | – | 5.4 | ns |
| $t_{gbp}$ | 28 | GLB Register Bypass Delay | – | 0.2 | – | 1.0 | – | 1.4 | ns |
| $t_{gsu}$ | 29 | GLB Register Setup Time before Clock | 0.9 | – | 1.1 | – | 1.4 | – | ns |
| $t_{gh}$ | 30 | GLB Register Hold Time after Clock | 2.1 | – | 2.9 | – | 4.1 | – | ns |
| $t_{gco}$ | 31 | GLB Register Clock to Output Delay | – | 0.8 | – | 0.9 | – | 1.0 | ns |
| $t_{gro}$ | 32 | GLB Register Reset to Output Delay | – | 1.3 | – | 1.8 | – | 2.7 | ns |
| $t_{ptre}$ | 33 | GLB Product Term Reset to Register Delay | – | 4.0 | – | 6.1 | – | 7.1 | ns |
| $t_{ptoe}$ | 34 | GLB Product Term Output Enable to I/O Cell Delay | – | 5.7 | – | 6.9 | – | 8.6 | ns |
| $t_{ptck}$ | 35 | GLB Product Term Clock Delay | 1.4 | 3.6 | 1.7 | 4.1 | 2.5 | 4.4 | ns |
| **ORP** | | | | | | | | | |
| $t_{orp}$ | 36 | ORP Delay | – | 1.4 | – | 1.5 | – | 1.9 | ns |
| $t_{orpbp}$ | 37 | ORP Bypass Delay | – | 0.4 | – | 0.5 | – | 0.9 | ns |
| **Outputs** | | | | | | | | | |
| $t_{ob}$ | 38 | Output Buffer Delay | – | 1.3 | – | 1.4 | – | 1.8 | ns |
| $t_{sl}$ | 39 | Output Slew Limited Delay Adder | – | 2.0 | – | 2.0 | – | 2.0 | ns |
| $t_{oen}$ | 40 | I/O Cell OE to Output Enabled | – | 2.8 | – | 3.4 | – | 3.4 | ns |
| $t_{odis}$ | 41 | I/O Cell OE to Output Disabled | – | 2.8 | – | 3.4 | – | 3.4 | ns |
| $t_{goe}$ | 42 | Global Output Enable | – | 2.2 | – | 2.6 | – | 3.6 | ns |
| **Clocks** | | | | | | | | | |
| $t_{gy0}$ | 43 | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 1.5 | 1.5 | 1.7 | 1.7 | 1.8 | 1.8 | ns |
| $t_{gy1/2}$ | 44 | Clock Delay, Y1 or Y2 to Global GLB Clock Line | 1.7 | 1.7 | 1.9 | 1.9 | 2.0 | 2.0 | ns |
| **Global Reset** | | | | | | | | | |
| $t_{gr}$ | 45 | Global Reset to GLB | – | 3.0 | – | 5.3 | – | 7.1 | ns |

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036A/2032VE
v.0.1

## ispLSI 2032VE Timing Model



0491/2000
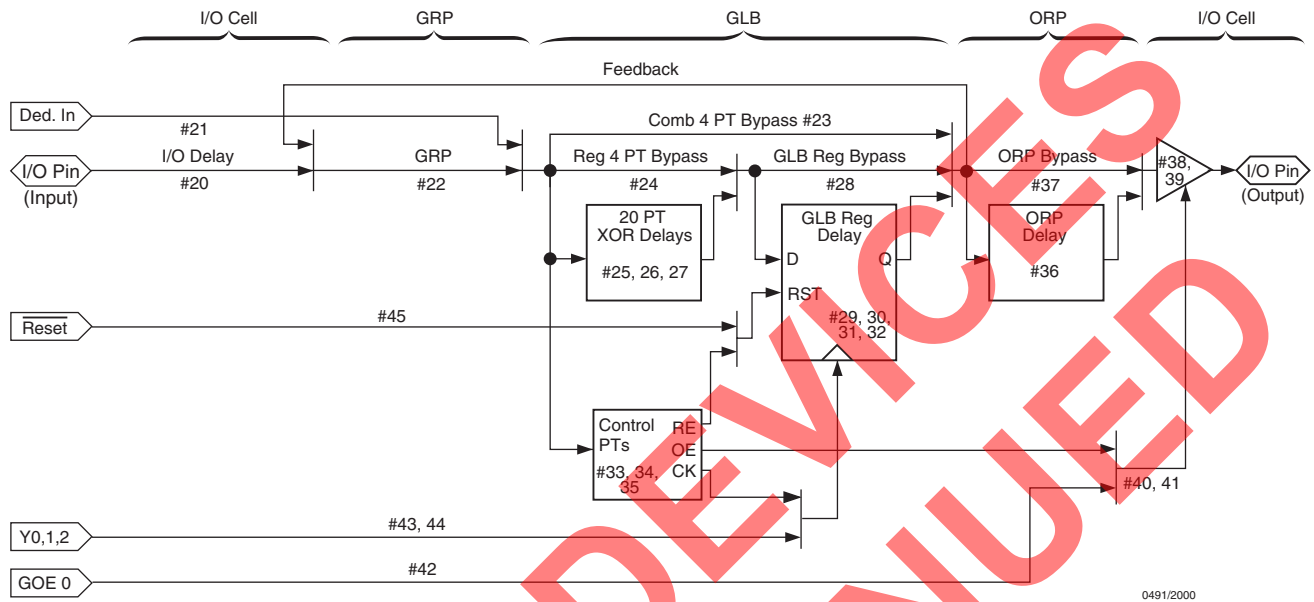
### Derivations of tsu, th and tco from the Product Term Clock

$$t_{su} = \text{Logic} + \text{Reg su} - \text{Clock (min)}$$
$$= (t_{io} + t_{grp} + t_{20ptxor}) + (t_{gsu}) - (t_{io} + t_{grp} + t_{ptck(min)})$$
$$= (\#20 + \#22 + \#26) + (\#29) - (\#20 + \#22 + \#35)$$
$$2.0ns = (0.4 + 0.6 + 1.9) + (0.5) - (0.4 + 0.6 + 0.4)$$

$$t_{h} = \text{Clock (max)} + \text{Reg h} - \text{Logic}$$
$$= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gh}) - (t_{io} + t_{grp} + t_{20ptxor})$$
$$= (\#20 + \#22 + \#35) + (\#30) - (\#20 + \#22 + \#26)$$
$$1.9ns = (0.4 + 0.6 + 2.3) + (1.5) - (0.4 + 0.6 + 1.9)$$

$$t_{co} = \text{Clock (max)} + \text{Reg co} + \text{Output}$$
$$= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$$
$$= (\#20 + \#22 + \#35) + (\#31) + (\#36 + \#38)$$
$$5.2ns = (0.4 + 0.6 + 2.3) + (0.3) + (0.6 + 1.0)$$

Note: Calculations are based on timing specifications for the ispLSI 2032VE-300L.

Table 2-0042/2032VE

## Power Consumption

Power consumption in the ispLSI 2032VE device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**
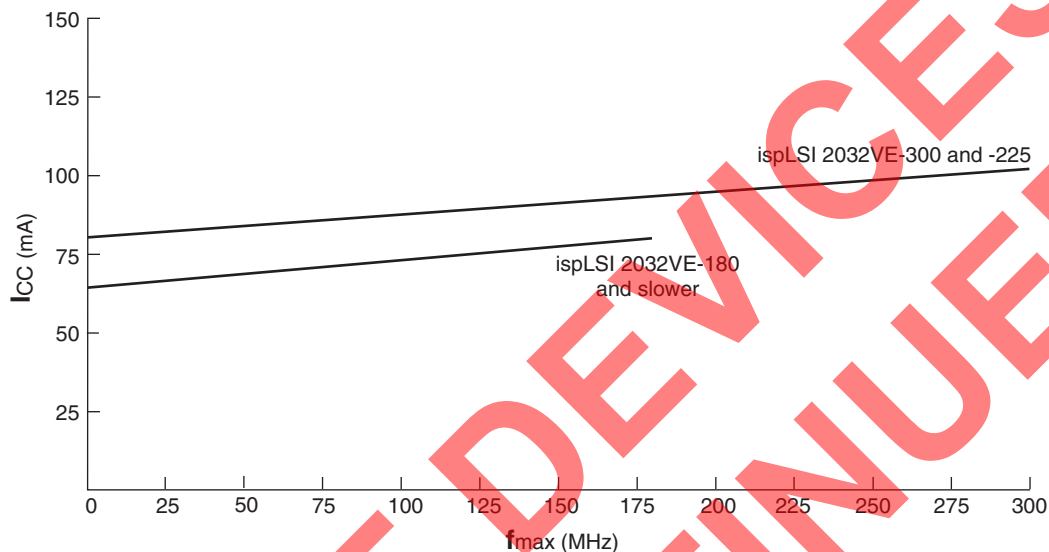


Notes: Configuration of two 16-bit counters
Typical current at 3.3V, 25° C

$I_{CC}$ can be estimated for the ispLSI 2032VE using the following equation:

For ispLSI 2032VE-300 and -225:  $I_{CC}(mA) = 4.5 + (\text{\# of PTs} * 1.29) + (\text{\# of nets} * Fmax * 0.0068)$

For ispLSI 2032VE-180 and slower:  $I_{CC}(mA) = 4.5 + (\text{\# of PTs} * 1.05) + (\text{\# of nets} * Fmax * 0.0068)$

Where:
   # of PTs = Number of product terms used in design
   # of nets = Number of signals used in device
   Max freq = Highest clock frequency to the device (in MHz)

The $I_{CC}$ estimate is based on typical conditions ($V_{CC}$ = 3.3V, room temperature) and an assumption of two GLB loads on average exists.  These values are for estimates only.  Since the value of $I_{CC}$ is sensitive to operating conditions and the program in the device, the actual $I_{CC}$ should be verified.

0127A/2032VE

## Signal Descriptions

| Signal Name | Description |
|---|---|
| GOE 0 | Global Output Enable input pin |
| Y0 | Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs in the device. |
| RESET/Y1 | This pin performs two functions: (1) Active Low (0) Reset pin which resets all of the registers in the device. (2) Dedicated Clock input. |
| BSCAN | Input – Dedicated in-system programming Boundary Scan enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active. |
| TDI/IN 0 | Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a serial data input pin to load programming data into the device. (2) When BSCAN is high, it functions as a dedicated input pin. |
| TMS/NC[1] | Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a mode control pin for the Boundary Scan state machine. (2) When BSCAN is high, this pin is not to be connected to any active signals, VCC or GND. |
| TDO/IN 1 | Output/Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as an output pin to read serial shift register data. (2) When BSCAN is high, it functions as a dedicated input pin. |
| TCK/Y2 | Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a clock pin for the Boundary Scan state machine. (2) When BSCAN is high, it functions as a Dedicated Clock input. |
| GND | Ground (GND) |
| VCC | Vcc |
| NC[1] | No Connect |
| I/O | Input/Output pins – These are the general purpose I/O pins used by the logic array. |

## Signal Locations

| Signal | 44-Pin TQFP | 44-Pin PLCC | 48-Pin TQFP | 49-Ball caBGA |
|---|---|---|---|---|
| GOE 0 | 40 | 2 | 43 | A4 |
| Y0 | 5 | 11 | 5 | C1 |
| RESET/Y1 | 29 | 35 | 31 | D7 |
| BSCAN | 7 | 13 | 7 | D1 |
| TDI/IN 0 | 8 | 14 | 8 | E2 |
| TMS/NC[1] | 30 | 36 | 32 | C6 |
| TDO/IN 1 | 18 | 24 | 19 | G4 |
| TCK/Y2 | 27 | 33 | 29 | E7 |
| GND | 17, 39 | 1, 23 | 18, 42 | C4, E4 |
| VCC | 6, 28 | 12, 34 | 6, 30 | D3, D5 |
| NC[1] | — | — | 12, 24, 36, 48 | A1, A7, D4, G1, G7 |

## I/O Locations

| Signal | 44-Pin TQFP | 44-Pin PLCC | 48-Pin TQFP | 49-Ball caBGA |
|---|---|---|---|---|
| I/O 0 - I/O 6 | 9, 10, 11, 12, 13, 14, 15 | 15, 16, 17, 18, 19, 20, 21 | 9, 10, 11, 13, 14, 15, 16 | E1, F2, F1, E3, F3, G2, F4 |
| I/O 7 - I/O 13 | 16, 19, 20, 21, 22, 23, 24 | 22, 25, 26, 27, 28, 29, 30 | 17, 20, 21, 22, 23, 25, 26 | G3, F5, G5, F6, G6, E5, E6 |
| I/O 14 - I/O 20 | 25, 26, 31, 32, 33, 34, 35 | 31, 32, 37, 38, 39, 40, 41 | 27, 28, 33, 34, 35, 37, 38 | F7, D6, C7, B6, B7, C5, B5 |
| I/O 21 - I/O 27 | 36, 37, 38, 41, 42, 43, 44 | 42, 43, 44, 3, 4, 5, 6 | 39, 40, 41, 44, 45, 46, 47 | A6, B4, A5, B3, A3, B2, A2 |
| I/O 28 - I/O 31 | 1, 2, 3, 4 | 7, 8, 9, 10 | 1, 2, 3, 4 | C3, C2, B1, D2 |

1. NC pins are not to be connected to any active signals, VCC or GND.
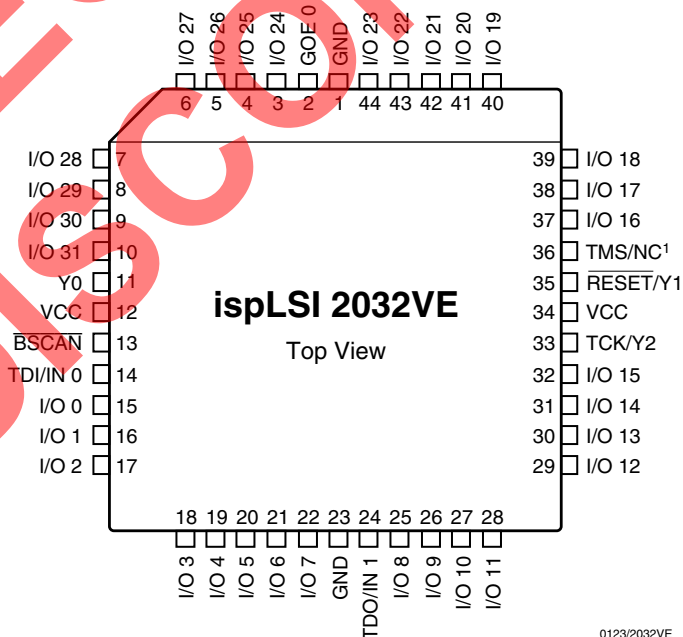
## Pin Configuration

**ispLSI 2032VE 44-Pin TQFP Pinout Diagram (0.8mm Lead Pitch/10.0 x 10.0mm Body Size)**
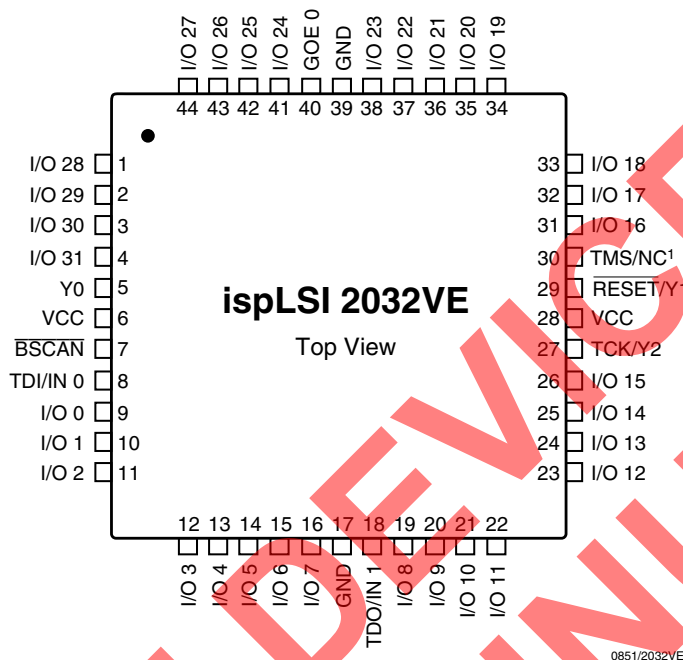


1. NC pins are not to be connected to any active signals, VCC or GND.
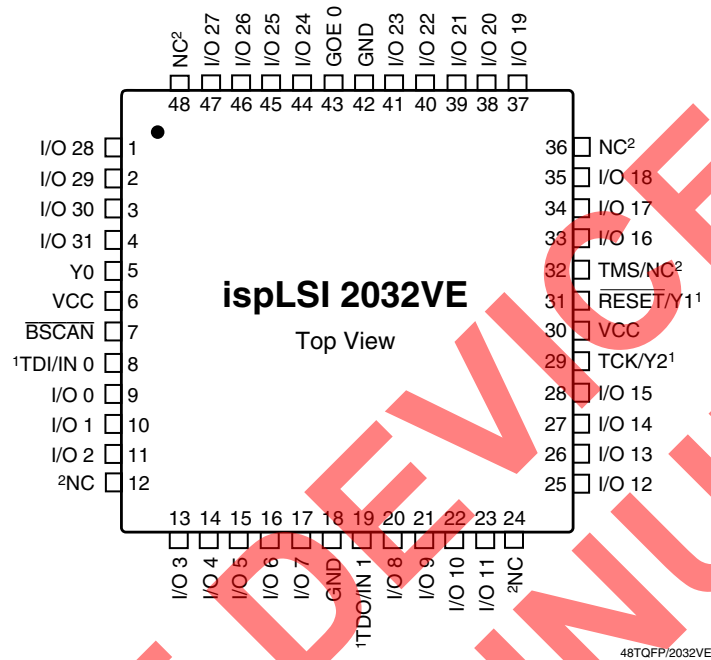
## Pin Configuration

**ispLSI 2032VE 44-Pin PLCC Pinout Diagram (0.5in Lead Pitch/0.65 x 0.65in Body Size)**



1. NC pins are not to be connected to any active signals, VCC or GND.

**Lattice**
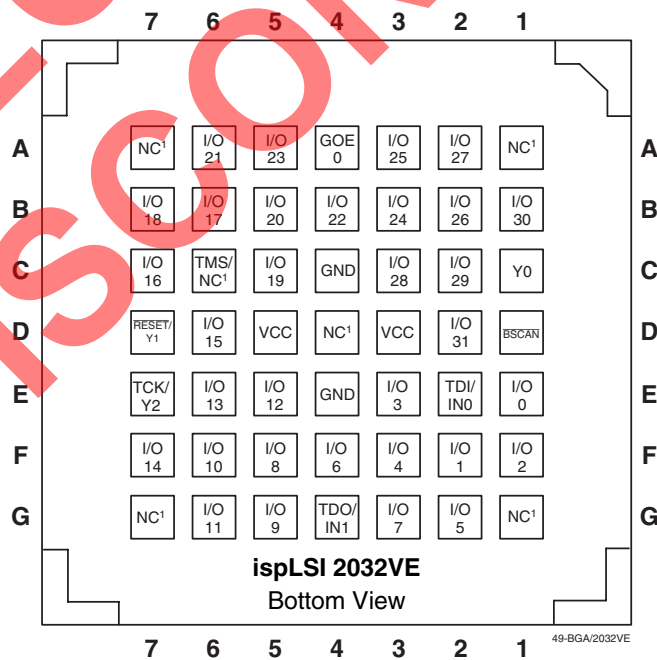Semiconductor
Corporation

## Pin Configuration

**ispLSI 2032VE 48-Pin TQFP Pinout Diagram (0.5mm Lead Pitch/7.0 x 7.0mm Body Size)**



Top pins (48–37): NC[2], I/O 27, I/O 26, I/O 25, I/O 24, GOE 0, GND, I/O 23, I/O 22, I/O 21, I/O 20, I/O 19

Left pins (1–12): I/O 28, I/O 29, I/O 30, I/O 31, Y0, VCC, BSCAN, [1]TDI/IN 0, I/O 0, I/O 1, I/O 2, [2]NC

Right pins (36–25): NC[2], I/O 18, I/O 17, I/O 16, TMS/NC[2], RESET/Y1[1], VCC, TCK/Y2[1], I/O 15, I/O 14, I/O 13, I/O 12

Bottom pins (13–24): I/O 3, I/O 4, I/O 5, I/O 6, I/O 7, GND, [1]TDO/IN 1, I/O 8, I/O 9, I/O 10, I/O 11, [2]NC

ispLSI 2032VE

48TQFP/2032VE

1. Pins have dual function capability.
2. NC pins are not to be connected to any active signals, V$_{CC}$ or GND.

## Signal Configuration

**ispLSI 2032VE 49-Ball caBGA Signal Diagram (0.8mm Lead Pitch/7.0 x 7.0mm Body Size)**



| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|
| A | NC[1] | I/O 21 | I/O 23 | GOE 0 | I/O 25 | I/O 27 | NC[1] | A |
| B | I/O 18 | I/O 17 | I/O 20 | I/O 22 | I/O 24 | I/O 26 | I/O 30 | B |
| C | I/O 16 | TMS/NC[1] | I/O 19 | GND | I/O 28 | I/O 29 | Y0 | C |
| D | RESET/Y1 | I/O 15 | VCC | NC[1] | VCC | I/O 31 | BSCAN | D |
| E | TCK/Y2 | I/O 13 | I/O 12 | GND | I/O 3 | TDI/IN0 | I/O 0 | E |
| F | I/O 14 | I/O 10 | I/O 8 | I/O 6 | I/O 4 | I/O 1 | I/O 2 | F |
| G | NC[1] | I/O 11 | I/O 9 | TDO/IN1 | I/O 7 | I/O 5 | NC[1] | G |

ispLSI 2032VE
Bottom View

49-BGA/2032VE

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

13

**Lattice**
Semiconductor
Corporation

## Part Number Description

ispLSI  2032VE – XXX  X  XXXX  X

**Device Family**

**Device Number**
2032VE

**Speed**
300 = 300 MHz **f**max
225 = 225 MHz **f**max
180 = 180 MHz **f**max
135 = 135 MHz **f**max
110 = 110 MHz **f**max

**Grade**
Blank = Commercial
I = Industrial

**Package**
T44 = 44-Pin TQFP
T48 = 48-Pin TQFP
J44 = 44-Pin PLCC
B49 = 49-Ball caBGA
TN44 = Lead-Free 44-Pin TQFP
TN48 = Lead-Free 48-Pin TQFP

**Power**
L = Low
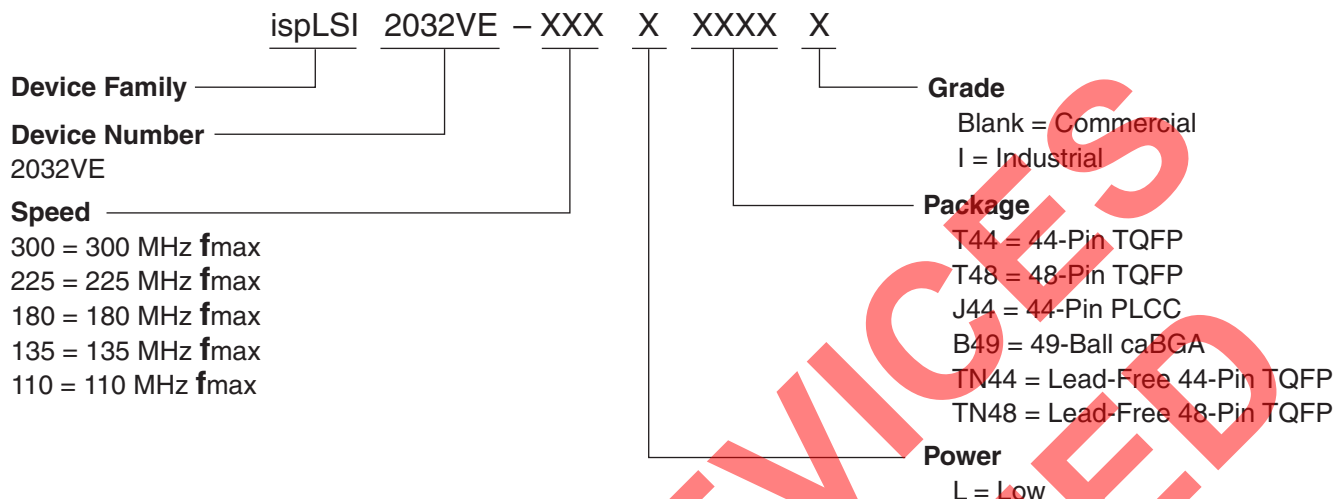
## ispLSI 2032VE Ordering Information

**Conventional Packaging**

**COMMERCIAL**

| FAMILY | **f**max (MHz) | **t**pd (ns) | ORDERING NUMBER | PACKAGE |
|--------|------|------|-----------------|---------|
| | 300 | 3.0 | ispLSI 2032VE-300LT44 | 44-Pin TQFP |
| | 300 | 3.0 | ispLSI 2032VE-300LT48 | 48-Pin TQFP |
| | 300 | 3.0 | ispLSI 2032VE-300LB49 | 49-Ball caBGA |
| | 225 | 4.0 | ispLSI 2032VE-225LT44* | 44-Pin TQFP |
| | 225 | 4.0 | ispLSI 2032VE-225LT48* | 48-Pin TQFP |
| | 225 | 4.0 | ispLSI 2032VE-225LJ44 | 44-Pin PLCC |
| | 225 | 4.0 | ispLSI 2032VE-225LB49* | 49-Ball caBGA |
| | 180 | 5.0 | ispLSI 2032VE-180LT44 | 44-Pin TQFP |
| | 180 | 5.0 | ispLSI 2032VE-180LT48 | 48-Pin TQFP |
| **ispLSI** | 180 | 5.0 | ispLSI 2032VE-180LJ44 | 44-Pin PLCC |
| | 180 | 5.0 | ispLSI 2032VE-180LB49 | 49-Ball caBGA |
| | 135 | 7.5 | ispLSI 2032VE-135LT44 | 44-Pin TQFP |
| | 135 | 7.5 | ispLSI 2032VE-135LT48 | 48-Pin TQFP |
| | 135 | 7.5 | ispLSI 2032VE-135LJ44 | 44-Pin PLCC |
| | 135 | 7.5 | ispLSI 2032VE-135LB49 | 49-Ball caBGA |
| | 110 | 10 | ispLSI 2032VE-110LT44 | 44-Pin TQFP |
| | 110 | 10 | ispLSI 2032VE-110LT48 | 48-Pin TQFP |
| | 110 | 10 | ispLSI 2032VE-110LJ44 | 44-Pin PLCC |
| | 110 | 10 | ispLSI 2032VE-110LB49 | 49-Ball caBGA |

*2032VE-300 recommended for new designs

Table 2-0041A/2032VE

**INDUSTRIAL**

| FAMILY | **f**max (MHz) | **t**pd (ns) | ORDERING NUMBER | PACKAGE |
|--------|------|------|-----------------|---------|
| **ispLSI** | 180 | 5.0 | ispLSI 2032VE-180LT44I | 44-Pin TQFP |

Table 2-0041B/2032VE

## ispLSI 2032VE Ordering Information (Cont.)

**Lead-Free Packaging**

### COMMERCIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|---|---|---|---|---|
| ispLSI | 300 | 3.0 | ispLSI 2032VE-300LTN44 | Lead-Free 44-Pin TQFP |
| | 300 | 3.0 | ispLSI 2032VE-300LTN48 | Lead-Free 48-Pin TQFP |
| | 180 | 5.0 | ispLSI 2032VE-180LTN44 | Lead-Free 44-Pin TQFP |
| | 180 | 5.0 | ispLSI 2032VE-180LTN48 | Lead-Free 48-Pin TQFP |
| | 135 | 7.5 | ispLSI 2032VE-135LTN44 | Lead-Free 44-Pin TQFP |
| | 135 | 7.5 | ispLSI 2032VE-135LTN48 | Lead-Free 48-Pin TQFP |
| | 110 | 10 | ispLSI 2032VE-110LTN44 | Lead-Free 44-Pin TQFP |
| | 110 | 10 | ispLSI 2032VE-110LTN48 | Lead-Free 48-Pin TQFP |

### INDUSTRIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|---|---|---|---|---|
| ispLSI | 180 | 5.0 | ispLSI 2032VE-180LTN44I | Lead-Free 44-Pin TQFP |

## Revision History

| Date | Version | Change Summary |
|---|---|---|
| — | 10 | Previous Lattice release. |
| August 2006 | 11 | Updated for 48-pin TQFP lead-free package option. |