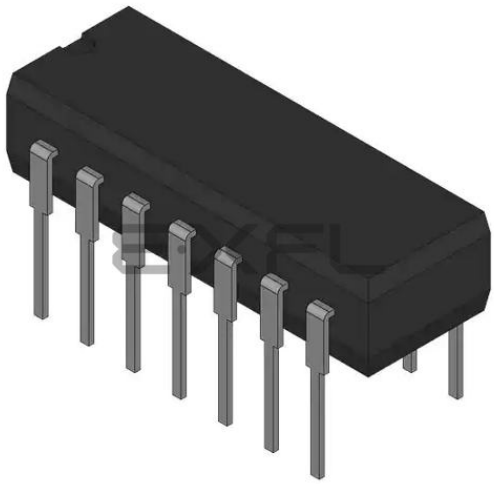

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Supplier Device Package	14-DIP
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List of Tables

Table 5. ADCNTRL1 Register Bit Definitions

ADCNTRL1 Register (addr. 0x9F)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
APND	AINTEN	ASTART	REFSEL	ACHSEL[3:0]			

Bit	Description
APND	(0) ADC's pending flag is cleared.
	(1) ADC's pending flag is triggered.
AINTEN	(0) Disables ADC hardware interrupts.
	(1) Enables ADC hardware interrupts.
ASTART	(0) ADC conversion is not in progress.
	(1) Start an ADC conversion / ADC conversion in progress.
REFSEL	(0) ADC Reference (V_{AREF}) = Internal V_{REF}
	(1) ADC Reference (V_{AREF}) = Vcc
ACHSEL[3:0]	Analog Input Channel Selection Bits. Refer to Table 6 for details.

Table 6. Analog Input Channel Selection (ACHSEL[3:0]) Bit Definitions

ACHSEL[3]	ACHSEL[2]	ACHSEL[1]	ACHSEL[0]	Analog Channel	I/O Equiv.
0	0	0	0	ACH1	G4/AIN0
0	0	0	1	ACH2	G3/AIN1
0	0	1	0	ACH3	G2/AIN2
0	0	1	1	ACH4	G1/AIN3
1	0	0	0	ACH5	G7/AIN4/A_{OUT}
1	0	0	1	GND	-
1	0	1	0	+V_{REF}	-
1	1	0	0	Vcc/3	-

4.1.2 ADCNTRL2 Register

The ADCNTRL2 is an 8-bit memory map register used to configure the analog circuits. Six of the eight register bits are used to configure circuits directly related to the ADC circuit while the others are not related.

Bit 7 (REFBY2) of the ADCNTRL2 register is the reference clock (F_{RCLK1}) divide-by-2 enable bit. The REFBY2 bit configures the reference clock of the PLL and Programmable Comparator circuit to be sourced either by F_{RCLK1} or $F_{RCLK1}/2$ clock. Refer to the Clock Circuit section of the datasheet for additional details.

Bit 6 (COMPSEL) of the ADCNTRL2 register is the Programmable Comparator's non-inverting input selection bit. If COMPSEL=0, the non-inverting input of the Programmable Comparator is the G4/AIN0 device pin. If COMPSEL=1, the non-inverting input of the Programmable Comparator is the G2/AIN2 device pin. Before enabling the Programmable Comparator circuit, the selected analog input port pin must be configured as a tri-state input bypassing the I/O circuitry.[9] Refer to the Programmable Comparator Circuit section of the datasheet for addition details.

Bit 5 of the ADCNTRL2 register is the Uncommitted Amplifier Enable (ENAMP) bit. If ENAMP=0, the Uncommitted Amplifier circuit is disabled and its pin connections (G6/-A_{IN} and G7/A_{OUT}) may be used as normal I/O ports. The G7/AIN4 pin may still be used as a standard ADC conversion input through the analog ACH5 channel. If ENAMP=1, the Uncommitted Amplifier circuit is enabled and its pin connections must be configured as tri-state inputs where G6/-A_{IN} is the inverting input and G7/A_{OUT} is the amplifier output.[9] If the ADC circuit is performing a conversion on the analog ACH5 input when driven by the Uncommitted Amplifier, software must avoid clearing the ENAMP bit. Refer to the following Uncommitted Amplifier section for additional details.

Bit 4 (ENDAS) of the ADCNTRL2 register enables the ADC conversion's gated auto-sampling operating mode. If ENDAS=1, the ADC circuit configures the F_{ADCLK} clock for synchronization with the PWM Timer 1's ADSTROBE output signal. The ADC circuit will then accept triggers by the active (on) edge transition of the ADSTROBE signal. All other ADC configuration

options must be prepared prior to setting the ENDAS bit. Refer to the following ADC Gated Auto-sampling Mode section for additional details. The ADSTROBE signal is generated by the PWM Timer 1 circuit and is configured using its T1CMPB and T1RA registers. Refer to the PWM Timer 1 Circuit section of the datasheet for details regarding its operation. If ENDAS=0, the ADC circuit is configured to accept only ADC start commands issued by software when setting the ASTART bit of the ADCNTRL1 register to 1. Refer to the following ADC Conversion Modes section for additional details.

Bits 3 and 2 (ASPEED[1:0]) of the ADCNTRL2 register selects the divide factor (1, 2, 4, or 8) to slow the F_{ADCLK} clock extending the ADC conversion cycle time. In most cases, the F_{ADCLK} clock division is performed to improve the ADC conversion accuracy. Refer to the following ADC Conversion Clock Configuration section for addition details.

Bit 1 of the ADCNTRL2 register is the Current Source Generator Enable (ENIS) bit. If ENIS=0, the Current Source Generator circuit is disabled and its G3/AIN1 pin may be used as a normal I/O port or as a standard ADC conversion input through the analog ACH2 channel. If ENIS=1, the Current Source Generator circuit is enabled and its pin connection must be configured as a tri-state input bypassing the I/O circuitry.[9] If the ADC circuit is performing a conversion on the analog ACH2 input when driven by the Current Source Generator, software must avoid clearing the ENIS bit. Refer to the following Current Source Generator section for additional details.

Bit 0 (GAIN) of the ADCNTRL2 register is the autozero amplifier enable bit. If GAIN=0, the autozero amplifier with its gain 16 circuitry is disabled where its G4/AIN0 pin connections may be used as a normal I/O port. The G4/AIN0 pin may still be used as a standard ADC conversion input through the analog ACH1 channel. If GAIN =1, the autozero amplifier with its gain 16 circuitry is enabled and its G4/AIN0 pin connection must be configured as a tri-state input where G4/AIN0 is the non-inverting and SR_GND is the inverting input of the amplifier.[9] Software may write to the GAIN bit at any time; however, the actual GAIN enable signal will not change while an ADC conversion is in progress. If a read command is issued while a conversion is in progress, the current value of the GAIN bit may not necessarily reflect the actual state of the GAIN enable signal. The last value of the GAIN bit written by software at the time of the ADC conversion trigger, dictates the state of the GAIN enable signal for the triggered ADC conversion cycle. Refer to the following Autozero Amplifier section for additional details.

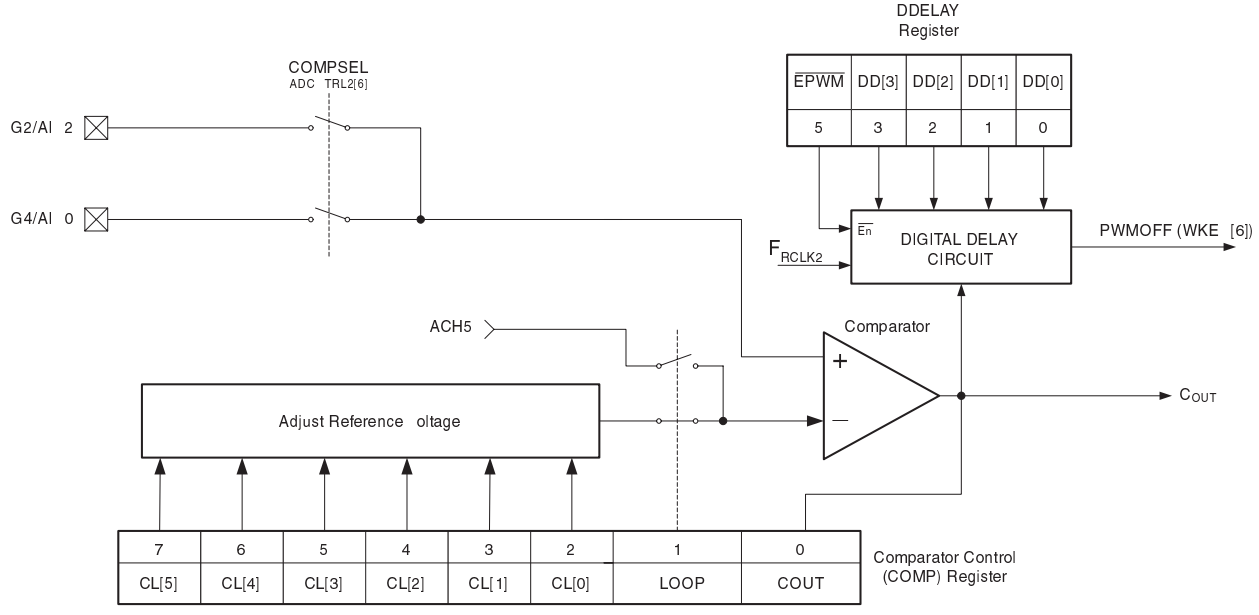
Bits 7-2 (CL[5:0]) is the comparator voltage threshold level selection bits of the Comparator Control (COMP) register. The CL bits may be programmed to select one of the voltage threshold levels as the inverting input of the analog comparator. Refer to Table 9 and Table 10 for a detailed list of voltages.

Bit 1 of the Comparator Control (COMP) register is the Programmable Comparator circuit's voltage loop (VLOOP) configuration enable bit. If VLOOP=0, the Programmable Comparator circuit is configured to compare the analog G4/AIN0 or G2/AIN2 input (COMPSEL=0 or 1) to one of the 63 voltage threshold levels. If VLOOP=1, enables the voltage loop configuration where the analog G4/AIN0 or G2/AIN2 input (COMPSEL=0 or 1) to the Uncommitted (Error) Amplifier output (A_{OUT}).

Bit 7 of the Digital Delay (DDELAY) register is the Programmable Comparator circuit enable (COMPEN) bit. If COMPEN=0, the Programmable Comparator circuit is disabled and the C_{OUT} signal is low. If COMPEN=1, the Programmable Comparator circuit is enabled and the C_{OUT} signal generated by the comparison of the two inputs.

The comparator output (C_{OUT}) signal is latched by the main system instruction (F_{ICLK}) clock into bit 0 (COUT) of the Comparator Control (COMP) register. Software may only read the COUT bit to monitor the comparator's activity. The COUT bit cannot cause a microcontroller hardware interrupt or perform any other action.

Figure 8. Programmable Comparator Block Diagram (VLOOP = 0)



Bit 6 of the ADCNTRL2 register is the Programmable Comparator non-inverting input selection (COMPSEL) bit.[1] If COMPSEL=0, the non-inverting input of the Programmable Comparator is the G4/AIN0 device pin. If COMPSEL=1, the non-inverting input of the Programmable Comparator is the G2/AIN2 device pin. Before enabling the Programmable Comparator circuit, the selected analog input port pin must be configured as a tri-state input bypassing the I/O circuitry.[2]

Bit 1 of the Comparator Control (COMP) register is the Programmable Comparator circuit's voltage loop (VLOOP) configuration enable bit. If VLOOP=0, the Programmable Comparator circuit is configured to compare the analog G4/AIN0 or G2/AIN2 input (COMPSEL=0 or 1) to one of the 63 voltage threshold levels. If VLOOP=1, enables the voltage loop configuration where the analog G4/AIN0 or G2/AIN2 input (COMPSEL=0 or 1) to the Uncommitted (Error) Amplifier output (A_{OUT}).

Bit 7 of the Digital Delay (DDELAY) register is the Programmable Comparator circuit enable (COMPEN) bit. If COMPEN=0, the Programmable Comparator circuit is disabled and the C_{OUT} signal is low. If COMPEN=1, the Programmable Comparator circuit is enabled and the C_{OUT} signal generated by the comparison of the two inputs.

Bit 0 (COUT) of the Comparator Control (COMP) register is the latched comparator output (C_{OUT}) signal. If the Programmable Comparator circuit is enabled, the C_{OUT} signal is latched by the main system instruction (F_{ICLK}) clock into the COUT bit of the COMP register. Software may only read the COUT bit to monitor the comparator's activity. The COUT bit cannot cause any microcontroller hardware interrupt or any other actions.

Figure 9. Programmable Comparator Block Diagram (VLOOP = 1)

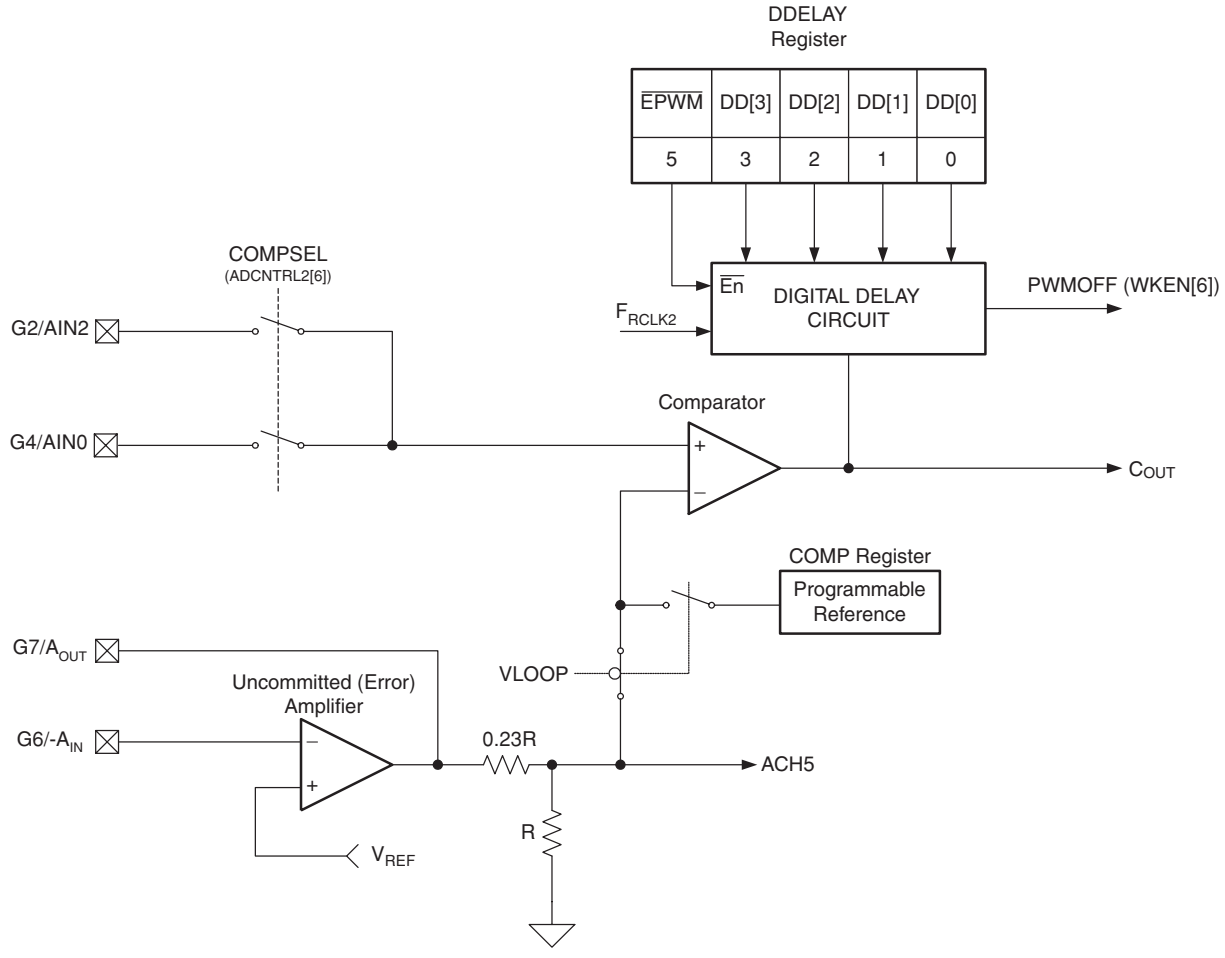
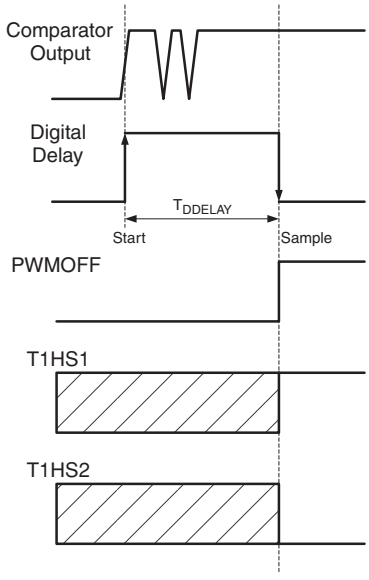


Table 11. Digital Delay (DDELAY) Register Bit Definitions

DDELAY Register (addr. 0xA2)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
COMPEN	PWMINT	EPWM	OFFMODE	DD[3:0]			

Bit	Description
COMPEN	(0) Disable the Programmable Comparator circuit. (1) Enable the Programmable Comparator circuit.
PWMINT	(0) The input of the G6 MIW circuit network is the G6/-A_{IN} device pin. (1) The input of the G6 MIW circuit network is the PWMOFF output signal (not the G6/-A_{IN} device pin).
EPWM	(0) Enables the Digital Delay Filter circuit. The PWMOFF output is triggered by C_{OUT} after the programmed delay (T_{DDELAY}). (1) Disables the Digital Delay Filter circuit and the PWMOFF output signal.
OFFMODE	(0) PWM outputs switched off and Timer 1 stops after a comparator detection with delay. (1) PWM outputs switched off for the current PWM cycle only.
DD[3:0]	Digital delay after C_{OUT} triggers high, T_{DDELAY} = DD • ($1/F_{RCLK2}$)

Figure 10. Digital Delay Timing



1. Refer to the ADC Circuit section of the datasheet for additional details.
2. Refer to the I/O Ports section of the datasheet for details.
3. Hardware interrupts are not executed by the microcontroller core unless the Global Interrupt enable (G) flag of the Status register is set. Refer to the 8-Bit Microcontroller Core section of the datasheet for details.
4. Refer to the Clock Circuit section of the datasheet for details regarding the F_{RCLK2} clock.

Table 16. Timer 1 Control (T1CNTRL) Register Bit Definitions

T1CNTRL Register (addr. 0xAE)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
T1C3	T1C2	T1C1	T1C0	T1PND	T1EN	X	T1BOUT

Bit	Description
T1C3	Timer 1 Mode Configuration Bit. Refer to Table 17 for details.
T1C2	Timer 1 Mode Configuration Bit. Refer to Table 17 for details.
T1C1	Timer 1 Mode Configuration Bit. Refer to Table 17 for details.
T1C0	PWM Mode (0) Stop the PWM Timer 1 circuit. (1) Start the PWM Timer 1 circuit.
	Input Capture Mode (0) Timer 1's TMR1 overflow pending flag is cleared. (1) Timer 1's TMR1 overflow pending flag is triggered.
T1PND	PWM Mode (0) Timer 1's TMR1 overflow pending flag is cleared. (1) Timer 1's TMR1 overflow pending flag is triggered.
	Input Capture Mode (0) Timer 1 capture pending flag is cleared. (1) Timer 1 capture pending flag is triggered.
T1EN	(0) Disables Timer 1 hardware interrupts. (1) Enables Timer 1 hardware interrupts.
T1BOUT	(0) Retain normal I/O function of the G1/AIN3 pin. (1) Enables Timer 1's ADSTROBE output to be sent to the G1 output port.

Table 17. Timer 1 Mode Configuration Bits

T1C3	T1C2	T1C1	Timer Mode Source	Interrupt	Timer count on
0	0	0	PWM mode no output toggle	TMR1 Overflow	Prescaler Input
0	1	1	PWM mode T1HS1 and T1HS2 toggle	TMR1 Overflow	Prescaler Input
0	0	1	PWM mode T1HS1 toggle	TMR1 Overflow	Prescaler Input
0	1	0	PWM mode T1HS2 toggle	TMR1 Overflow	Prescaler Input
1	0	0	Capture mode no T1HS1 toggle	TMR1 Overflow T1HS2 rising-edge	Prescaler Input
1	0	1	Capture mode with T1HS1 toggle	TMR1 Overflow T1HS2 rising-edge	Prescaler Input
1	1	0	Capture mode no T1HS1 toggle	TMR1 Overflow T1HS2 falling-edge	Prescaler Input
1	1	1	Capture mode with T1HS1 toggle	TMR1 Overflow T1HS2 falling-edge	Prescaler Input

6.2 Pulse Width Modulation (PWM) Mode

In PWM Mode, the Timer 1 circuit may be configured to generate pulses of a specified duty cycle and period on the T1HS1 (G0), T1HS2 (G5), and/or ADSTROBE (G1) timer outputs. The 12-bit TMR1 counter increments at the F_{T1CLK} clock rate defined by the FSEL bit of the PSCALE register. Refer to the previous PSCALE Register and Timer 1 Clock Configuration section of the datasheet for details.

A PWM cycle begins with the TMR1 counter incrementing from 0x000 until it matches the value stored in the T1RA register. At this point, the TMR1 counter completes its T1RA count and overflows (a transitions from T1RA to 0x000) setting the T1PND flag of the T1CNTRL register ending the PWM cycle. The Timer 1 circuit has two additional TMR1 compare (T1CMPA and T1CMPB) registers used to generate the T1HS1, T1HS2, and ADSTROBE output signals. All three output signals are initialized to a resting (off) state. Once the TMR1 counter is enabled (by setting the T1C0 bit of the T1CNTRL register), both compare registers are matched against the incrementing TMR1 counter. When the TMR1 completes its count equal to the value stored in the T1CMPA and T1CMPB registers, the T1HS1, T1HS2, and ADSTROBE output signals are set to an active (on) state until the TMR1 counter matches the value stored in the T1RA compare register (overflows). Once the TMR1 counter overflows, the output signals are cleared returning them to a resting (off) state. Refer to Figure 11 for a Timer 1 PWM Mode block diagram.

The PWM Timer 1 can be programmed to toggle one or both PWM output signals (T1HS1 and T1HS2) to support a variety of output configurations (half bridge, full bridge,[8] low side or high side driving). These outputs may be used to drive an external half-bridge driver and are enabled by programming the T1C1 and T1C2 bits in the T1CNTRL register (see Table 16). The T1HS1 (G0) and T1HS2 (G5) output signals may be configured with opposite phases and dead time controlled edges (see Figure 12). The phases of the output signals are configured by the bits of the PORTGD I/O configuration register.[9] Upon device power-up, the T1HS1 and T1HS2 signals may be programmed to default as active high/low outputs by the default I/O configuration register bits in the non-volatile Initialization Register 4.[10] Both G0/T1HS1 and G5/T1HS2 pins will configure to their programmed default state after T_{DIO}[2] from the system reset trigger (e.g. from a POR). The G0/T1HS1 and G5/T1HS2 pins may both be configured as outputs with common or opposite phases. If configured as outputs, the PORTGD[0] and PORTGD[5] bits configure the T1HS1 and T1HS2 signals as active high or low. If the PORTGD bit is 0, the output signal is active high, otherwise it is active low. The PORTGD[1] bit also configures the G1/ADSTROBE pin as an active high/low signal once configured as an output. The Initialization Register 4 bits only default the G0/T1HS1 and G5/T1HS2 pins not the G1/ADSTROBE pin. From factory, the G0/T1HS1, G5/T1HS2 and G1/ADSTROBE device pins are defaulted as tri-stated inputs. The pins must be configured by the Initialization Register 4 bits or by software directly through the PORTGC and PORTGD register as an output port before enabling the TMR1 counter and its outputs.

The dead time counter of the Timer 1 circuit controls the dead time (T_{DT}) delay between the T1HS1 and T1HS2 output edge transitions through the DT[4:0] bits of the DTIME register. The dead time counter delay is first triggered after the TMR1 counter equals to the T1CMPA value and the T1HS1 signal transitions from its resting (off) to its active (on) state. Once the programmed T_{DT} completes, the T1HS2 signal then transitions from its resting (off) to its active (on) state. The dead time counter delay is triggered for a second time after the TMR1 counter equals to the T1RA value and the T1HS2 signal transitions from its active (on) to its resting (off) state. Once the programmed T_{DT} completes, the T1HS1 signal then transitions from its active (on) to its resting (off) state ending the PWM cycle. The PWM cycle is considered complete once the TMR1 counter completes the T1RA count plus T_{DT} even in the T1HS1 and T1HS2 outputs are disabled.

The T1HS1 and T1HS2 PWM output signals may be programmed to be automatically disabled by the output of the digital filter (PWMOFF) in Programmable Comparator circuit. The output may be programmed to disable the Timer 1 circuit completely or disable only the current PWM cycle. Refer to the Programmable Comparator Circuit section of the datasheet for details.

The Timer 1's ADSTROBE output signal may be configured as the G1/ADSTROBE device output if the T1BOUT bit of the T1CNTRL register is set. The ADSTROBE signal, however, is always generated by the Timer 1 circuit. Initially, the ADSTROBE begins its PWM cycle at its resting (off) state and transitions to its active (on) state once the TMR1 counter completes its count equal to the T1CMPB value. The active (on) edge transition of the ADSTROBE output may be programmed to automatically trigger an ADC conversion cycle if the ENDAS bit of the ADCNTRL2 register is set. Refer to the ADC Circuit section of the datasheet for details.

The T1PND bit of the T1CNTRL register is set once the TMR1 counter completes the count equal to the T1RA value (overflows). Software may use the T1PND bit to monitor the PWM cycles and/or trigger microcontroller hardware interrupts (TMRI1) if the T1EN bit of the T1CNTRL register is set. Software must clear the T1PND bit in order to detect a new overflow condition and/or trigger a new interrupt.[6]

Figure 11. Timer 1's PWM Mode Block Diagram

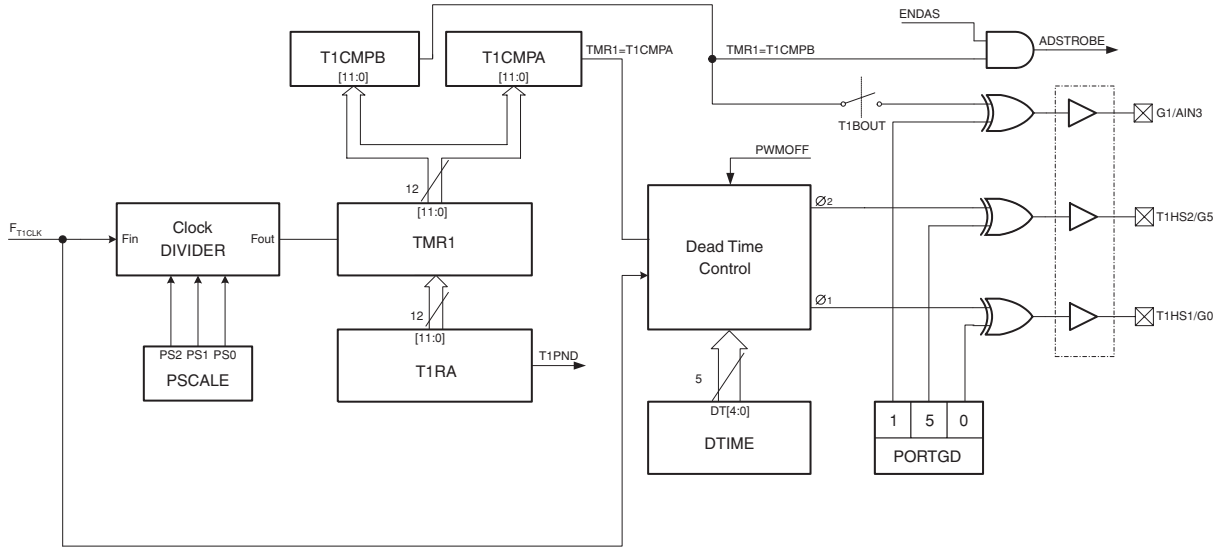
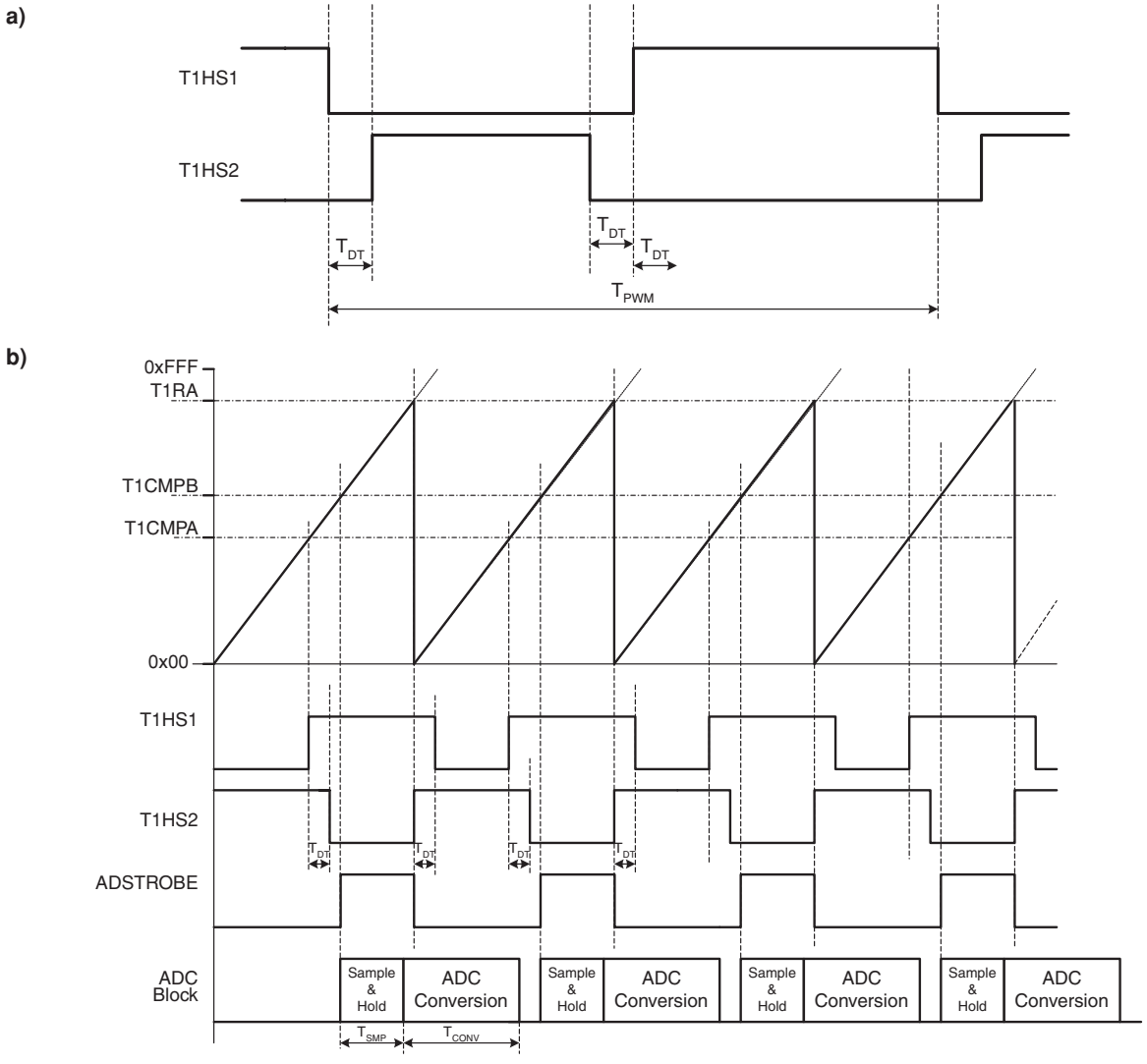


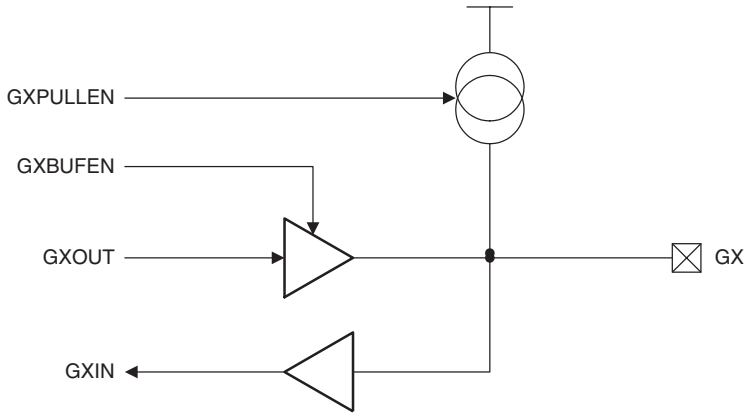
Figure 12. Example PWM Output Signals a) and b)



8 I/O Ports

The eight I/O pins (six on the 8-pin package option) are bi-directional (see Figure 14). The bi-directional I/O pins can be individually configured by software to operate as high-impedance inputs, as inputs with weak pull-up, or as push-pull outputs. The operating state is determined by the contents of the corresponding bits in the data and configuration registers. Each bi-directional I/O pin can be used for general purpose I/O, or in some cases, for a specific alternate function determined by the on-chip hardware.

Figure 14. PORTGD Logic Diagram



8.1 I/O Registers

The I/O pins (G0–G7) have three memory mapped port registers associated with the I/O circuitry: a Port Configuration (PORTGC), Port Data (PORTGD) and Port Input (PORTGP) register.[1] PORTGC is used to configure the pins as inputs or outputs. A pin may be configured as an input by writing a 0 or as an output by writing a 1 to its corresponding PORTGC bit. If a pin is configured as an output, its PORTGD bit represents the state of the pin (1 = logic high, 0 = logic low). If the pin is configured as an input, its PORTGD bit selects whether the pin is a weak pull-up or a high-impedance input. Table 20 provides details of the port configuration options. The port configuration and data registers can both be read from or written to. Reading PORTGP returns the value of the port pins regardless of how the pins are configured. Since this device supports MIW, all input ports have Schmitt triggers.

Upon power-up, the PORTGC and PORTGD registers are initialized to 0x00. However, the G0/T1HS1 and G5/T1HS2 pins may be defaulted to the different I/O configurations defined by the default I/O configuration bits of the Initialization Register 4. Refer to Table 29 in the Device Memory section of the datasheet for details.

Table 20. I/O Register Bit Assignments

PORTGC, PORTGD, PORTGD Registers (addr. 0xB3, 0xB2, 0xB4)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
G7[2]	G6[2]	G5	G4	G3	G2	G1	G0

Table 21. I/O Configuration Options

PORTGC Bit	PORTGD Bit	Port Pin Configuration
0	0	High-impedance input (tri-state input)
0	1	Input with pull-up (weak one input)
1	0	Push-pull zero output
1	1	Push-pull one output

1. Refer to Table 30 of the Device Memory section of the datasheet for the detailed memory map.
2. Available only on the 14-pin package option.

10.1.1 Accumulator (A)

The Accumulator is a general-purpose 8-bit register that is used to hold data and results of arithmetic calculations or data manipulations.

10.1.2 X-Pointer (X)

The X-Pointer register allows for an 11-bit indexing value to be added to an 8-bit offset creating an effective address used for reading and writing among the memory space. This provides software with the flexibility of storing lookup tables in the code EEPROM memory space for the core's accessibility during normal operation.[1]

The microcontroller core allows software to access the entire 11-bit X-Pointer register using the special X-pointer instructions e.g. LD X, #040H (see Table 24). Software may also access the register through any of the memory mapped instructions using the XHI (X[10:8]) and XLO (X[7:0]) variables located at address 0xBE and 0xBF (see Table 30).

The X register is divided into two sections. The most significant bit (MSB) is write only and selects between the data (0x000 to 0x0FF) or program (0xC00 to 0xFFF) memory space. The 10 least significant bits (LSBs) represent the specific address location within the data or program memory space.

For example: If X[10] = 0, the LD A, [#0,X] instruction will take the data at address X[9:0] from the data memory space (0x000 to 0x0FF) and load it into A. However, if X[10] = 1 the LD A, [#0,X] instruction will take the data at address X[9:0] from the program memory space (0xC00 to 0xFFF) and load it into A.

The X register can also serve as a counter or temporary storage register. However, this is true only for the 10-LSBs since the MSB is dedicated for memory space selection.

10.1.3 Program Counter (PC)

The 10-bit Program Counter (PC) register contains the address of the next instruction to be executed. After a system reset, PC is initialized to 0xC00 and the microcontroller core begins executing the instruction program residing in the code EEPROM memory at the initialized PC value.

10.1.4 Stack Pointer (SP)

The microcontroller core has an automatic program stack with a 4-bit stack pointer. The stack can be initialized to any location between addresses 0x30-0x3F in SRAM. Normally, the stack pointer is initialized by one of the first instructions in an application program. After a reset, the stack pointer is defaulted to 0xF pointing to the top of the stack at address 0x3F.

The stack is configured as a data structure which decrements from high to low memory. Each time a new address is pushed onto the stack, the microcontroller core decrements the stack pointer by two. Each time an address is pulled from the stack, the microcontroller core increments the stack pointer is by two. At any given time, the stack pointer points to the next free location in the stack.

When a subroutine is called by a jump-to-subroutine (JSR) instruction, the instruction's address is automatically pushed onto the stack with the least significant byte first. When the subroutine is finished, a return-from-subroutine (RET) instruction is executed. The RET instruction pulls the previously stacked return address and loads it into the program counter. Instruction execution then continues at the pulled return address.

10.1.5 Status Register (SR)

The 8-bit Status Register (SR) contains four condition code indicators (C, H, Z, and N), a global interrupt (G) mask bit, and the data EEPROM write ready (R) flag. The condition codes are automatically updated by most instructions (see Table 25). All status register bits except for the global interrupt mask are read only when using direct, indirect, or indexed instructions. The carry and half carry bits may be written by using their special inherent (SC, RC, LDC, RRC and RLC) instructions. Software cannot restore SR using the traditional microcontroller methods. Refer to the Interrupt Handling section for additional details.

Carry/Borrow (C)

The carry flag is set if the arithmetic logic unit (ALU) performs a carry or borrows during an arithmetic operation and by its special inherent instructions—set carry (SC), load carry (LDC) and invert carry (INVC). The rotate instructions—rotate right/left through carry (RRC/RLC)—operate with and through the carry bit to facilitate multiple-word shift operations. The RC, SC, INVC, LDC and STC (store carry) instructions facilitate direct bit manipulation using the carry flag.

Half Carry (H)

The half carry flag indicates whether an overflow has taken place on the boundary between the two nibbles in the accumulator. It is primarily used for Binary Coded Decimal (BCD) arithmetic calculation. The RC and SC instructions facilitate direct bit manipulation of the half carry flag.

Zero (Z)

The zero flag is set if the result of an arithmetic, logic, or data manipulation operation is zero. Otherwise, the zero flag is cleared.

Negative (N)

The result from an arithmetic, logic, or data manipulation operation is negative if the MSB is one, therefore setting the negative flag. Otherwise, the negative flag is cleared.

Global Interrupt Mask (G)

The global interrupt bit (G) is a global mask that disables all maskable interrupt sources. If G is cleared, interrupts can become pending but the operation of the core continues uninterrupted (even if the individual interrupts are enabled). However, if G is set when an interrupt becomes pending the core will be interrupted and execute the appropriate interrupt service routine.

After a reset, G is defaulted to zero and can only be set by a software instruction. When an interrupt is recognized, G is automatically cleared after the program counter value is stacked and the interrupt vector addressing the interrupt service routine is fetched. Once the interrupt is serviced, a return-from-interrupt (RETI) instruction is normally executed to restore the program counter to the value before the interrupt occurred. G is the restored to one after the return from interrupt is executed. Although G can be set within an interrupt service routine, “nesting” interrupts in this way should only be done when there is a clear understanding of latency and of the arbitration mechanism.

Table 23. Interrupt Priority Sequence

Priority (5 highest, 1 lowest)	Interrupt	
5	Software	(INTR)
4	MIW	(EDGEI)
3	Timer 0	(TMRI0)
2	PWM Timer 1	(TMRI1)
1	ADC	(ADCI)

Table 24. Instruction Addressing Modes

Instruction	Immediate			Direct		Indexed	Indirect	Inherent		Relative	Absolute
ADC	A, #			A, M		A, [#, X]	A, [X]				
ADD	A, #			A, M		A, [#, X]	A, [X]				
AND	A, #			A, M		A, [#, X]	A, [X]				
OR	A, #			A, M		A, [#, X]	A, [X]				
SUBC	A, #			A, M		A, [#, X]	A, [X]				
XOR	A, #			A, M		A, [#, X]	A, [X]				
CLR				M				A	X		
INC				M				A	X		
DEC				M				A	X		
IFEQ	A, #	X, #	M, #	A, M		A, [#, X]	A, [X]				
IFGT	A, #	X, #		A, M		A, [#, X]	A, [X]				
IFNE	A, #	X, #	M, #	A, M		A, [#, X]	A, [X]				
IFLT		X, #									
SC								no-op			
RC								no-op			
IFC								no-op			
IFNC								no-op			
INVC								no-op			
LDC				#, M							
STC				#, M							
RLC				M				A			
RRC				M				A			
LD	A, #	X, #	M, #	A, M	M, M	A, [#, X]	A, [X]				
ST				A, M		A, [#, X]	A, [X]				
NOP								no-op			
IFBIT	#, A			#, M			#, [X]				
IFNBIT	#, A			#, M			#, [X]				
SBIT				#, M			#, [X]				
RBIT				#, M			#, [X]				
JP										Rel.	
JSR						[#, X]					M
JMP						[#, X]					M
RET								no-op			
RETI								no-op			
INTR								no-op			

Table 31. Memory Mapped Registers and their Register Bit Definitions

Definitions of Register Bits									
Address	**Name**[10]	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0x9D	ADATA	8-bit digital value of ADC conversion							
0x9F	ADCNTRL1	APND	AINTEN	ASTART	REFSEL	ACHSEL [3:0]			
0xA0	ADCNTRL2	REFBY2	COMPSEL	ENAMP	ENDAS	ASPEED [1:0]		ENIS	GAIN
0xA2	DDELAY	COMPEN	PWINT	EPWM	OFFMODE	DD [3:0]			
0xA4	PSCALE	PLLEN	FS [1:0]		FSEL	FMODE	PS [2:0]		
0xA5	DTIME	X	X	X	DT [4:0]				
0xA6	T1CMPALO	Low 8 bits of 12-bit T1CMPA register							
0xA7	T1CMPAHI	X	X	X	X	High 4 bits of 12-bit T1CMPA register			
0xA8	T1CMPBLO	Low 8 bits of 12-bit T1CMPB register							
0xA9	T1CMPBHI	X	X	X	X	High 4 bits of 12-bit T1CMPB register			
0xAA	T1RALO	Low 8 bits of 12-bit T1RA register							
0xAB	T1RAHI	X	X	X	X	High 4 bits of 12-bit T1RA register			
0xAC	TMR1LO	Low 8 bits of 12-bit TMR1 register							
0xAD	TMR1HI	X	X	X	X	High 4 bits of 12-bit TMR1 register			
0xAE	T1CNTRL	T1C3	T1C2	T1C1	T1C0	T1PND	T1EN	X	T1BOUT
0xAF	WKEDG	Bit number = port number, Edge direction							
0xB0	WKPND	Bit number = port number, Pending flag for port							
0xB1	WKEN	Bit number = port number, Interrupt enable for port							
0xB2	PORTGD	Bit number = port number, Data when output, Weak pull-up when input							
0xB3	PORTGC	Bit number = port number, Input or output setting of port							
0xB4	PORTGP	Bit number = port number, Digital value at pin, Read-only							
0xB5	WDSVR	Accepts the value 0x1B as a watchdog service							
0xB6	T0CNTRL	WKINTEN	X	X	X	X	X	T0PND	T0INTEN
0xB7	HALT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EIDLE	EHALT
0xBB	InitReg1	CLK_ADJ	CMODE	unused	WDEN	BOREN	UBD	WDIS	RDIS
0xBC	InitReg2	8-bit value used internally to trim the internal oscillator frequency							
0xBD	COMP	CL [5:0]						VLOOP	COUT
0xBE	XHI	X	X	X	X	X	code/data	X [9:8]	
0xBF	XLO	Low 8 bits of 11-bit X register							
0xCE	SP	X	X	X	X	SP [3:0]			
0xCF	STATUS	EE Ready	unused	unused	Global Int.	Zero	Carry	Half Carry	Negative
0xD1	InitReg3	unused	unused	BOR_TRIM [2:0]			COMP_TRIM [2:0]		
0xD4	InitReg4	T1HS_DIR	T1HS2_LEV	T1HS1_LEV	ISOURCE_TRIM [4:0]				

1. The FMS7401L's normal mode operation begins after a system reset and is when the 8-bit microcontroller core begins executing the instruction program residing in the code EEPROM memory.
2. The FMS7401L must be placed in a special programming mode of operation in order to have full write and read access of all of the device memories. Refer to the In-circuit Programming Specification section of the datasheet for details.
3. Refer to the the 8-Bit Microcontroller Core section of the datasheet for additional details.
4. Refer to the Electrical Characteristics section of the datasheet.
5. The Initialization Register 2 shadow register will automatically be restored with its original factory setting during a system reset.
6. Once the read and/or write protection is enabled, the only possible external action of accessing the memory in programming mode is to issue a "Program Erase" command through the programming interface that clears the entire code EEPROM memory contents including the volatile Initialization Register 1. This allows full access to the user enabling new device memory programming for the single programming mode session (unless the non-volatile WDIS and RDIS bits are cleared). Refer to the In-circuit Programming Specification section of the datasheet for addition details.
7. The register can only be read.
8. The register cannot be access during normal operation only in programming mode.
9. All SR bits except for bit 7 (the global interrupt mask) are read only when using direct, indirect, or indexed instructions. Software cannot restore SR using the traditional microcontroller methods. Refer to the 8-Bit Microcontroller Core section of the datasheet for additional details.
10. A) Names in all capital letters are predefined in the assembler. B) Names of the individual bits are not predefined and must be definced using an EQU statement in the user program source code: for example, "APND EQU 7". C) The initialization registers listed are the non-volatile registers. Each register has a volatile shadow register.

12.2.4 Program Memory Erase

The external programmer may erase the entire code EEPROM memory array using two special program erase byte write commands. This special erase option may also be used to unlock memory protected (WDIS/RDIS=1) devices without compromising design security. The special program erase byte write command overrides the WDIS memory security bit if set. Once both special byte write commands are issued, the volatile Initialization Register 1 is automatically cleared to unprotect the current programming mode session and allow complete access of the device memories.[5] The external programmer may then re-program the code EEPROM with a new pattern or permanently disable all security features by re-programming the non-volatile Initialization Register 1. All other memories, including the data EEPROM, are unaffected by the program erase commands.

The special program erase protocol requires the external programmer to shift two 32-bit command words addressing two separate page addresses. The special program erase 32-bit command word is similar to a byte write command except that bit 22 must be set to 1 to enable the program erase mode. The code EEPROM memory must also be selected by setting bit 28 of the command word. The first command word must select all even pages of the memory by setting the address bits (bits 17 to 8) to 0x000. The second command word must select all odd pages by setting the address bits to 0x010 of the command word. Any data value (bits 7 to 0) shifted as part of the individual command word may be used to erase the pages of the code EEPROM. After each even/odd page program erase command is executed, the even/odd pages of the code EEPROM memory is filled with the data supplied in the command erasing their previous program code data values. If the external programmer issues only one of the (even/odd page) erase commands, only half the pages will be erased by the data selected and the volatile Initialization Register 1 will not be cleared. Therefore, the current programming mode session will remain protected if either the memory protection (WDIS/RDIS) bits are set.

After the external programmer puts the FMS7401L into programming mode, the LOAD pin must be set to Vcc before serially shifting the first 32-bit program erase command word using the SHIFT_IN and CLOCK signals. By definition, bit 31 of the command word must be shifted first and then followed by all other bits. With each bit of the 32-bit write command word shifted, the device shifts out a bit of the 32-bit response word from the previous command through the SHIFT_OUT pin. The external programmer may sample SHIFT_OUT after T_{ACCESS} from the rising edge of CLOCK. The serial response word sent immediately after entering programming mode may contain indeterminate data. After all 32 bits of the command word are shifted, the external programmer must set the LOAD signal to 0V and apply two clock pulses to the CLOCK signal, as shown in Figure 19, to complete the program cycle. Once the LOAD signal is brought low, the SHIFT_OUT pin acts as the handshaking signal between the device and external programmer hardware. When executing the write command, the device sets SHIFT_OUT low by the time the external programmer has issued the second rising edge of CLOCK informing the external programmer that the memory write is in progress. The external programmer must wait T_{READY} for SHIFT_OUT to return high before returning the LOAD signal to Vcc to initiate the second program erase command cycle. The volatile Initialization Register 1 will only be cleared if both commands are successfully executed. All other memory accesses from this point forward are executed normally.

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1. During in-circuit programming, G5 must be either not connected or driven high.
2. The following characteristics are guaranteed by design but are not 100% tested.
3. For addition detail regarding the device power-up and reset conditions refer the Reset Circuit section of the datasheet.
4. Each page in the code EEPROM has 16 bytes and starts at address 0xC00, 0xC10, 0xC20, etc.
5. For additional details regarding the WDIS, RDIS, and initialization registers, refer to the Device Memory section of the datasheet.

AC Electrical Characteristics

All measurements are valid for T_A=+25°C unless otherwise stated.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OSC}[5]	Internal oscillator frequency (factory trim set-point)	Vcc=3.3V	1.96	2.00	2.04	MHz
Δckv	Internal oscillator frequency voltage variation		-0.5		+0.5	%
Δckt	Internal oscillator frequency temperature variation	Vcc=3.3V -40°C to 85°C	-3		+3	%
		Vcc=3.3V -40°C to 125°C	-4		+4	%
F_{PLL}	PLL input reference frequency			2.00		MHz
T_{PLL_LOCK}[3]	PLL Lock time	-40°C to 125°C			60	µS
T_{EEW}	EEPROM Writing time			3.7	5	mS
T_{RESET}[3]	System reset time	-40°C to 125°C	2.5	3.7	4.7	mS
T_{DIO}[3]	T1HS1 and T1HS2 default I/O configuration settling time			40		µS
T_{HALT_REC}[3]	Internal device start time after exiting from Halt where $F_{ICLK} = F_{OSC}$[2]	-40°C to 125°C		5	7	µS

Brown-out Reset (BOR) Electrical Characteristics

All measurements are valid for T_A=+25°C unless otherwise stated.

Parameter	Conditions	Min.	Typ.	Max.	Units
BOR Trigger Vcc Threshold Level		2.64	2.71	2.78	V
	-40°C to +85°C	2.60		2.83	V
	-40°C to 125°C	2.59		2.83	V

Programmable Comparator Electrical Characteristics

All measurements are valid for T_A=+25°C unless otherwise stated.

Parameter	Conditions	Min.	Typ.	Max.	Units
All 32 thresholds (V_{THU})		-6%	V_{THU}	+6%	V
Upper Range (0.45V to 2.0V)	-40°C to 125°C	-8%	V_{THU}	+8%	V
All 31 thresholds (V_{THL})		V_{THU} – 30mV	V_{THL}	V_{THU} + 30mV	V
Lower Range (0.03V to 0.43V)	-40°C to 125°C	V_{THU} – 35mV	V_{THL}	V_{THU} + 35mV	V
Comparator Response Time[3]	2mV overdrive		359		nS
	5mV overdrive		173		nS
	10mV overdrive		95		nS

ADC Electrical Characteristics

All measurements are valid for T_A=+25°C unless otherwise stated.

Parameter	Conditions	Min.	Typ.	Max.	Units
ADC Integral Non Linearity (INL) Best Fit[3]	V_{AREF}=Vcc ASPEED=0 where (F_{ICLK}=F_{OSC})/1[2]			1.5	LSB
	V_{AREF}=Internal Reference (V_{REF}) ASPEED=0 where (F_{ICLK}=F_{OSC})/1[2]			1.5	LSB
	V_{AREF}=Internal Reference (V_{REF}) ASPEED=2 where (F_{ICLK}=F_{OSC})/4[2] -40°C to +125°C			0.5	LSB
ADC Differential Non Linearity (DNL)[3]	Vref=Vcc ASPEED=0 where (F_{ICLK}=F_{OSC})/1[2]			2.5	LSB
	V_{AREF}=Internal Reference (V_{REF}) ASPEED=0 where (F_{ICLK}=F_{OSC})/1[2]			1.5	LSB
	V_{AREF}=Internal Reference (V_{REF}) ASPEED=2 where (F_{ICLK}=F_{OSC})/4[2] -40°C to +125°C			1	LSB
ADC Conversion Time[3]	ASPEED=0 where (F_{ICLK}=F_{OSC})/1[2] -40°C to +125°C			20	µS
Internal Voltage Reference (V_{REF})[3]			1.215		V
Amplifier x16 Gain Error[3]	-40°C to +125°C	2		2	%
Current Source (I_{SRC}) on G3/AIN1		0.9	1	1.1	mA
Current Source (I_{SRC}) on G3/AIN1	-40°C to +125°C	0.89	1	1.11	mA

Independent Amplifier Electrical Characteristics[3]

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Bias Current	-40°C to +125°C	-1		+1	µA
Input Offset Voltage	-40°C to +125°C		4		mV
Open Loop Voltage Gain	-40°C to +125°C		97		dB
Gain Bandwidth Product	-40°C to +125°C		3.7		MHz
Sink/Source Current	-40°C to +125°C	0.5		4.5	mA

Figure 28. Idle Current vs. Temperature (with PLL)

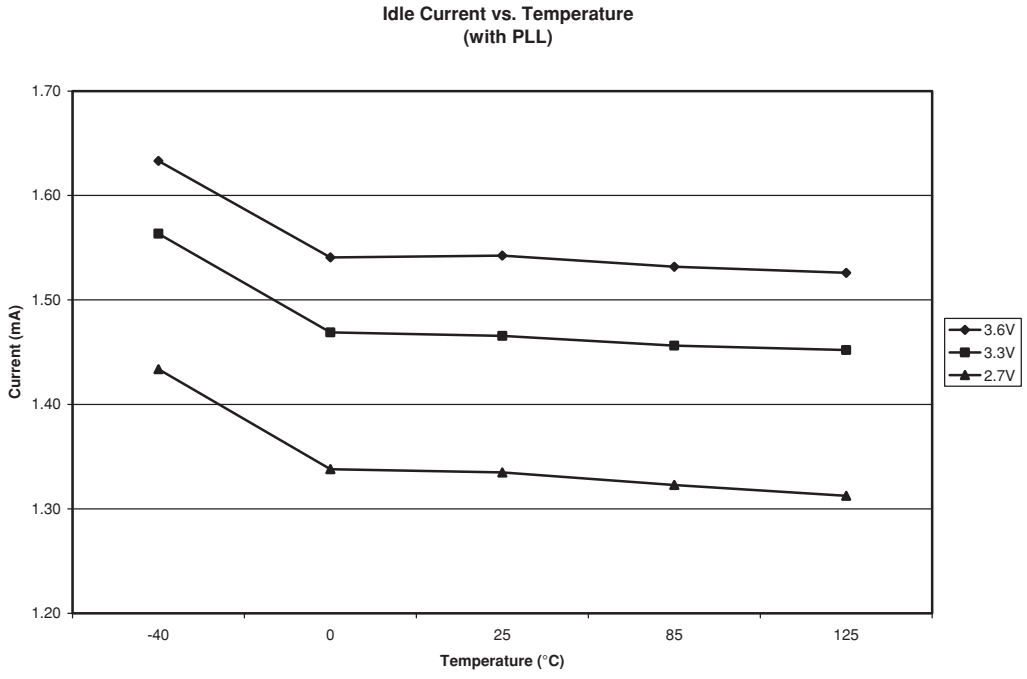

Figure 29. V_{OL} vs. I_{OL} @ 25°C (G1–G4, G6, G7)

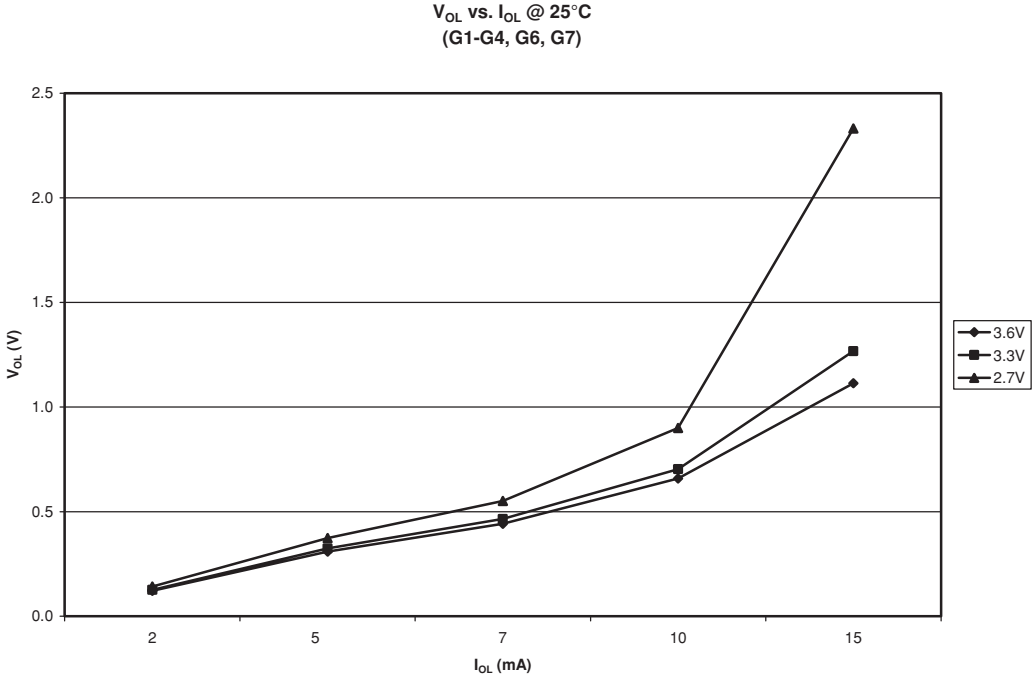

Figure 32. V_{OH} vs. I_{OH} @ 25°C (G0, G5)

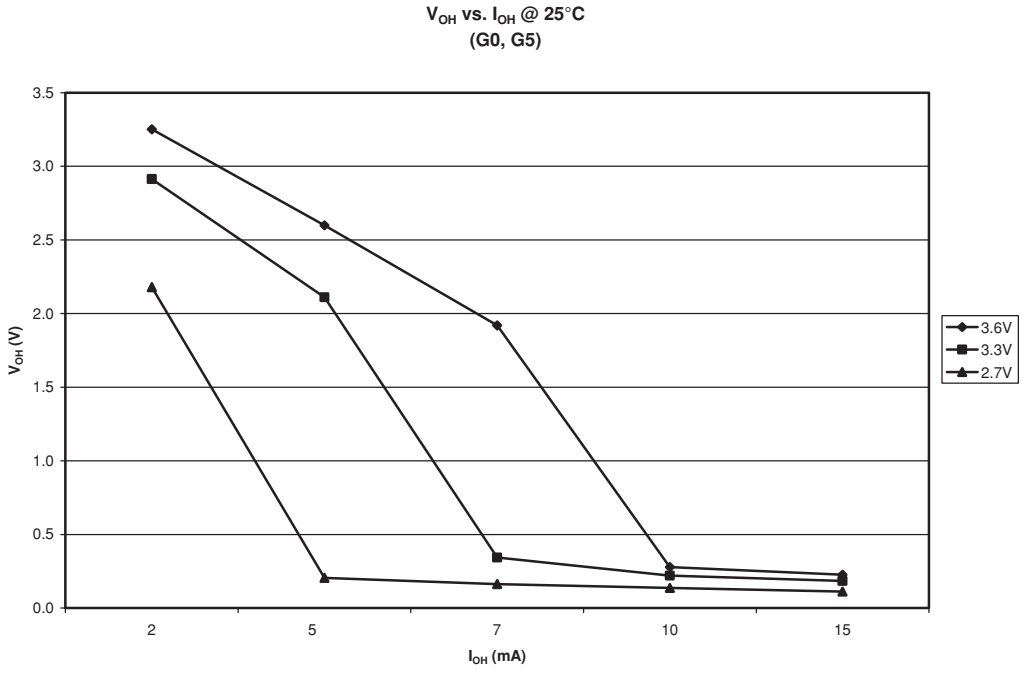

Figure 33. BOR Level vs. Temperature

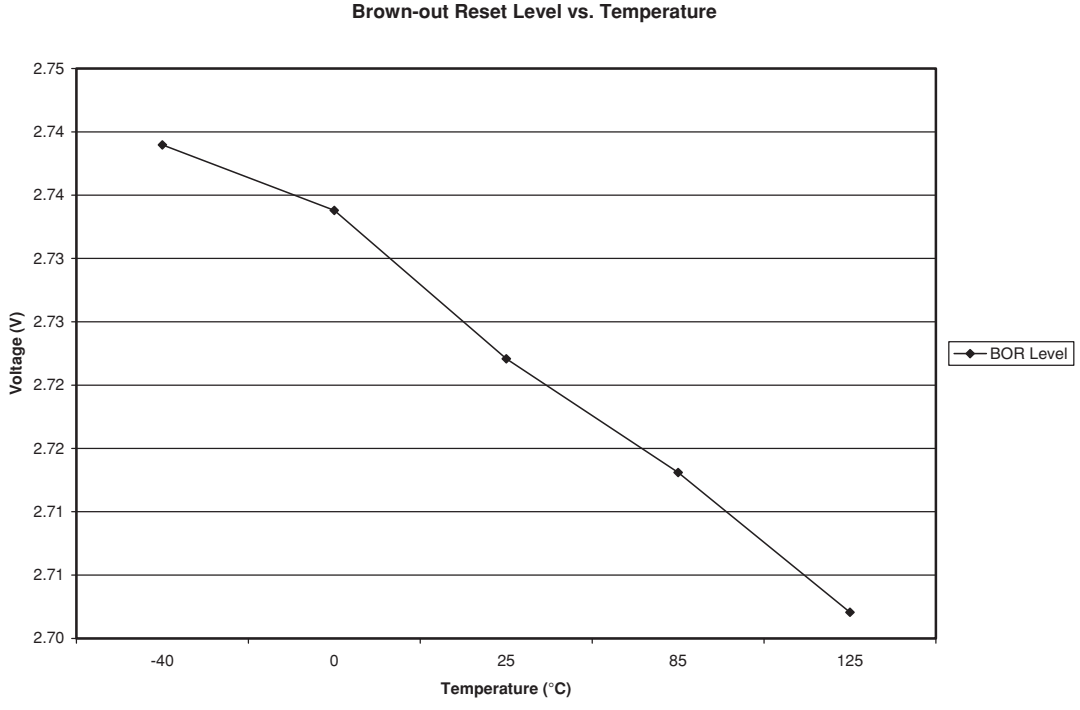

Figure 34. Programmable Comparator Voltage Level vs. Temperature

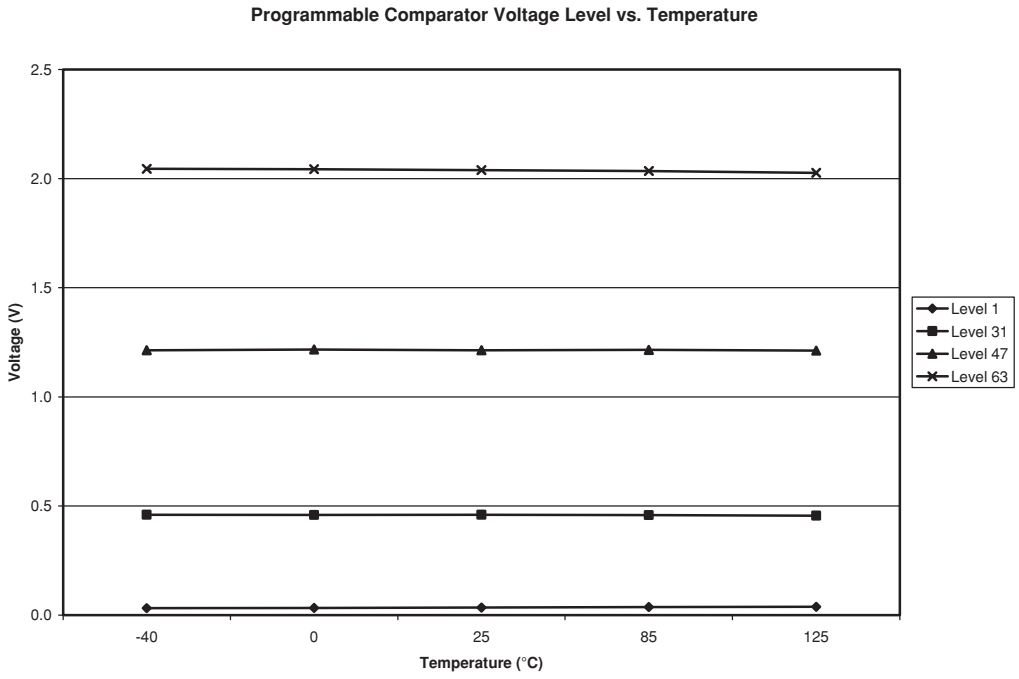

Figure 35. V_{REF} vs. Temperature