Renesas Electronics America Inc - UPD78F1177AGF-GAT-AX Datasheet

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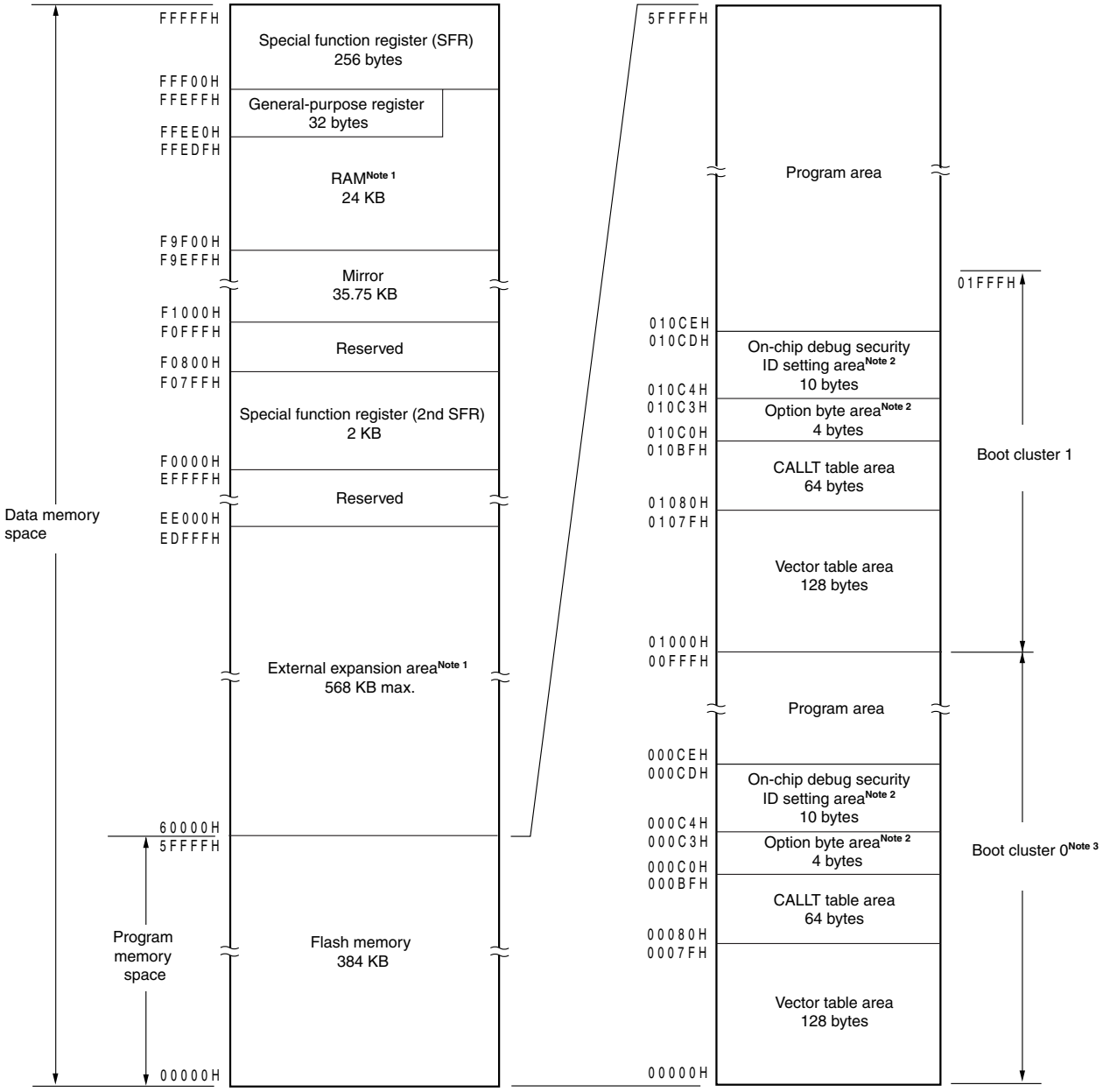
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1177agf-gat-ax

Figure 3-4. Memory Map (μPD78F1177, 78F1177A)



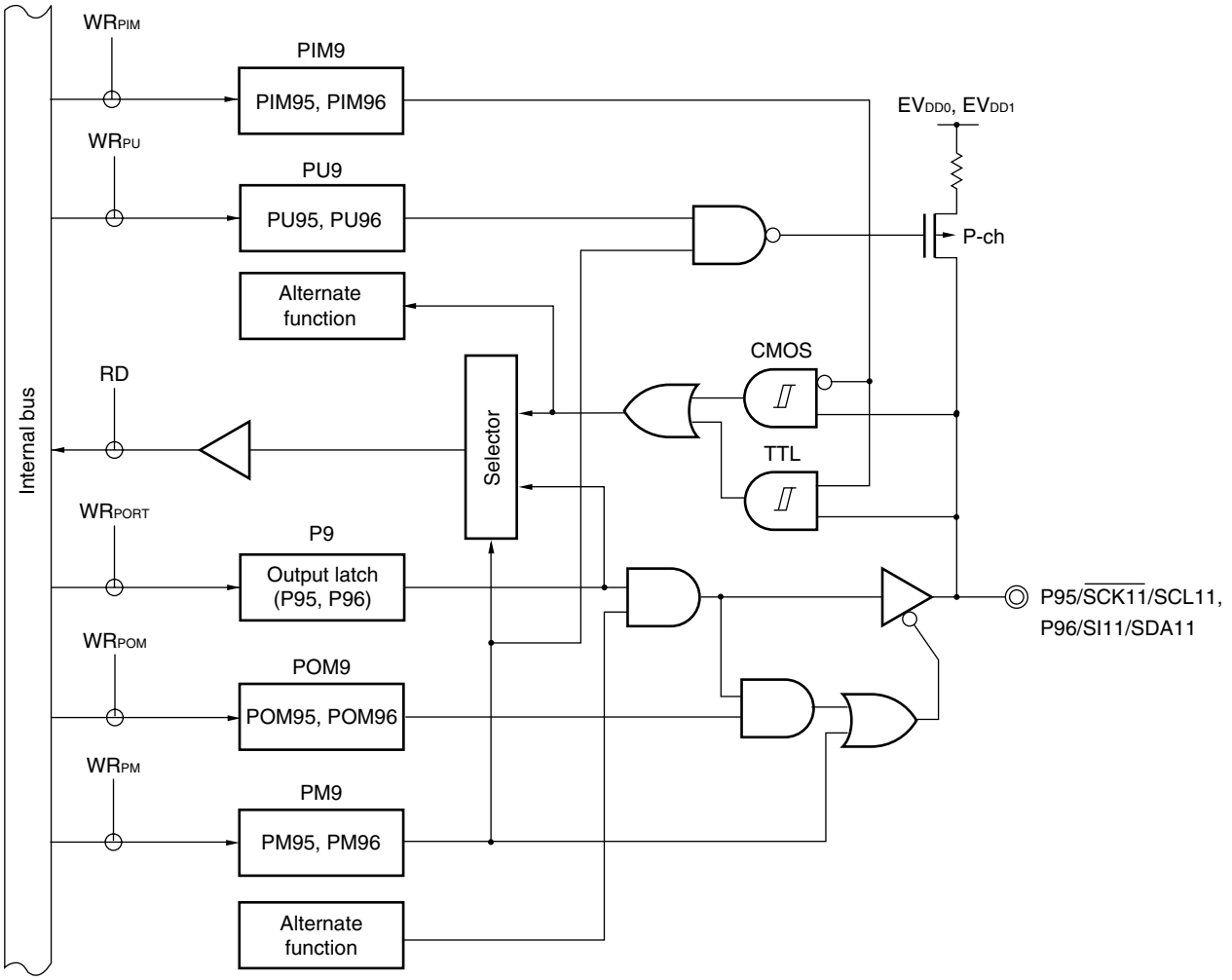
Notes 1. Instructions can be executed from the RAM area excluding the general-purpose register area, and from the external expansion area.

2. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

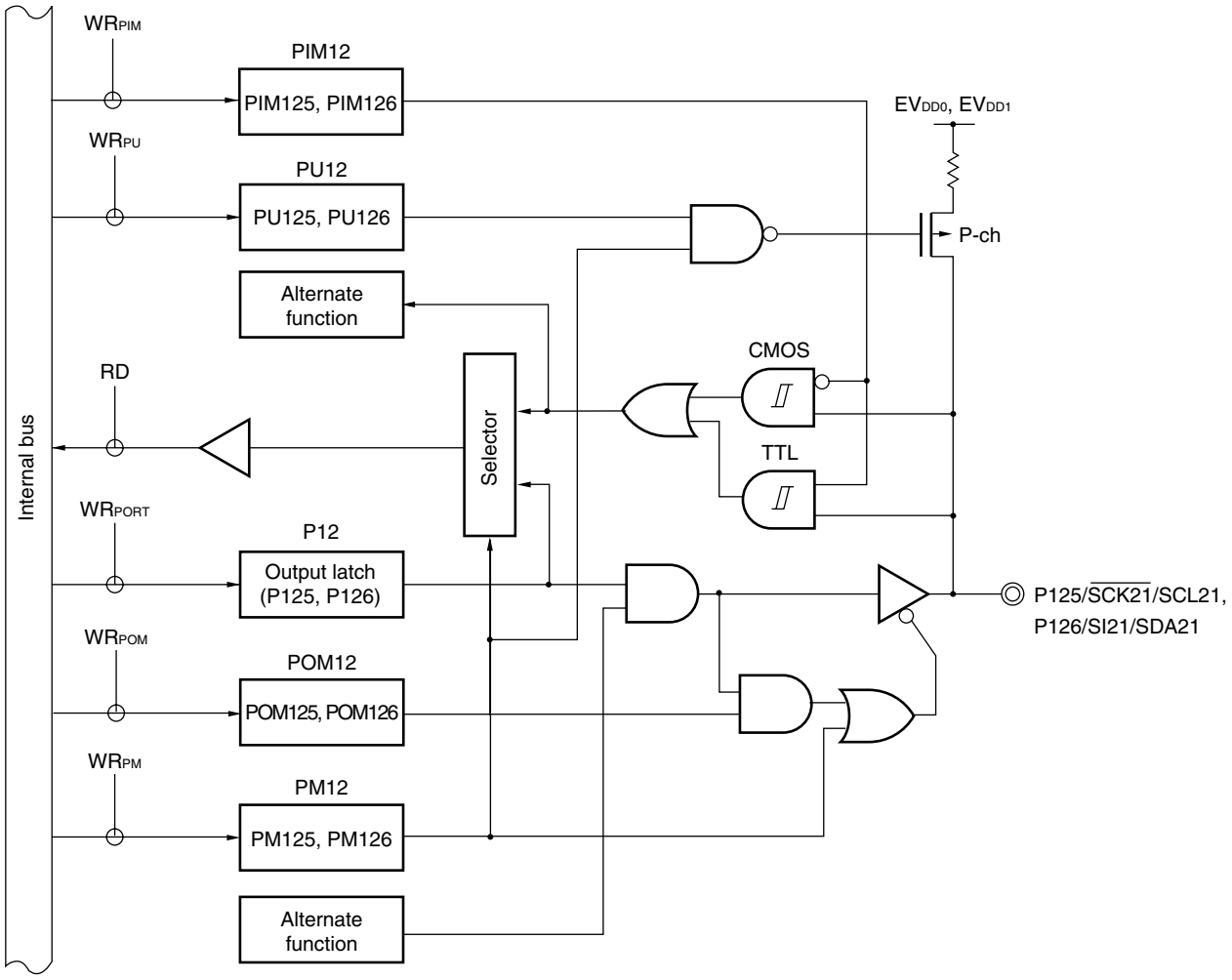
3. Writing boot cluster 0 can be prohibited depending on the setting of security (see **25.7 Security Setting**).

Figure 4-34. Block Diagram of P95 and P96



P9: Port register 9
PU9: Pull-up resistor option register 9
PM9: Port mode register 9
PIM9: Port input mode register 9
POM9: Port output mode register 9
RD: Read signal
WR××: Write signal

Figure 4-41. Block Diagram of P125 and P126



P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
PIM12: Port input mode register 12
POM12: Port output mode register 12
RD: Read signal
WR××: Write signal

(7) Operation speed mode control register (OSMC)

This register is used to control the step-up circuit of the flash memory for high-speed operation.

If the microcontroller operates at a low speed with a system clock of 10 MHz or less, the power consumption can be lowered by setting this register to the default value, 00H.

OSMC can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6-8. Format of Operation Speed Mode Control Register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	0	0	0	0	0	0	0	FSEL

FSEL	f_{CLK} frequency selection
0	Operates at a frequency of 10 MHz or less (default).
1	Operates at a frequency higher than 10 MHz.

Cautions 1. OSMC can be written only once after reset release, by an 8-bit memory manipulation instruction.

2. Write "1" to FSEL before the following two operations.

- **Changing the clock prior to dividing f_{CLK} to a clock other than f_{IH}.**
- **Operating the DMA controller.**

3. The CPU waits when "1" is written to the FSEL flag.
Interrupt requests issued during a wait will be suspended.
The wait time is 16.6 μs to 18.5 μs when $f_{CLK} = f_{IH}$, and 33.3 μs to 36.9 μs when $f_{CLK} = f_{IH}/2$.
However, counting the oscillation stabilization time of f_X can continue even while the CPU is waiting.

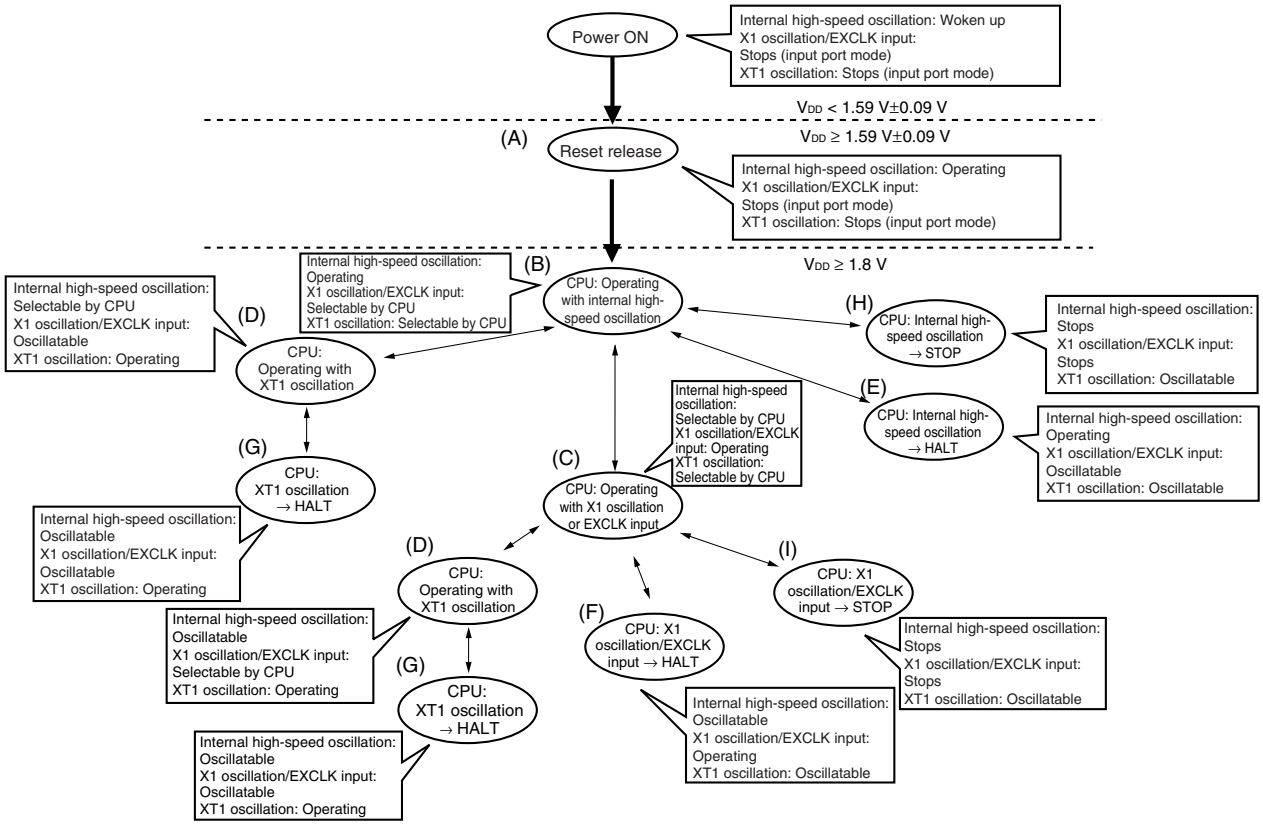
<R> **4. To increase f_{CLK} to 10 MHz or higher, set FSEL to "1", then change f_{CLK} after two or more clocks have elapsed. Use the external bus interface two clock cycles after setting FSEL to 1.**

<R> **5. Flash memory can be used at a frequency of 10 MHz or lower if FSEL is 1.**

6.6.5 CPU clock status transition diagram

Figure 6-15 shows the CPU clock status transition diagram of this product.

Figure 6-15. CPU Clock Status Transition Diagram



Remark If the low-power-supply detector (LVI) is set to ON by default by the option bytes, the reset will not be released until the power supply voltage (V_{DD}) exceeds 2.07 V±0.2 V.

After the reset operation, the status will shift to (B) in the above figure.

Figure 7-24. Format of Noise Filter Enable Register 2 (NFEN2)

Address: F0062H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN2	0	0	0	0	TNFEN13	TNFEN12	TNFEN11	TNFEN10

TNFEN13	Enable/disable using noise filter of TI13/TO13/P163 pin input signal
0	Noise filter OFF
1	Noise filter ON

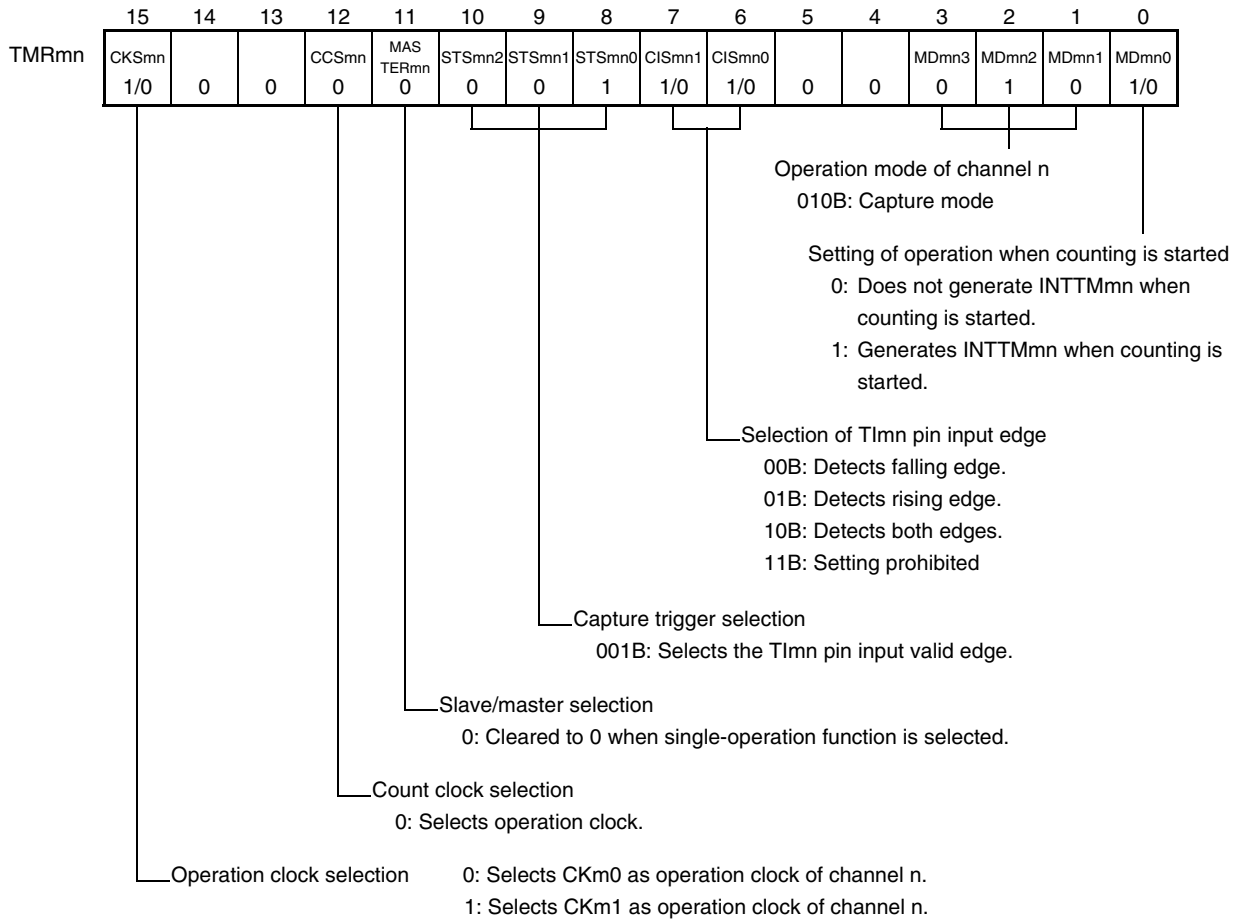
TNFEN12	Enable/disable using noise filter of TI12/TO12/P162 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN11	Enable/disable using noise filter of TI11/TO11/P161 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN10	Enable/disable using noise filter of TI10/TO10/P160 pin input signal
0	Noise filter OFF
1	Noise filter ON

Figure 7-51. Example of Set Contents of Registers to Measure Input Pulse Interval

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn	0: Outputs 0 from TOmn.
	0	

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn	0: Stops TOmn output operation by counting operation.
	0	

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn	0: Cleared to 0 when TOMmn = 0 (toggle mode).
	0	

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn	0: Sets toggle mode.
	0	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7),
mn = 00 to 07, 10 to 13

Figure 7-56. Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit, TAU1EN bit of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPSm register. Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets the TMRmn register (determines operation mode of channel). Clears TOEmn to 0 and stops operation of TOmn.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and the TImn pin start edge detection wait status is set.
	Detects TImn pin input count start valid edge. →	Clears TCRmn to 0000H and starts counting up.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	When the TImn pin start edge is detected, the counter (TCRmn) counts up from 0000H. If a capture edge of the TImn pin is detected, the count value is transferred to TDRmn and INTTMmn is generated. If an overflow occurs at this time, the OVF bit of the TSRmn register is set; if an overflow does not occur, the OVF bit is cleared. TCRmn stops the count operation until the next TImn pin start edge is detected.
Operation stop	The TTmn bit is set to 1. → TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. TCRmn holds count value and stops. The OVF bit of the TSRmn register is also held.
TAU stop	The TAU0EN bit, TAU1EN bit of PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7),
mn = 00 to 07, 10 to 13

Figure 7-66. Operation Procedure of One-Shot Pulse Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit, TAU0EN bit of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPSm register. Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets the TMRmn and TMRmp registers of two channels to be used (determines operation mode of channels). An output delay is set to the TDRmn register of the master channel, and a pulse width is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of the TOMm register is set to 1 (combination-operation mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmp pin goes into Hi-Z output state. The TOmp default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets TOEmp to 1 and enables operation of TOmp. →	TOmp does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmp pin outputs the TOmp set level.

Remark m: Unit number, n: Channel number, p: Slave channel number (p = n+1),
When m = 0: n = 0, 2, 4, 6
When m = 1: n = 0, 2

(10) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Set a decimal value of 00 to 06 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.

WEEK can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 8-11. Format of Week Count Register (WEEK)

Address: FFF95H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
WEEK	0	0	0	0	0	WEEK4	WEEK2	WEEK1

Caution The value corresponding to the month count register or the day count register is not stored in the week count register automatically. After reset release, set the week count register as follow.

Day	WEEK
Sunday	00H
Monday	01H
Tuesday	02H
Wednesday	03H
Thursday	04H
Friday	05H
Saturday	06H

(3) 10-bit A/D conversion result register (ADCR)

This register is a 16-bit register that stores the A/D conversion result. The lower 6 bits are fixed to 0. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register. The higher 8 bits of the conversion result are stored in FFF1FH and the lower 2 bits are stored in the higher 2 bits of FFF1EH.

ADCR can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 11-7. Format of 10-Bit A/D Conversion Result Register (ADCR)

Address: FFF1FH, FFF1EH After reset: 0000H R

Symbol	FFF1FH								FFF1EH							
ADCR											0	0	0	0	0	0

Caution When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using timing other than the above may cause an incorrect conversion result to be read.

(4) 8-bit A/D conversion result register (ADCRH)

This register is an 8-bit register that stores the A/D conversion result. The higher 8 bits of 10-bit resolution are stored.

ADCRH can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-8. Format of 8-Bit A/D Conversion Result Register (ADCRH)

Address: FFF1FH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ADCRH								

Caution When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using timing other than the above may cause an incorrect conversion result to be read.

The D/A converter includes the following hardware.

Table 12-1. Configuration of D/A Converter

Item	Configuration
Control registers	Peripheral enable register 0 (PER0) D/A converter mode register (DAM) 8-bit D/A conversion value setting registers 0, 1 (DACS0, DACS1)

(1) AV_{REF1} pin

This is the D/A converter reference voltage input pin and the positive power supply pin of P110, P111, and the D/A converter.

The voltage that can be supplied to AV_{REF1} varies as follows, depending on whether the P110/ANO0 and P111/ANO1 pins are used as digital I/Os or analog outputs.

Table 12-2. AV_{REF1} Voltage Applied to P110/ANO0 and P111/ANO1 Pins

Analog/Digital	V_{DD} Condition	AV_{REF1} Voltage
Using at least one pin as an analog output and using all pins not as digital I/Os	1.8 V ≤ V_{DD} ≤ 5.5 V	1.8 V ≤ AV_{REF1} ≤ V_{DD} = EV_{DD0} = EV_{DD1}
Pins used as analog outputs and digital I/Os are mixed[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REF1} ≤ V_{DD} = EV_{DD0} = EV_{DD1}
	1.8 V ≤ V_{DD} < 2.7 V	AV_{REF1} has same potential as EV_{DD0}, EV_{DD1}, and V_{DD}
Using at least one pin as a digital I/O and using all pins not as analog outputs[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REF1} ≤ V_{DD} = EV_{DD0} = EV_{DD1}
	1.8 V ≤ V_{DD} < 2.7 V	AV_{REF1} has same potential as EV_{DD0}, EV_{DD1}, and V_{DD}

Note AV_{REF1} is the reference for the I/O voltage of a port to be used as a digital port.

- High-/low-level input voltage (V_{IH5}/V_{IL5})
- High-/low-level output voltage (V_{OH2}/V_{OL2})

12.4.3 Cautions

Observe the following cautions when using the D/A converter of the 78K0R/KH3.

(1) The digital port I/O function, which is the alternate function of the ANO0 and ANO1 pins, does not operate during D/A conversion.

<R> During D/A conversion, 0 is read from the P11 register in input mode.

(2) Do not read/write the P11 register and do not change the setting of the PM11 register during D/A conversion (otherwise the conversion accuracy may decrease).

(3) It is recommended that both the ANO0 and ANO1 pins be used as analog output pins or digital I/O pins, that is, use these two channels for the same application (if these pins are used for the different applications, the conversion accuracy may decrease).

(4) In the real-time output mode, set the DACSn register value before the timer trigger is generated. In addition, do not change the set value of the DACSn register while the trigger signal is output.

(5) Before changing the operation mode, be sure to clear the DACEn bit of the DAM register to 0 (D/A conversion stop).

(6) When using the port that functions alternately as the ANO0 or ANO1 pin, use it as the port input with few level changes.

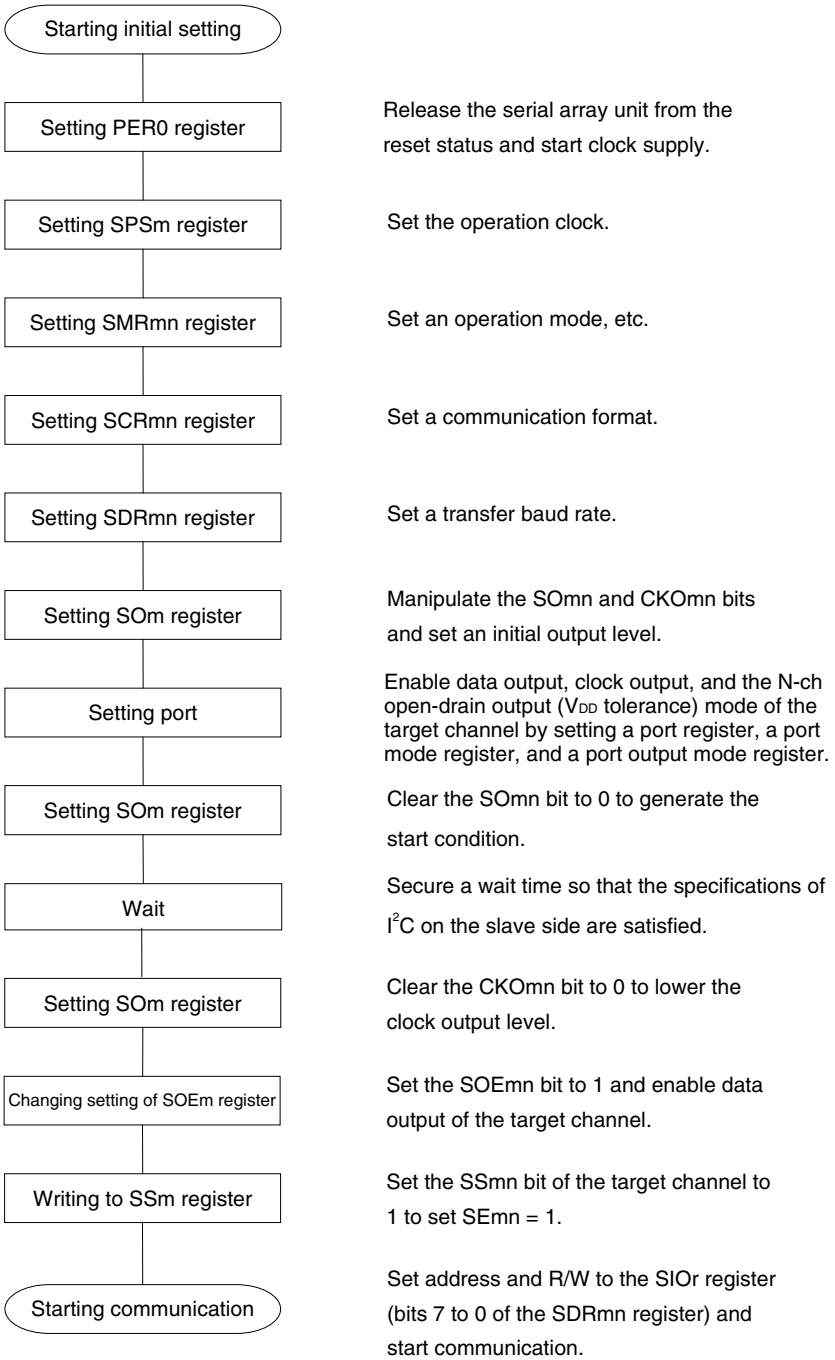
<R> (7) Stop the conversion performed by the D/A converter when supplying AV_{REF1} or AV_{REF0} (the reference voltages for the A/D converter) starts or stops.

(8) Because the D/A converter stops operation in the STOP mode, the ANO0 and ANO1 pins go into a high-impedance state, and the power consumption can be reduced.
In the standby modes other than the STOP mode, however, the operation continues. To lower the power consumption, therefore, clear the DACEn bit of the DAM register to 0 (D/A conversion stop).

(9) Since the output impedance of the D/A converter is high, the current cannot be obtained from the ANOn pin (n = 0, 1). When the input impedance of the load is low, insert a follower amplifier between the load and ANOn pin keeping the wiring length as short as possible (for high impedance). If the wiring becomes too long, take necessary actions such as surrounding with a ground pattern.

(2) Operation procedure

Figure 13-94. Initial Setting Procedure for Address Field Transmission



Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

13.7.6 Procedure for processing errors that occurred during simplified I²C (IIC10, IIC11, IIC20, IIC21) communication

The procedure for processing errors that occurred during simplified I²C (IIC10, IIC11, IIC20, IIC21) communication is described in Figures 13-105 and 13-106.

<R> **Figure 13-105. Processing Procedure in Case of Parity Error or Overrun Error**

Software Manipulation	Hardware Status	Remark
Reads SDRmn register. →	BFF = 0, and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads SSRmn register.		Error type is identified and the read value is used to clear error flag.
Writes SIRmn register. →	Error flag is cleared.	Only error generated at the point of reading can be cleared, by writing the value read from the SSRmn register to the SIRmn register without modification.

Figure 13-106. Processing Procedure in Case of Parity Error (ACK error) in Simplified I²C Mode

Software Manipulation	Hardware Status	Remark
Reads SDRmn register. →	BFF = 0, and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads SSRmn register.		Error type is identified and the read value is used to clear error flag.
Writes SIRmn register. →	Error flag is cleared.	Only error generated at the point of reading can be cleared, by writing the value read from the SSRmn register to the SIRmn register without modification.
Sets STmn bit to 1. →	SEmn = 0, and channel n stops operation.	Slave is not ready for reception because ACK is not returned. Therefore, a stop condition is created, the bus is released, and communication is started again from the start condition. Or, a restart condition is generated and transmission can be redone from address transmission.
Creates stop condition.		
Creates start condition.		
Sets SSmn bit to 1. →	SEmn = 1, and channel n is enabled to operate.	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 02, 03, 10, 11

Operation example 2: When used as interrupt

Interrupt requests may be generated frequently.

Take the following action.

<Action>

Confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, in the servicing routine of the LVI interrupt by using bit 0 (LVIF) of the low-voltage detection register (LVIM). Clear bit 1 (LVIIF) of interrupt request flag register 0L (IF0L) to 0.

For a system with a long supply voltage fluctuation period near the LVI detection voltage, take the above action after waiting for the supply voltage fluctuation time.

Remark If bit 2 (LVISEL) of the low voltage detection register (LVIM) is set to "1", the meanings of the above words change as follows.

- Supply voltage (V_{DD}) → Input voltage from external input pin (EXLVI)
- Detection voltage (V_{LVI}) → Detection voltage (V_{EXLVI} = 1.21 V)

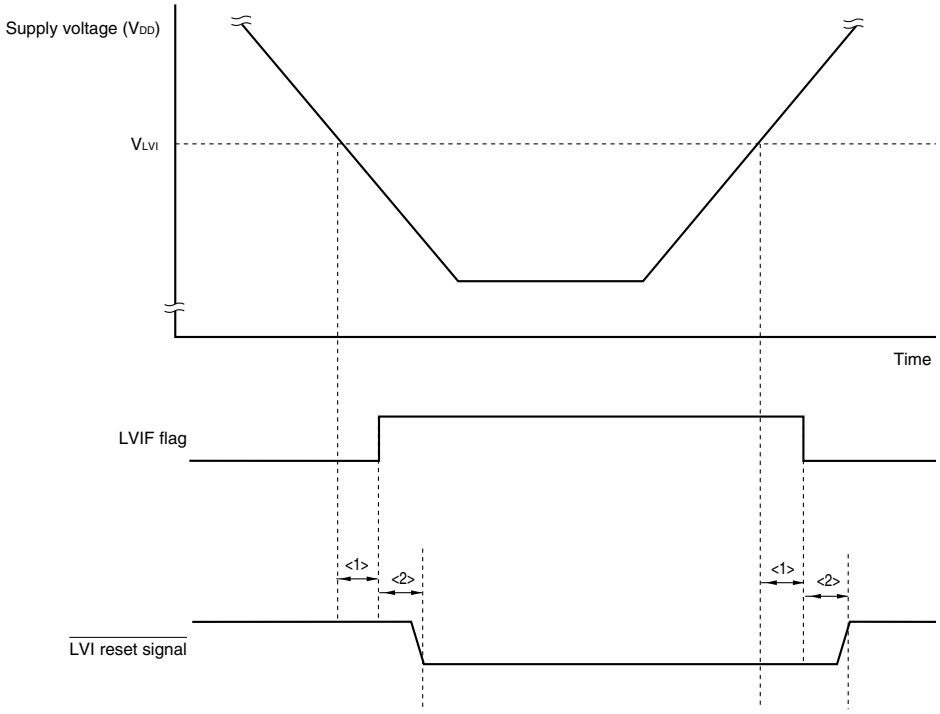
(2) Delay from the time LVI reset source is generated until the time LVI reset has been generated or released

There is some delay from the time supply voltage (V_{DD}) < LVI detection voltage (V_{LVI}) until the time LVI reset has been generated.

In the same way, there is also some delay from the time LVI detection voltage (V_{LVI}) ≤ supply voltage (V_{DD}) until the time LVI reset has been released (see **Figure 22-12**).

See the timing in **Figure 21-2 (2) When LVI is ON upon power application (option byte: LVIOFF = 0)** for the reset processing time until the normal operation is entered after the LVI reset is released.

Figure 22-12. Delay from the time LVI reset source is generated until the time LVI reset has been generated or released



<1> : Minimum pulse width (200 μs (MIN.))

<2> : Detection delay time (200 μs (MAX.))

25.8 Processing Time of Each Command When Using PG-FP4 or PG-FP5 (Reference Values)

The processing time of each command (reference values) when using PG-FP4 or PG-FP5 as the dedicated flash memory programmer is shown below.

Table 25-9. Processing Time of Each Command When Using PG-FP4 (Reference Values)

PG-FP4 Command	Port: UART									
	Speed: 115200 bps					Speed: 1 Mbps				
	μPD78F1174, μPD78F1174A	μPD78F1175, μPD78F1175A	μPD78F1176, μPD78F1176A	μPD78F1177, μPD78F1177A	μPD78F1178, μPD78F1178A	μPD78F1174, μPD78F1174A	μPD78F1175, μPD78F1175A	μPD78F1176, μPD78F1176A	μPD78F1177, μPD78F1177A	μPD78F1178, μPD78F1178A
Signature	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	1 s (TYP.)	1 s (TYP.)
Blankcheck	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)
Erase	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)
Program	19 s (TYP.)	26.5 s (TYP.)	35 s (TYP.)	51.5 s (TYP.)	68.5 s (TYP.)	6.5 s (TYP.)	9 s (TYP.)	12 s (TYP.)	17.5 s (TYP.)	23 s (TYP.)
Verify	16 s (TYP.)	23.5 s (TYP.)	31 s (TYP.)	46 s (TYP.)	61 s (TYP.)	4.5 s (TYP.)	6 s (TYP.)	8 s (TYP.)	11.5 s (TYP.)	15.5 s (TYP.)
E.P.V	20 s (TYP.)	28 s (TYP.)	36.5 s (TYP.)	53.5 s (TYP.)	71 s (TYP.)	7.5 s (TYP.)	10.5 s (TYP.)	13.5 s (TYP.)	19.5 s (TYP.)	25.5 s (TYP.)
Checksum	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)
Security	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	1 s (TYP.)	1 s (TYP.)

Table 25-10. Processing Time of Each Command When Using PG-FP5 (Reference Values)

PG-FP5 Command	Port: UART									
	Speed: 115200 bps					Speed: 1 Mbps				
	μPD78F1174, μPD78F1174A	μPD78F1175, μPD78F1175A	μPD78F1176, μPD78F1176A	μPD78F1177, μPD78F1177A	μPD78F1178, μPD78F1178A	μPD78F1174, μPD78F1174A	μPD78F1175, μPD78F1175A	μPD78F1176, μPD78F1176A	μPD78F1177, μPD78F1177A	μPD78F1178, μPD78F1178A
Signature read	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)
Blank check	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)
Erase	1 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)
Program	17.5 s (TYP.)	26 s (TYP.)	34 s (TYP.)	51 s (TYP.)	67.5 s (TYP.)	6 s (TYP.)	8.5 s (TYP.)	11 s (TYP.)	16.5 s (TYP.)	22 s (TYP.)
Verify	15.5 s (TYP.)	23 s (TYP.)	30.5 s (TYP.)	45.5 s (TYP.)	60 s (TYP.)	4 s (TYP.)	5.5 s (TYP.)	7.5 s (TYP.)	11 s (TYP.)	14 s (TYP.)
Auto-procedure	18 s (TYP.)	26.5 s (TYP.)	35 s (TYP.)	52 s (TYP.)	69 s (TYP.)	6 s (TYP.)	9 s (TYP.)	12 s (TYP.)	18 s (TYP.)	23.5 s (TYP.)
Checksum	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)
Security	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)	0.5 s (TYP.)

Table 26-1. Differences Between 1-Line Mode and 2-Line Mode

Communication Mode	Flash Memory Programming Function	Debugging Function
1-line mode	Available	• Pseudo real-time RAM monitor (RRM) function not supported
2-line mode	None	• Pseudo real-time RAM monitor (RRM) function supported

Remark 2-line mode is not used for flash programming, however, even if TOOL1 pin is connected with CLK_IN of QB-MINI2, writing is performed normally with no problem.

26.2 On-Chip Debug Security ID

The 78K0R/KH3 has an on-chip debug operation control bit in the flash memory at 000C3H (see **CHAPTER 24 OPTION BYTE**) and an on-chip debug security ID setting area at 000C4H to 000CDH, to prevent third parties from reading memory content.

When the boot swap function is used, also set a value that is the same as that of 010C3H and 010C4H to 010CDH in advance, because 000C3H, 000C4H to 000CDH and 010C3H, and 010C4H to 010CDH are switched.

For details on the on-chip debug security ID, refer to the **QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual (U18371E)**.

Table 26-2. On-Chip Debug Security ID

Address	On-Chip Debug Security ID
000C4H to 000CDH	Any ID code of 10 bytes
010C4H to 010CDH	

26.3 Securing of user resources

To perform communication between the 78K0R/KH3 and QB-MINI2, as well as each debug function, the securing of memory space must be done beforehand.

If NEC Electronics assembler RA78K0R or compiler CC78K0R is used, the items can be set by using linker options.

(1) Securement of memory space

The shaded portions in Figure 26-2 are the areas reserved for placing the debug monitor program, so user programs or data cannot be allocated in these spaces. When using the on-chip debug function, these spaces must be secured so as not to be used by the user program. Moreover, this area must not be rewritten by the user program.

Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

(a) Conventional-specification products (μPD78F117x)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
V_{DD} supply current	I_{DD}	TYP. = 10 MHz, MAX. = 20 MHz			4.5	15	mA
CPU/peripheral hardware clock frequency	f_{CLK}			2		20	MHz
Number of rewrites (number of deletes per block)	C_{WRT}	Used for updating programs When using flash memory programmer and NEC Electronics self programming library	Retained for 15 years	100			Times
		Used for updating data When using NEC Electronics EEPROM emulation library (usable ROM size: 6 KB of 3 consecutive blocks)	Retained for 3 years	10,000			Times

Remark When updating data multiple times, use the flash memory as one for updating data.

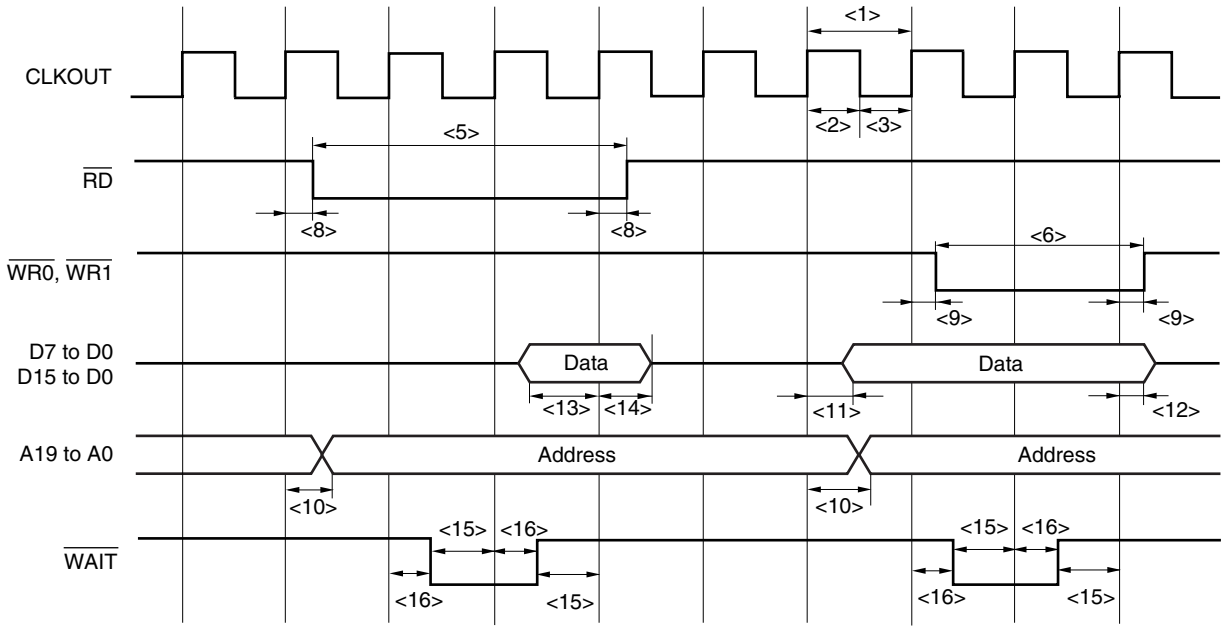
(b) Expanded-specification products (μPD78F117xA)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
V_{DD} supply current	I_{DD}	TYP. = 10 MHz, MAX. = 20 MHz			4.5	15	mA
CPU/peripheral hardware clock frequency	f_{CLK}			2		20	MHz
<R> Number of rewrites (number of deletes per block)	C_{WRT}	Used for updating programs When using flash memory programmer and NEC Electronics self programming library	Retained for 15 years	1000			Times
		Used for updating data When using NEC Electronics EEPROM emulation library (usable ROM size: 6 KB of 3 consecutive blocks)	Retained for 5 years	10,000			Times

Remark When updating data multiple times, use the flash memory as one for updating data.

(2) External bus interface (2/4)

Read/write cycle (CLKOUT synchronous): In separate bus mode



Read/write cycle (CLKOUT synchronous): In multiplexed bus mode