Renesas Electronics America Inc - UPD78F1178AGF-GAT-AX Datasheet

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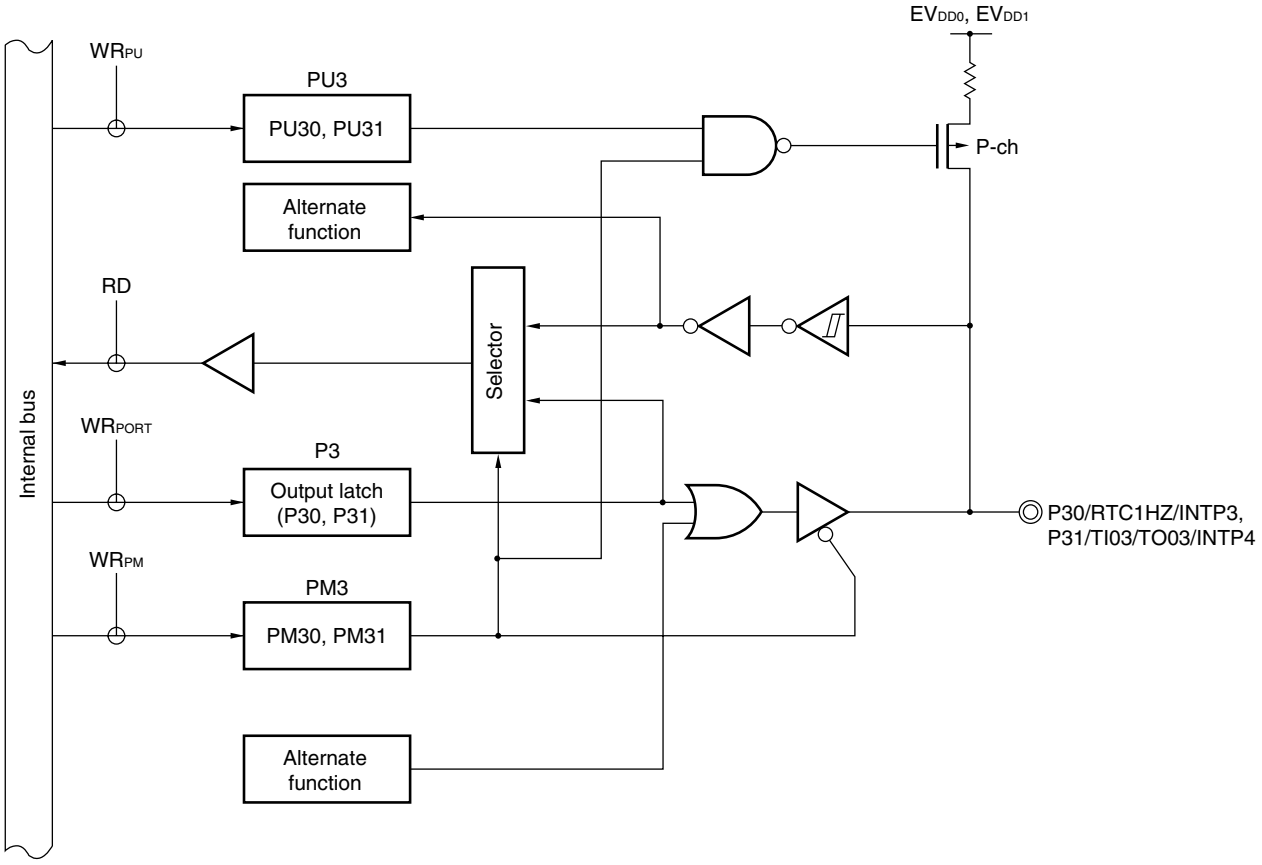
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	30K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1178agf-gat-ax

Figure 4-15. Block Diagram of P30 and P31



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

4.2.12 Port 12

P120 and P125 to P127 are a 4-bit I/O port with an output latch. P120 and P125 to P127 can be set to the input mode or output mode in 1-bit units using port mode register 12 (PM12). When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 are 4-bit input ports.

Input to the P125 and P126 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 12 (PIM12).

Output from the P125 to P127 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 12 (POM12).

This port can also be used for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, external clock input for main system clock, serial interface data I/O, and clock I/O.

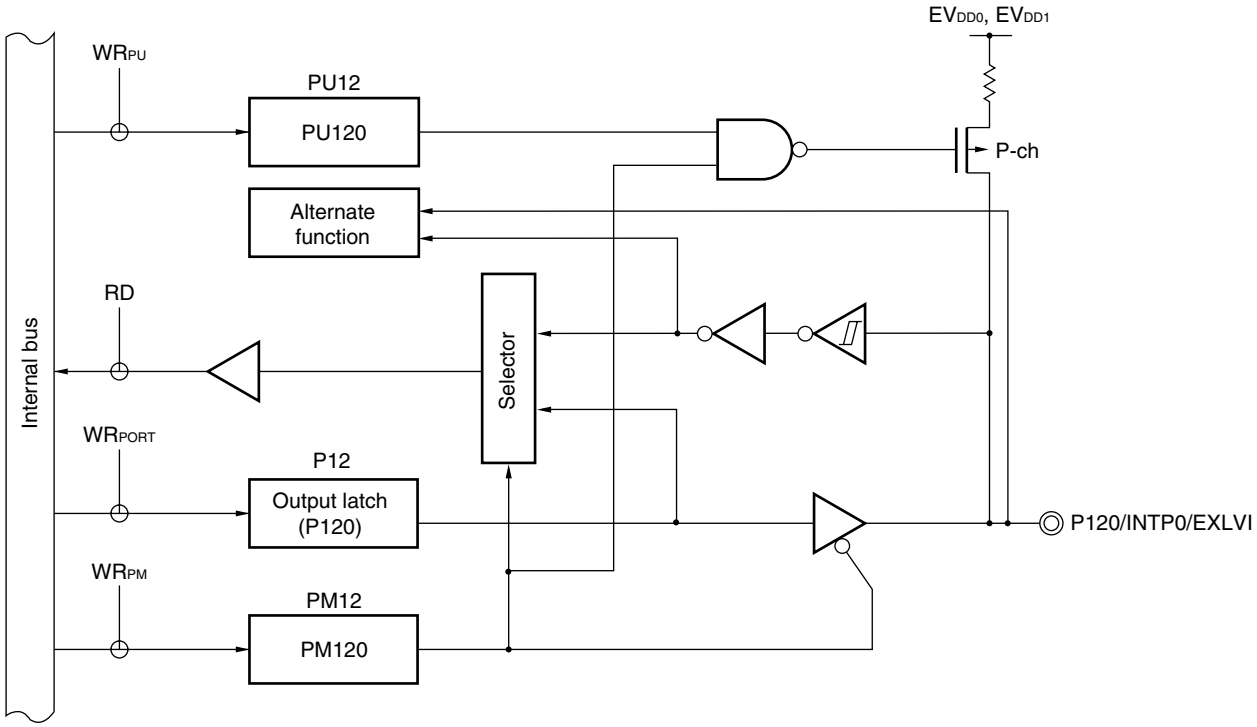
Reset signal generation sets port 12 to input mode.

Figures 4-38 to 4-42 show block diagrams of port 12.

Caution 1. The function setting on P121 to P124 is available only once after the reset release. The port once set for connection to an oscillator cannot be used as an input port unless the reset is performed.

2. To use P125/$\overline{\text{SCK21}}$/SCL21, P126/SI21/SDA21, or P127/SO21 as a general-purpose port, note the serial array unit 1 setting. For details, refer to Table 13-10 Relationship Between Register Settings and Pins (Channel 1 of Unit 1: CSI21, UART2 reception, IIC21).

Figure 4-38. Block Diagram of P120



P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
RD: Read signal
WR××: Write signal

(1) Peripheral enable register 0 (PER0)

PER0 is used to enable or disable use of each peripheral hardware macro. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the timer array unit 0 is used, be sure to set bit 0 (TAU0EN) of this register to 1.

When the timer array unit 1 is used, be sure to set bit 1 (TAU1EN) of this register to 1.

PER0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-5. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN	DACEN	ADCEN	IIC0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN

TAUmEN	Control of timer array unit m input clock
0	Stops supply of input clock. • SFR used by the timer array unit m cannot be written. • The timer array unit m is in the reset status.
1	Supplies input clock. • SFR used by the timer array unit m can be read/written.

Caution When setting the timer array unit, be sure to set TAUmEN to 1 first. If TAUmEN = 0, writing to a control register of the timer array unit is ignored, and all read values are default values (except for timer input select register m (TISm), input switch control register (ISC), noise filter enable registers 1, 2 (NFEN1, NFFN2), port mode registers 0, 1, 3, 4, 13, 14, 16 (PM0, PM1, PM3, PM4, PM13, PM14, PM16), and port registers 0, 1, 3, 4, 13, 14, 16 (P0, P1, P3, P4, P13, P14, P16)).

Remark m = 0, 1

Table 7-4. Operations from Count Operation Enabled State to TCRmn Count Start (2/2)

Timer operation mode	Operation when TSmn = 1 is set
• One-count mode	When TSmn = 0, writing 1 to TSmn bit sets the start trigger wait state. No operation is carried out from start trigger detection until count clock generation. The first count clock loads the value of TDRmn to TCRmn and the subsequent count clock performs count down operation (see **7.3 (6) (d) Start timing in one-count mode**).
• Capture & one-count mode	When TSmn = 0, writing 1 to TSmn bit sets the start trigger wait state. No operation is carried out from start trigger detection until count clock generation. The first count clock loads 0000H to TCRmn and the subsequent count clock performs count up operation (see **7.3 (6) (e) Start timing in capture & one-count mode**).

(a) Start timing in interval timer mode

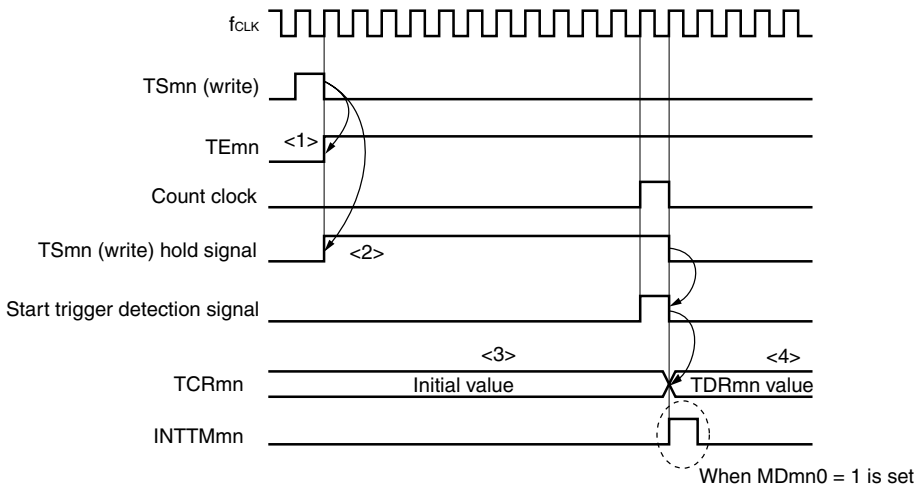
<1> Writing 1 to TSmn sets TEmn = 1

<2> The write data to TSmn is held until count clock generation.

<3> TCRmn holds the initial value until count clock generation.

<4> On generation of count clock, the “TDRmn value” is loaded to TCRmn and count starts.

Figure 7-11. Start Timing (In Interval Timer Mode)



Caution In the first cycle operation of count clock after writing TSmn, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting MDmn0 = 1.

(10) Timer output register m (TOm)

TOm is a buffer register of timer output of each channel.

The value of each bit in this register is output from the timer output pin (TOmn) of each channel.

This register can be rewritten by software only when timer output is disabled (TOEmn = 0). When timer output is enabled (TOEmn = 1), rewriting this register by software is ignored, and the value is changed only by the timer operation.

To use the P01/TO00, P16/TO01, P17/TO02, P31/TO03, P42/TO04, P46/TO05, P131/TO06, P145/TO07, P160/TO10, P161/TO11, P162/TO12, or P163/TO13 pin as a port function pin, set the corresponding TOmn bit to “0”.

TOm can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of TOm can be set with an 8-bit memory manipulation instruction with TOmL.

Reset signal generation clears this register to 0000H.

Figure 7-19. Format of Timer Output Register m (TOm)

Address: F01B8H, F01B9H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO0	0	0	0	0	0	0	0	0	TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00

Address: F01E0H, F01E1H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO1	0	0	0	0	0	0	0	0	0	0	0	0	TO13	TO12	TO11	TO10

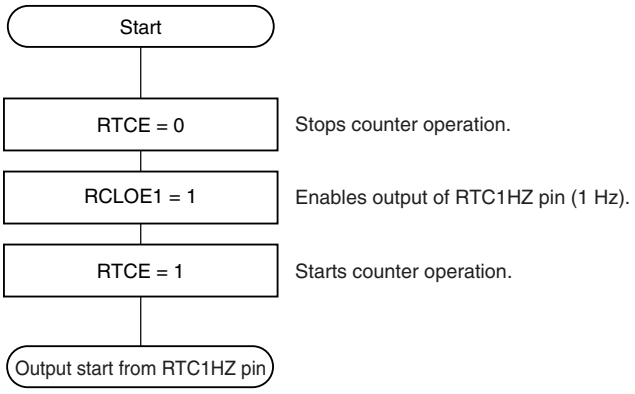
TOmn	Timer output of channel n
0	Timer output value is “0”.
1	Timer output value is “1”.

Caution Be sure to clear bits 15 to 8 of TO0 and bits 15 to 4 of TO1 to “0”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7),
mn = 00 to 07, 10 to 13

8.4.5 1 Hz output of real-time counter

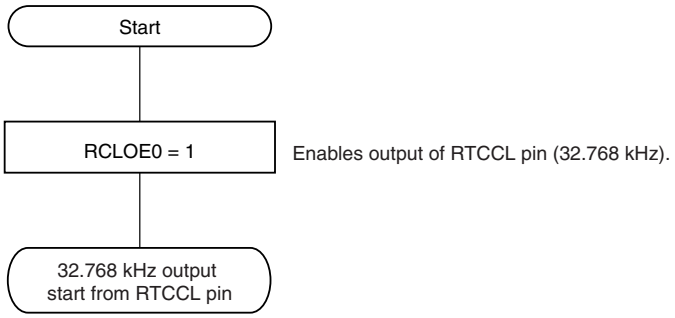
Figure 8-24. 1 Hz Output Setting Procedure



<R> **Caution First set RTCEN to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.**

<R> ### 8.4.6 32.768 kHz output of real-time counter

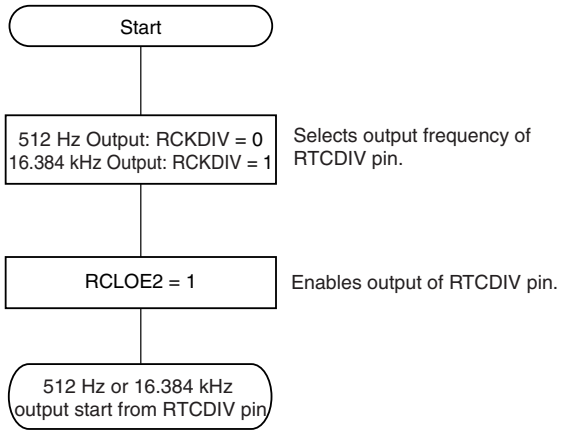
Figure 8-25. 32.768 kHz Output Setting Procedure



Caution First set RTCEN to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.

<R> ### 8.4.7 512 Hz, 16.384 kHz output of real-time counter

Figure 8-26. 512 Hz, 16.384 kHz output Setting Procedure



Caution First set RTCEN to 1, while oscillation of the subsystem clock (f_{SUB}) is stable.

Remarks 1. If the overflow time is set to $2^{10}/f_{IL}$, the window close time and open time are as follows.

	Setting of Window Open Period			
	25%	50%	75%	100%
Window close time	0 to 3.56 ms	0 to 2.37 ms	0 to 0.119 ms	None
Window open time	3.56 to 3.88 ms	2.37 to 3.88 ms	0.119 to 3.88 ms	0 to 3.88 ms

<When window open period is 25%>

- Overflow time:
  $2^{10}/f_{IL}$ (MAX.) = 2^{10}/264 kHz (MAX.) = 3.88 ms
- Window close time:
  0 to $2^{10}/f_{IL}$ (MIN.) × (1 − 0.25) = 0 to 2^{10}/216 kHz (MIN.) × 0.75 = 0 to 3.56 ms
- Window open time:
  $2^{10}/f_{IL}$ (MIN.) × (1 − 0.25) to $2^{10}/f_{IL}$ (MAX.) = 2^{10}/216 kHz (MIN.) × 0.75 to 2^{10}/264 kHz (MAX.)
  = 3.56 to 3.88 ms

2. f_{IL}: Internal low-speed oscillation clock frequency

9.4.4 Setting watchdog timer interval interrupt

Depending on the setting of bit 7 (WDTINT) of an option byte (000C0H), an interval interrupt (INTWDTI) can be generated when 75% of the overflow time is reached.

Table 9-5. Setting of Watchdog Timer Interval Interrupt

WDTINT	Use of Watchdog Timer Interval Interrupt
0	Interval interrupt is used.
1	Interval interrupt is generated when 75% of overflow time is reached.

Caution When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.
Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.
Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

Remark The watchdog timer continues counting even after INTWDTI is generated (until ACH is written to the WDTE register). If ACH is not written to the WDTE register before the overflow time, an internal reset signal is generated.

11.5.2 Registers used by temperature sensors

The following four types of registers are used when using a temperature sensor.

- Peripheral enable register 0 (PER0)
- A/D converter mode register (ADM)
- Analog input channel specification register (ADS)
- 10-bit A/D conversion result register (ADCR)

Caution Setting of the A/D port configuration register (ADPC), port mode register 2 (PM2) and port register 2 (P2) is not required when using the temperature sensor. There is no problem if the pin function is set as digital I/O.

(1) Peripheral enable register 0 (PER0)

Use the PER0 register in the same manner as during A/D converter basic operation (see **11.3 (1) Peripheral enable register 0 (PER0)**).

(2) A/D converter mode register (ADM)

Use the ADM register in the same manner as during A/D converter basic operation (see **11.3 (2) A/D converter mode register (ADM)**).

However, selection of the A/D conversion time when a temperature sensor is used varies as shown in Table 11-5.

Table 11-5. Selection of A/D Conversion Time When Using Temperature Sensor

(1) 2.7 V ≤ AV_{REF0} ≤ 5.5 V

A/D Converter Mode Register (ADM)					Conversion Time Selection				Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 2 MHz	f_{CLK} = 8 MHz	f_{CLK} = 20 MHz	
0	0	0	0	1	480/f_{CLK}	Setting prohibited	60.0 μs	24.0 μs	f_{CLK}/12
0	0	1	0	1	320/f_{CLK}		40.0 μs	Setting prohibited	f_{CLK}/8
0	1	0	0	1	240/f_{CLK}		30.0 μs		f_{CLK}/6
0	1	1	0	1	160/f_{CLK}		Setting prohibited		f_{CLK}/4
1	0	0	0	1	120/f_{CLK}	60.0 μs			f_{CLK}/3
1	0	1	0	1	80/f_{CLK}	40.0 μs			f_{CLK}/2
1	1	1	0	1	40/f_{CLK}	Setting prohibited			f_{CLK}
Other than above					Setting prohibited				

Cautions 1. Set the conversion times so as to satisfy the following condition.
f_{AD} = 0.6 to 1.8 MHz

2. When rewriting FR2 to FR0, LV1, and LV0 to other than the same data, stop A/D conversion (ADCS = 0) beforehand.

3. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

13.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) Communication

This is a clocked communication function that uses three lines: serial clock ($\overline{SCK}$) and serial data (SI and SO) lines.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

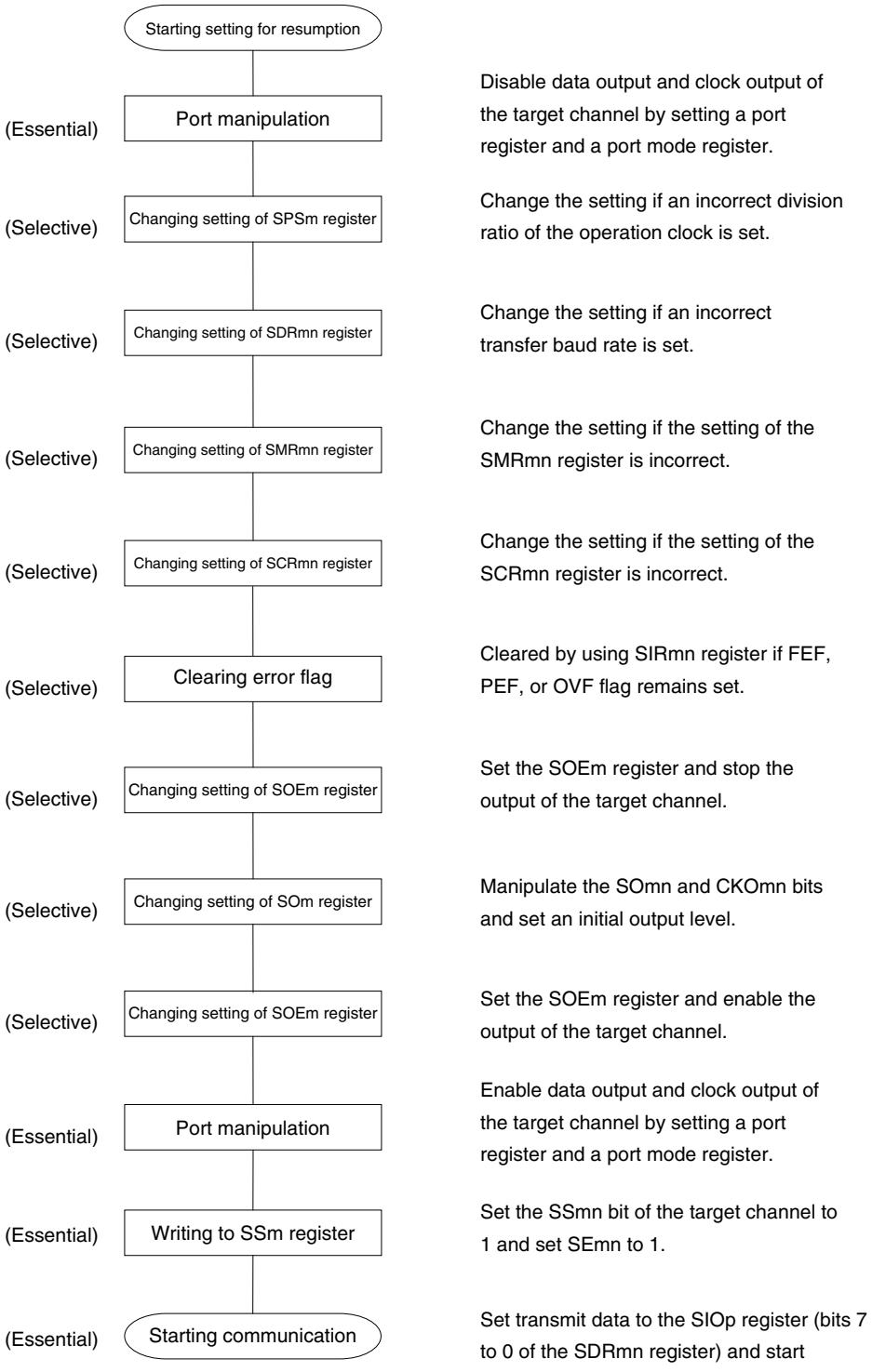
The channels supporting 3-wire serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) are channels 0 to 3 of SAU0 and channel 0 and 1 of SAU1.

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	CSI11		IIC11
1	0	CSI20	UART2	IIC20
	1	CSI21		IIC21
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–

3-wire serial I/O (CSI00, CSI01, CIS10, CIS11, CSI20, CIS21) performs the following six types of communication operations.

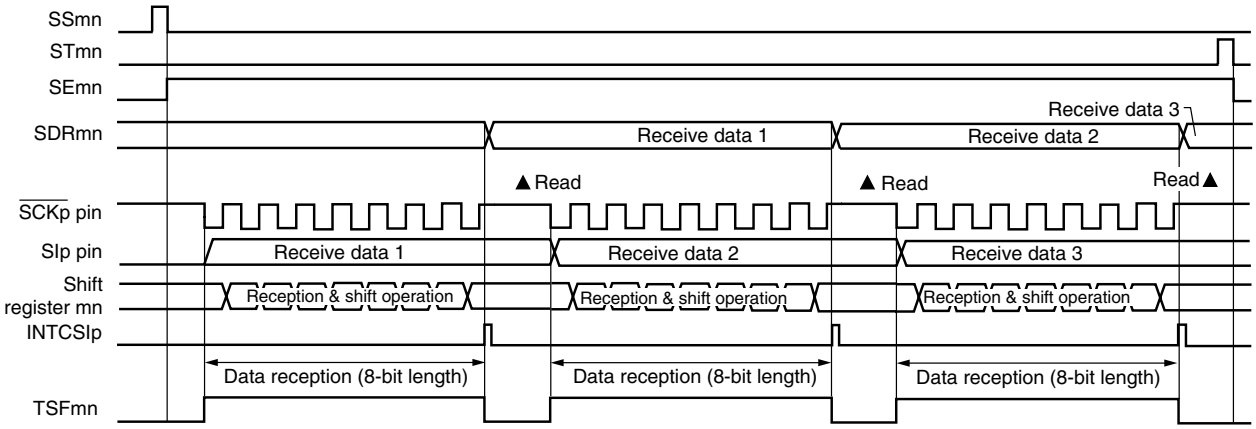
- Master transmission (See **13.5.1**.)
- Master reception (See **13.5.2**.)
- Master transmission/reception (See **13.5.3**.)
- Slave transmission (See **13.5.4**.)
- Slave reception (See **13.5.5**.)
- Slave transmission/reception (See **13.5.6**.)

Figure 13-43. Procedure for Resuming Master Transmission/Reception



(3) Processing flow (in single-reception mode)

Figure 13-60. Timing Chart of Slave Reception (in Single-Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21)

14.4 I^2C Bus Mode Functions

14.4.1 Pin configuration

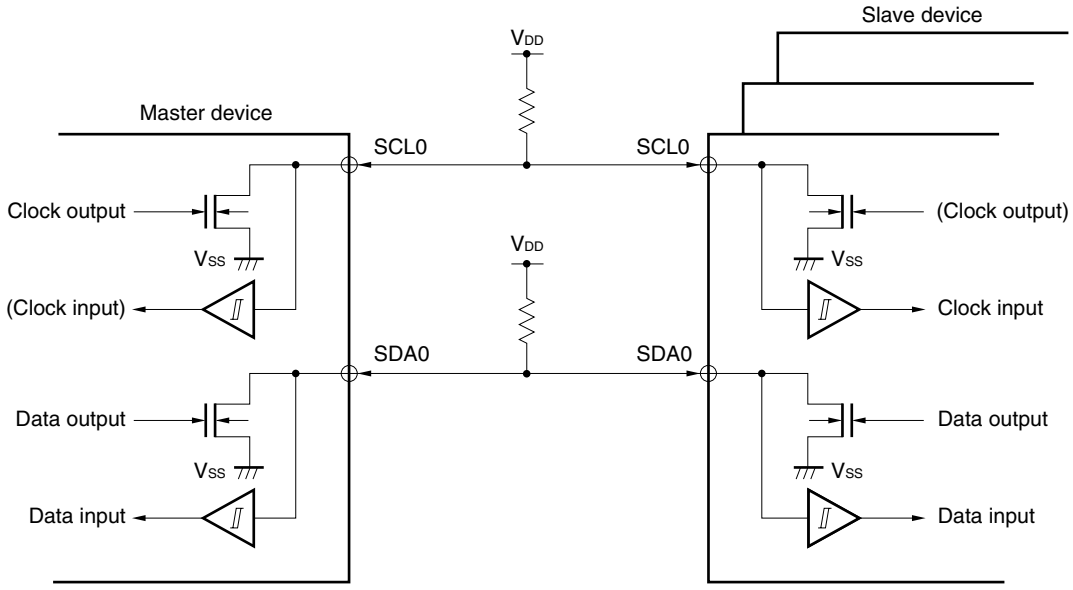
The serial clock pin (SCL0) and serial data bus pin (SDA0) are configured as follows.

(1) SCL0 ..... This pin is used for serial clock input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

(2) SDA0 ..... This pin is used for serial data input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

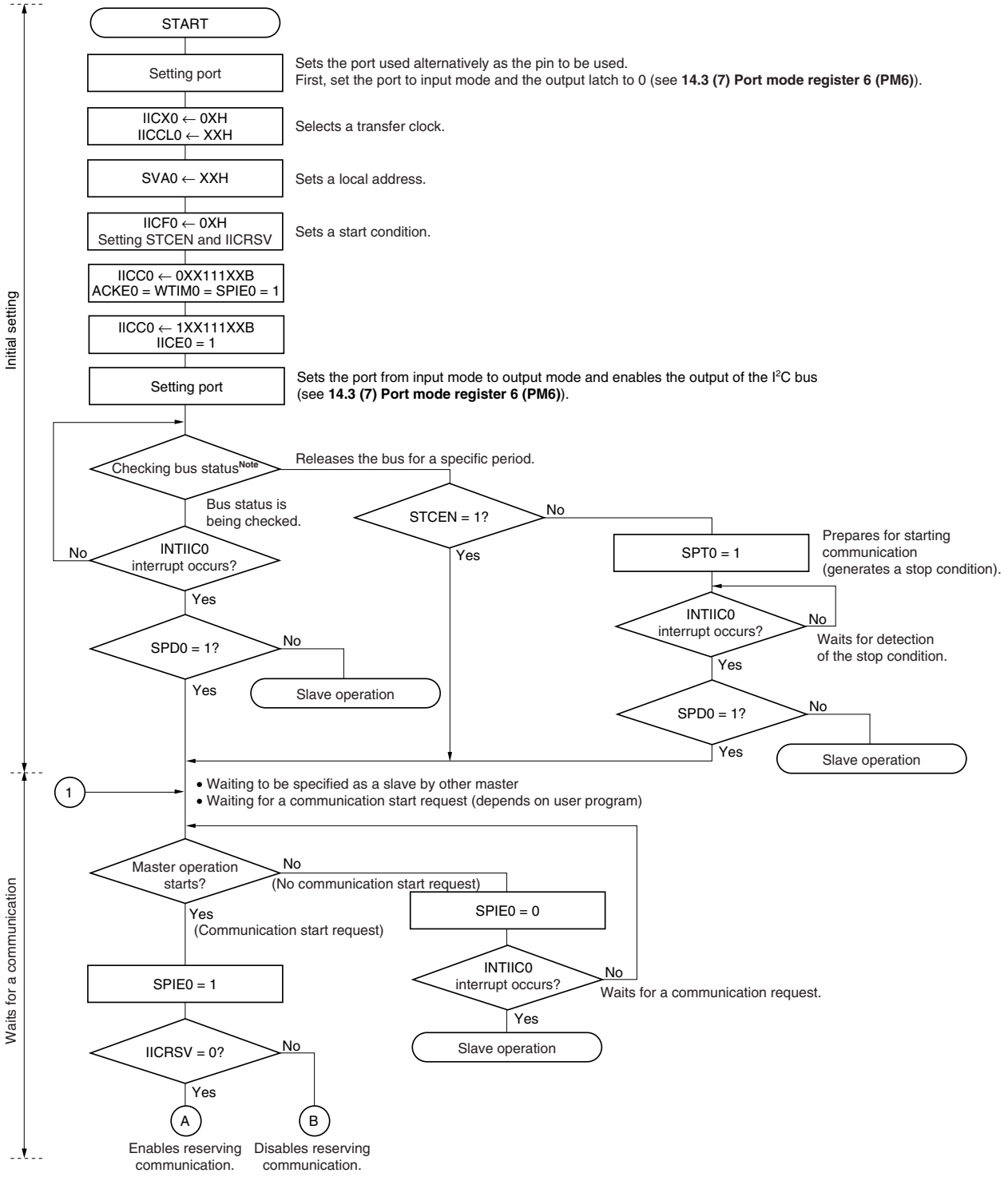
Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

Figure 14-12. Pin Configuration Diagram



(2) Master operation in multi-master system

Figure 14-25. Master Operation in Multi-Master System (1/3)



Note Confirm that the bus is released (CLD0 bit = 1, DAD0 bit = 1) for a specific period (for example, for a period of one frame). If the SDA0 pin is constantly at low level, decide whether to release the I^2C bus (SCL0 and SDA0 pins = high level) in conformance with the specifications of the product that is communicating.

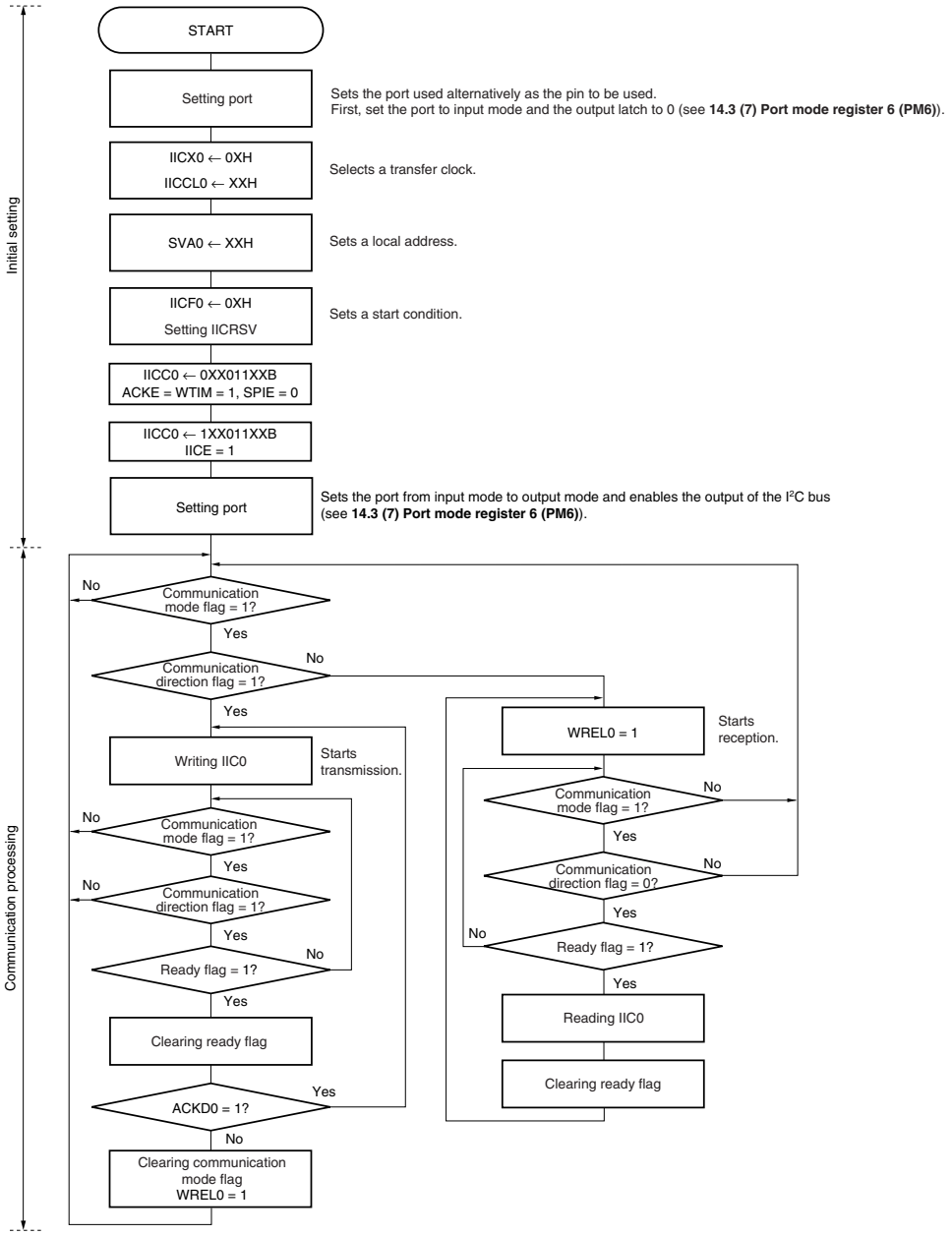
The main processing of the slave operation is explained next.

Start serial interface IIC0 and wait until communication is enabled. When communication is enabled, execute communication by using the communication mode flag and ready flag (processing of the stop condition and start condition is performed by an interrupt. Here, check the status by using the flags).

The transmission operation is repeated until the master no longer returns ACK. If $\overline{\text{ACK}}$ is $\overline{\text{not}}$ returned from the master, communication is completed.

For reception, the necessary amount of data is received. When communication is completed, ACK is $\overline{\text{not}}$ returned as the next data. After that, the master generates a stop condition or restart condition. Exit from the communication status occurs in this way.

Figure 14-26. Slave Operation Flowchart (1)



Remark Conform to the specifications of the product that is in communication, regarding the transmission and reception formats.

(2) DMA operation control register n (DRCn)

DRCn is a register that is used to enable or disable transfer of DMA channel n.

Rewriting bit 7 (DENn) of this register is prohibited during operation (when DSTn = 1).

DRCn can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16-5. Format of DMA Operation Control Register n (DRCn)

Address: FFFBCH (DRC0), FFFBDH (DRC1) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
DRCn	DENn	0	0	0	0	0	0	DSTn

DENn	DMA operation enable flag
0	Disables operation of DMA channel n (stops operating cock of DMA).
1	Enables operation of DMA channel n.
The DMA controller waits for a DMA trigger when DSTn = 1 after DMA operation is enabled (DENn = 1).	

DSTn	DMA transfer mode flag
0	DMA transfer of DMA channel n is completed.
1	DMA transfer of DMA channel n is not completed (still under execution).
The DMA controller waits for a DMA trigger when DSTn = 1 after DMA operation is enabled (DENn = 1). When a software trigger (STGn) or the start source trigger set by IFCn3 to IFCn0 is input, DMA transfer is started. When DMA transfer is completed after that, this bit is automatically cleared to 0. Write 0 to this bit to forcibly terminate DMA transfer under execution.	

Caution The DSTn flag is automatically cleared to 0 when a DMA transfer is completed. Writing the DENn flag is enabled only when DSTn = 0. When a DMA transfer is terminated without waiting for generation of the interrupt (INTDMAn) of DMAn, therefore, set DSTn to 0 and then DENn to 0 (for details, refer to 16.5.7 Forced termination by software).

Remark n: DMA channel number (n = 0, 1)

Table 17-2. Flags Corresponding to Interrupt Request Sources (3/3)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTTM05	TMIF05	IF2L	TMMK05	MK2L	TMPR005, TMPR105	PR02L, PR12L
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106	
INTTM07	TMIF07		TMMK07		TMPR007, TMPR107	
INTP6	PIF6		PMK6		PPR06, PPR16	
INTP7	PIF7		PMK7		PPR07, PPR17	
INTP8	PIF8		PMK8		PPR08, PPR18	
INTP9	PIF9		PMK9		PPR09, PPR19	
INTP10	PIF10		PMK10		PPR010, PPR110	
INTP11	PIF11	IF2H	PMK11	MK2H	PPR011, PPR111	PR02H, PR12H
INTTM10	TMIF10		TMMK10		TMPR010, TMPR110	
INTTM11	TMIF11		TMMK11		TMPR011, TMPR111	
INTTM12	TMIF12		TMMK12		TMPR012, TMPR112	
INTTM13	TMIF13		TMMK13		TMPR013, TMPR113	

(1) Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

IF0L, IF0H, IF1L, IF1H, IF2L, and IF2H can be set by a 1-bit or 8-bit memory manipulation instruction. When IF0L and IF0H, IF1L and IF1H, and IF2L and IF2H are combined to form 16-bit registers IF0, IF1, and IF2, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 17-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H) (1/2)

Address: FFFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF

Address: FFFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	SREIF0	SRIF0 CSIIF01	STIF0 CSIIF00	DMAIF1	DMAIF0	SREIF3	SRIF3	STIF3

Table 20-2. Hardware Statuses After Reset Acknowledgment (1/3)

Hardware		After Reset Acknowledgment[Note 1]
Program counter (PC)		The contents of the reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		06H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Port registers (P0 to P9, P11 to P16) (output latches)		00H
Port mode registers (PM0 to PM9, PM11 to PM16)		FFH
Port input mode registers 0, 4, 9, 12, 14 (PIM0, PIM4, PIM9, PIM12, PIM14)		00H
Port output mode registers 0, 4, 9, 12, 14 (POM0, POM4, POM9, POM12, POM14)		00H
Pull-up resistor option registers (PU0, PU1, PU3 to PU9, PU11 to PU14, PU16)		00H
Memory extension mode control register (MEM)		00H
Clock operation mode control register (CMC)		00H
Clock operation status control register (CSC)		C0H
Processor mode control register (PMC)		00H
System clock control register (CKC)		09H
Oscillation stabilization time counter status register (OSTC)		00H
Oscillation stabilization time select register (OSTS)		07H
Noise filter enable registers 0, 1, 2 (NFEN0, NFEN1, NFEN2)		00H
Peripheral enable registers 0, 1 (PER0, PER1)		00H
Internal high-speed oscillator trimming register (HIOTRM)		10H
Operation speed mode control register (OSMC)		00H
Timer array unit (TAU)	Timer data registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TDR00, TDR01, TDR02, TDR03, TDR04, TDR05, TDR06, TDR07, TDR10, TDR11, TDR12, TDR13)	0000H
	Timer mode registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TMR00, TMR01, TMR02, TMR03, TMR04, TMR05, TMR06, TMR07, TMR10, TMR11, TMR12, TMR13)	0000H
	Timer status registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TSR00, TSR01, TSR02, TSR03, TSR04, TSR05, TSR06, TSR07, TSR10, TSR11, TSR12, TSR13)	0000H
	Timer input select registers 0, 1 (TIS0, TIS1)	00H
	Timer counter registers 00, 01, 02, 03, 04, 05, 06, 07, 10, 11, 12, 13 (TCR00, TCR01, TCR02, TCR03, TCR04, TCR05, TCR06, TCR07, TCR10, TCR11, TCR12, TCR13)	FFFFH
	Timer channel enable status registers 0, 1 (TE0, TE1)	0000H
	Timer channel start registers 0, 1 (TS0, TS1)	0000H
	Timer channel stop registers 0, 1 (TT0, TT1)	0000H
	Timer clock select registers 0, 1 (TPS0, TPS1)	0000H
	Timer output registers 0, 1 (TO0, TO1)	0000H
	Timer output enable registers 0, 1 (TOE0, TOE1)	0000H
	Timer output level registers 0, 1 (TOL0, TOL1)	0000H
	Timer output mode registers 0, 1 (TOM0, TOM1)	0000H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. When a reset is executed in the standby mode, the pre-reset status is held even after reset.

A/D Converter Characteristics (1/2)

(T_A = –40 to +85°C, 2.3 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 2.3 V ≤ AV_{REF0} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

(a) Conventional-specification products (μPD78F117x)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				10	bit
Overall error[Notes 1, 2]	AINL	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF0} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF0} < 2.7 V			±0.7	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF0} ≤ 5.5 V	6.1		66.6	μs
		2.7 V ≤ AV_{REF0} < 4.0 V	12.2		66.6	μs
		2.3 V ≤ AV_{REF0} < 2.7 V	27		66.6	μs
Zero-scale error[Notes 1, 2]	EZS	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF0} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF0} < 2.7 V			±0.6	%FSR
Full-scale error[Notes 1, 2]	EFS	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF0} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF0} < 2.7 V			±0.6	%FSR
Integral linearity error[Note 1]	ILE	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF0} < 4.0 V			±4.5	LSB
		2.3 V ≤ AV_{REF0} < 2.7 V			±4.5	LSB
Differential linearity error[Note 1]	DLE	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF0} < 4.0 V			±2.0	LSB
		2.3 V ≤ AV_{REF0} < 2.7 V			±2.0	LSB
Analog input voltage	V_{AIN}	2.3 V ≤ AV_{REF0} ≤ 5.5 V	AV_{SS}		AV_{REF0}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 29	Hard	Electrical specifications (standard products)	During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)	Select the normal input buffer for SIj and $\overline{SCKj}$ and the normal output mode for SOj by using the PIMg and POMg registers.	p.820 □
			During communication at same potential (simplified I^2C mode)	Select the normal input buffer and the N-ch open-drain output (V_{DD} tolerance) mode for SDAr and the normal output mode for SCLr by using the PIMg and POMg registers.	p.823 □
			During communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output)	Select the TTL input buffer for RxDq and the N-ch open-drain output (V_{DD} tolerance) mode for TxDq by using the PIMg and POMg registers.	pp.824, 825, 827 □
			During communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output)	Select the TTL input buffer for SIp and the N-ch open-drain output (V_{DD} tolerance) mode for SOp and $\overline{SCKp}$ by using the PIMg and POMg registers.	pp.828 to 830 □
			During communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)	Select the TTL input buffer for SIp and $\overline{SCKp}$ and the N-ch open-drain output (V_{DD} tolerance) mode for SOp by using the PIMg and POMg registers.	pp.832, 833 □
			During communication at different potential (2.5 V, 3 V) (simplified I^2C mode)	Select the TTL input buffer and the N-ch open-drain output (V_{DD} tolerance) mode for SDAr and the N-ch open-drain output (V_{DD} tolerance) mode for SCLr by using the PIMg and POMg registers.	pp.834, 835 □

C.2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

(1/13)

Edition	Description	Chapter
2nd edition	Deletion of target from the capacitance value of the capacitor connected to the REGC pin	Throughout
	Change of corresponding pins of EV_{DD} and V_{DD} in **Table 2-1. Pin I/O Buffer Power Supplies**	CHAPTER 2 PIN FUNCTIONS
	Change of description in **2.2.21 REGC**	
	Change of description in **2.2.24 FLMD0**	
	Modification of P60 to P64, P110 and P111 in **Table 2-2. Connection of Unused Pins**	
	Modification of 12-D to 12-G, 37-A to 37-B, and 39 to 2-W in **Table 2-2. Connection of Unused Pins**	
	Modification of 12-D to 12-G, 37-A to 37-B, and 39 to 2-W in **Figure 2-1. Pin I/O Circuit List**	
	Change of address in **Figure 3-16. Configuration of General-Purpose Registers**	CHAPTER 3 CPU ARCHITECTURE
	Addition of register and **Note** in **Table 3-5. SFR List**	
	Addition of the BCDADJ register to **Table 3-6. Extended SFR (2nd SFR) List (1/6)**	
	Change of address of the SOL0 register in **Table 3-6. Extended SFR (2nd SFR) List (2/6)**	
	Change of address and symbol of the SOL1 register in **Table 3-6. Extended SFR (2nd SFR) List (3/6)**	
	Addition of PIM register and POM register in block diagram	CHAPTER 4 PORT FUNCTIONS
	Change of corresponding pins of EV_{DD} and V_{DD} in **Table 4-1. Pin I/O Buffer Power Supplies**	
	Change of **Cautions 1** and **Cautions 2** in **4.2.1 Port 0**	
	Change of **Cautions 1, Cautions 2**, and **Cautions 3** in **4.2.2 Port 1**	
	Change of **Cautions 1** and addition of **Cautions 2** in **4.2.4 Port 3**	
	Change of **Cautions 2** and **Cautions 3** in **4.2.5 Port 4**	
	Addition of **Caution** to **4.2.7 Port 6**	
	Change of **Caution** in **4.2.10 Port 9**	
	Change of **Figure 4-36. Block Diagram of P110 and P111**	
	Addition of description to **4.2.12 Port 12** and change of **Cautions 2**	
	Change of **Caution** in **4.2.13 Port 13**	
	Change of **Cautions 1** and **Cautions 2** and addition of **Cautions 3** to **4.2.14 Port 14**	
	Change of **Caution** in **4.2.16 Port 16**	
	Addition description to **(4) Port input mode registers (PIM0, PIM4, PIM9, PIM12, PIM14)** and **(5) Port output mode registers (POM0, POM4, POM9, POM12, POM14)** in **4.3**	
	Change of **Figure 4-56. Bit Manipulation Instruction (P10)**	
	Addition of description to **5.1 Functions of External Bus Interface**	CHAPTER 5 EXTERNAL BUS INTERFACE
	Addition of description to title of **(d)** in **Figure 5-5. Timing to Write to External Memory**	
	Change of **(b)** and **(d)** in **Figure 5-6. Timing to Read External Memory**	
	Addition of description to title of **(c)** in **Figure 5-7. Timing to Write to External Memory**	