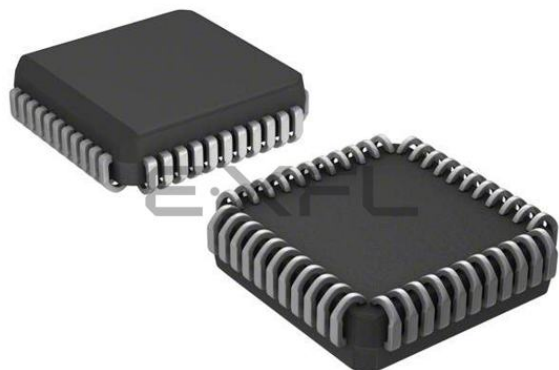




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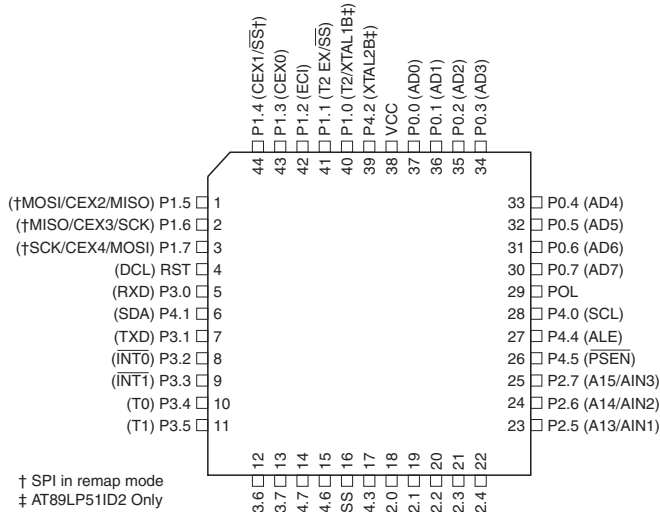
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Details

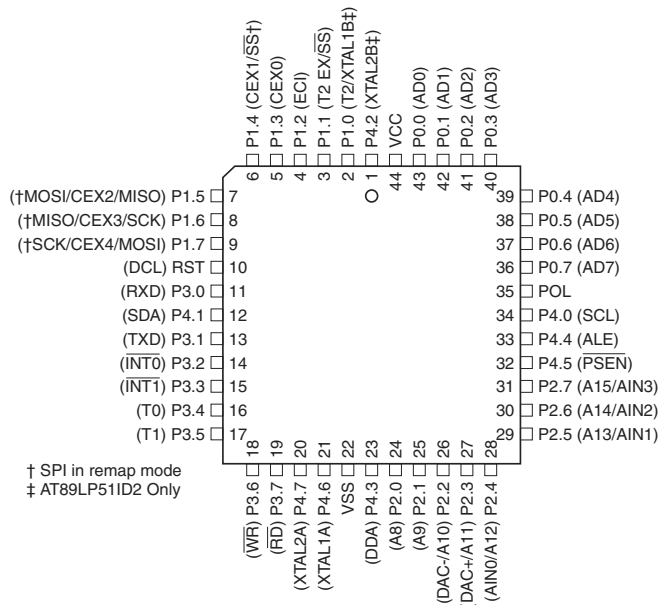
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.375K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp51rb2-20ju

1. Pin Configurations

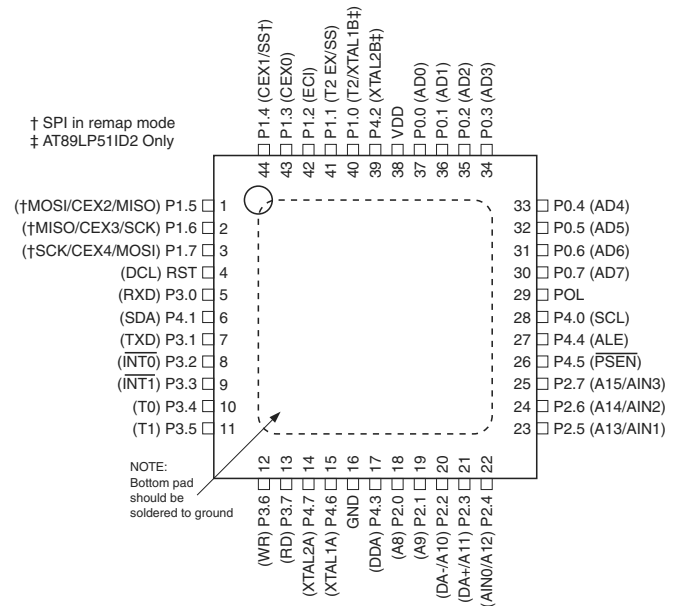
1.1 44-lead VQFP



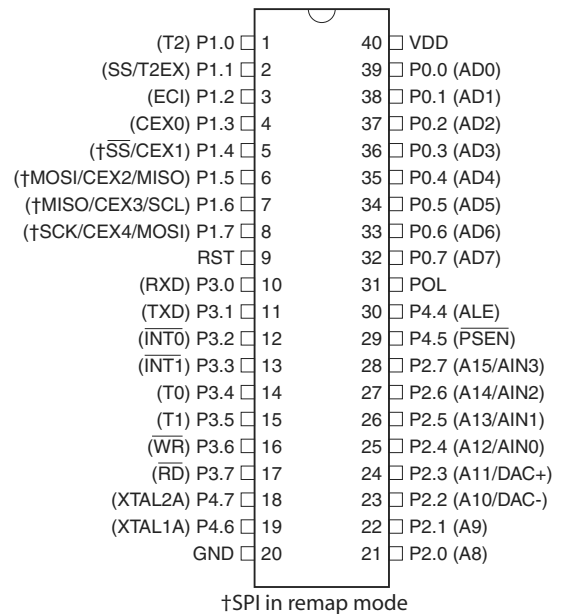
1.2 44-lead PLCC



1.3 44-pad VQFN/QFN/MLF



1.4 40-pin PDIP



1.5 Pin Description

Table 1-1. Atmel AT89LP51RB2/RC2/IC2 Pin Description

Pin Number			Symbol	Type	Description
VQFP VQFN	PLCC	PDIP			
1	7	6	P1.5	I/O I/O I/O I/O	P1.5: User-configurable I/O Port 1 bit 5. MISO: SPI master-in/slave-out. When configured as master, this pin is an input. When configured as slave, this pin is an output. MOSI: SPI master-out/slave-in (Remap mode). When configured as master, this pin is an output. When configured as slave, this pin is an input. During In-System Programming, this pin is an input. CEX2: Capture/Compare external I/O for PCA module 2.
2	8	7	P1.6	I/O I/O I/O I/O	P1.6: User-configurable I/O Port 1 bit 6. SCK: SPI Clock. When configured as master, this pin is an output. When configured as slave, this pin is an input. MISO: SPI master-in/slave-out (Remap mode). When configured as master, this pin is an input. When configured as slave, this pin is an output. During In-System Programming, this pin is an output. CEX3: Capture/Compare external I/O for PCA module 3.
3	9	8	P1.7	I/O I/O I/O I/O	P1.7: User-configurable I/O Port 1 bit 7. MOSI: SPI master-out/slave-in. When configured as master, this pin is an output. When configured as slave, this pin is an input. SCK: SPI Clock (Remap mode). When configured as master, this pin is an output. When configured as slave, this pin is an input. During In-System Programming, this pin is an input. CEX4: Capture/Compare external I/O for PCA module 4.
4	10	9	RST	I/O I	RST: External Reset input (Reset polarity depends on POL pin). The RST pin can output a pulse when the internal Watchdog reset or POR is active. DCL: Serial Debug Clock input for On-Chip Debug Interface when OCD is enabled.
5	11	10	P3.0	I/O I	P3.0: User-configurable I/O Port 3 bit 0. RXD: Serial Port Receiver Input.
6	12		P4.1	I/O I/O	P4.1: User-configurable I/O Port 4 bit 1. SDA: TWI bidirectional Serial Data line.
7	13	11	P3.1	I/O O	P3.1: User-configurable I/O Port 3 bit 1. TXD: Serial Port Transmitter Output.
8	14	12	P3.2	I/O I	P3.2: User-configurable I/O Port 3 bit 2. INT0: External Interrupt 0 Input or Timer 0 Gate Input.
9	15	13	P3.3	I/O I	P3.3: User-configurable I/O Port 3 bit 3. INT1: External Interrupt 1 Input or Timer 1 Gate Input
10	16	14	P3.4	I/O I/O	P3.4: User-configurable I/O Port 3 bit 4. T1: Timer/Counter 0 External input or output.
11	17	15	P3.5	I/O I/O	P3.5: User-configurable I/O Port 3 bit 5. T1: Timer/Counter 1 External input or output.
12	18	16	P3.6	I/O O	P3.6: User-configurable I/O Port 3 bit 6. WR: External memory interface Write Strobe (active-low).
13	19	17	P3.7	I/O O	P3.7: User-configurable I/O Port 3 bit 7. RD: External memory interface Read Strobe (active-low).
14	20	18	P4.7	I/O O	P4.7: User-configurable I/O Port 4 bit 7. XTAL2A: Output from inverting oscillator amplifier A. It may be used as a port pin if the internal RC oscillator or external clock is selected as the clock source A.
15	21	19	P4.6	I/O I	P4.6: User-configurable I/O Port 4 bit 6. XTAL1A: Input to the inverting oscillator amplifier A and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source A.

Table 1-1. Atmel AT89LP51RB2/RC2/IC2 Pin Description

Pin Number			Symbol	Type	Description
VQFP VQFN	PLCC	PDIP			
16	22	20	GND	I	Ground
17	23		P4.3	I/O I/O	P4.3: User-configurable I/O Port 4 bit 3. DDA: Bidirectional Debug Data line for the On-Chip Debug Interface when OCD is enabled.
18	24	21	P2.0	I/O O	P2.0: User-configurable I/O Port 2 bit 0. A8: External memory interface Address bit 8.
19	25	22	P2.1	I/O O	P2.1: User-configurable I/O Port 2 bit 1. A9: External memory interface Address bit 9.
20	26	23	P2.1	I/O O O	P2.2: User-configurable I/O Port 2 bit 2. DA-: DAC negative differential output. A10: External memory interface Address bit 10.
21	27	24	P2.3	I/O O O	P2.3: User-configurable I/O Port 2 bit 3. DA+: DAC positive differential output. A11: External memory interface Address bit 11.
22	28	25	P2.4	I/O I O	P2.4: User-configurable I/O Port 2 bit 5. AIN0: Analog Comparator Input 0. A12: External memory interface Address bit 12.
23	29	26	P2.5	I/O I O	P2.5: User-configurable I/O Port 2 bit 5. AIN1: Analog Comparator Input 1. A13: External memory interface Address bit 13.
24	30	27	P2.6	I/O I O	P2.6: User-configurable I/O Port 2 bit 6. AIN2: Analog Comparator Input 2. A14: External memory interface Address bit 14.
25	31	28	P2.7	I/O I O	P2.7: User-configurable I/O Port 2 bit 7. AIN3: Analog Comparator Input 3. A15: External memory interface Address bit 15.
26	32	29	P4.5	I/O O	P4.5: User-configurable I/O Port 4 bit 5. PSEN: External memory interface Program Store Enable (active-low).
27	33	30	P4.4	I/O I/O	P4.4: User-configurable I/O Port 4 bit 4. ALE: External memory interface Address Latch Enable.
28	34		P4.0	I/O	P4.0: User-configurable I/O Port 4 bit 0. SCL: TWI Serial Clock line. This line is an output in master mode and an input in slave mode.
29	35	31	POL	I	POL: Reset polarity
30	36	32	P0.7	I/O I/O	P0.7: User-configurable I/O Port 0 bit 7. AD7: External memory interface Address/Data bit 7.
31	37	33	P0.6	I/O I/O I	P0.6: User-configurable I/O Port 0 bit 6. AD6: External memory interface Address/Data bit 6. ADC6: ADC analog input 6.
32	38	34	P0.5	I/O I/O I	P0.5: User-configurable I/O Port 0 bit 5. AD5: External memory interface Address/Data bit 5. ADC5: ADC analog input 5.
33	39	35	P0.4	I/O I/O I	P0.4: User-configurable I/O Port 0 bit 4. AD4: External memory interface Address/Data bit 4. ADC4: ADC analog input 4.
34	40	36	P0.3	I/O I/O I	P0.3: User-configurable I/O Port 0 bit 3. AD3: External memory interface Address/Data bit 3. ADC3: ADC analog input 3.

Table 1-1. Atmel AT89LP51RB2/RC2/IC2 Pin Description

Pin Number			Symbol	Type	Description
VQFP VQFN	PLCC	PDIP			
35	41	37	P0.2	I/O I/O I	P0.2: User-configurable I/O Port 0 bit 2. AD2: External memory interface Address/Data bit 2. ADC2: ADC analog input 2.
36	42	38	P0.1	I/O I/O I	P0.1: User-configurable I/O Port 0 bit 1. AD1: External memory interface Address/Data bit 1. ADC1: ADC analog input 1.
37	43	39	P0.0	I/O I/O I	P0.0: User-configurable I/O Port 0 bit 0. AD0: External memory interface Address/Data bit 0. ADC0: ADC analog input 0.
38	44	40	VDD	I	Supply Voltage
39	1		P4.2	I/O	P4.2: User-configurable I/O Port 4bit 2. XTAL2B: Output from low-frequency inverting oscillator amplifier B (AT89LP51IC2 only). It may be used as a port pin if the internal RC oscillator or external clock is selected as the clock source B.
40	2	1	P1.0	I/O I/O	P1.0: User-configurable I/O Port 1 bit 0. T2: Timer 2 External Input or Clock Output. XTAL1B: Input to the low-frequency inverting oscillator amplifier B and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source B.
41	3	2	P1.1	I/O I I	P1.1: User-configurable I/O Port 1 bit 1. T2EX: Timer 2 External Capture/Reload Input. SS: SPI Slave-Select.
42	4	3	P1.2	I/O	P1.2: User-configurable I/O Port 1 bit 2.
43	5	4	P1.3	I/O I/O	P1.3: User-configurable I/O Port 1 bit 3. CEX0: Capture/Compare external I/O for PCA module 0.
44	6	5	P1.4	I/O I I/O	P1.4: User-configurable I/O Port 1 bit 4. SS: SPI Slave-Select (Remap Mode). This pin is an input for In-System Programming CEX1: Capture/Compare external I/O for PCA module 1.

2. Overview

The Atmel® AT89LP51RB2/RC2/IC2 is a low-power, high-performance CMOS 8-bit 8051 micro-controller with 64KB of In-System Programmable Flash program memory. The devices are manufactured using Atmel's high-density nonvolatile memory technology and are compatible with the industry-standard 80C51 instruction set.

The AT89LP51RB2/RC2/IC2 is built around an enhanced CPU core that can fetch a single byte from memory every clock cycle. In the classic 8051 architecture, each fetch requires 6 clock cycles, forcing instructions to execute in 12, 24 or 48 clock cycles. In the AT89LP51RB2/RC2/IC2 CPU, standard instructions need only one to four clock cycles providing six to twelve times more throughput than the standard 8051. Seventy percent of instructions need only as many clock cycles as they have bytes to execute, and most of the remaining instructions require only one additional clock. The enhanced CPU core is capable of 20 MIPS throughput whereas the classic 8051 CPU can deliver only 4 MIPS at the same current consumption. Conversely, at the same throughput as the classic 8051, the new CPU core runs at a much lower speed and thereby greatly reducing power consumption and EMI. The AT89LP51RB2/RC2/IC2 also includes a compatibility mode that will enable classic 12 clock per machine cycle operation for true timing compatibility with the Atmel AT89C51RB2/RC2.



The AT89LP51RB2/RC2/IC2 retains all of the standard features of the AT89C51RB2/RC2, including: 64KB of In-System Programmable Flash program memory, 256 bytes of RAM, 1152 bytes of expanded RAM, up to 40 I/O lines, three 16-bit timer/counters, a Programmable Counter Array, a programmable hardware watchdog timer, a keyboard interface, a full-duplex enhanced serial port, a serial peripheral interface (SPI), on-chip crystal oscillator, and a four-level, ten-vector interrupt system. A block diagram is shown in Figure 2-1.

In addition, the Atmel® AT89LP51RB2/RC2/IC2 provides a Two-Wire Interface (TWI) for up to 400KB/s serial transfer; a 10-bit, 8-channel Analog-to-Digital Converter (ADC) with temperature sensor and digital-to-analog (DAC) mode; two analog comparators; and an 8MHz internal oscillator.

Some standard features on the AT89LP51RB2/RC2/IC2 are enhanced with new modes or operations. Mode 0 of Timer 0 or Timer 1 acts as a variable 9–16 bit timer/counter and Mode 1 acts as a 16-bit auto-reload timer/counter. In addition, each timer/counter may independently drive an 8-bit precision pulse width modulation output. Mode 0 (synchronous mode) of the serial port allows flexibility in the phase/polarity relationship between clock and data.

The I/O ports of the AT89LP51RB2/RC2/IC2 can be independently configured in one of four operating modes. In quasi-bidirectional mode, the ports operate as in the classic 8051. In input-only mode, the ports are tristated. Push-pull output mode provides full CMOS drivers and open-drain mode provides just a pull-down. Unlike other 8051s, this allows Port 0 to operate with on-chip pull-ups if desired.

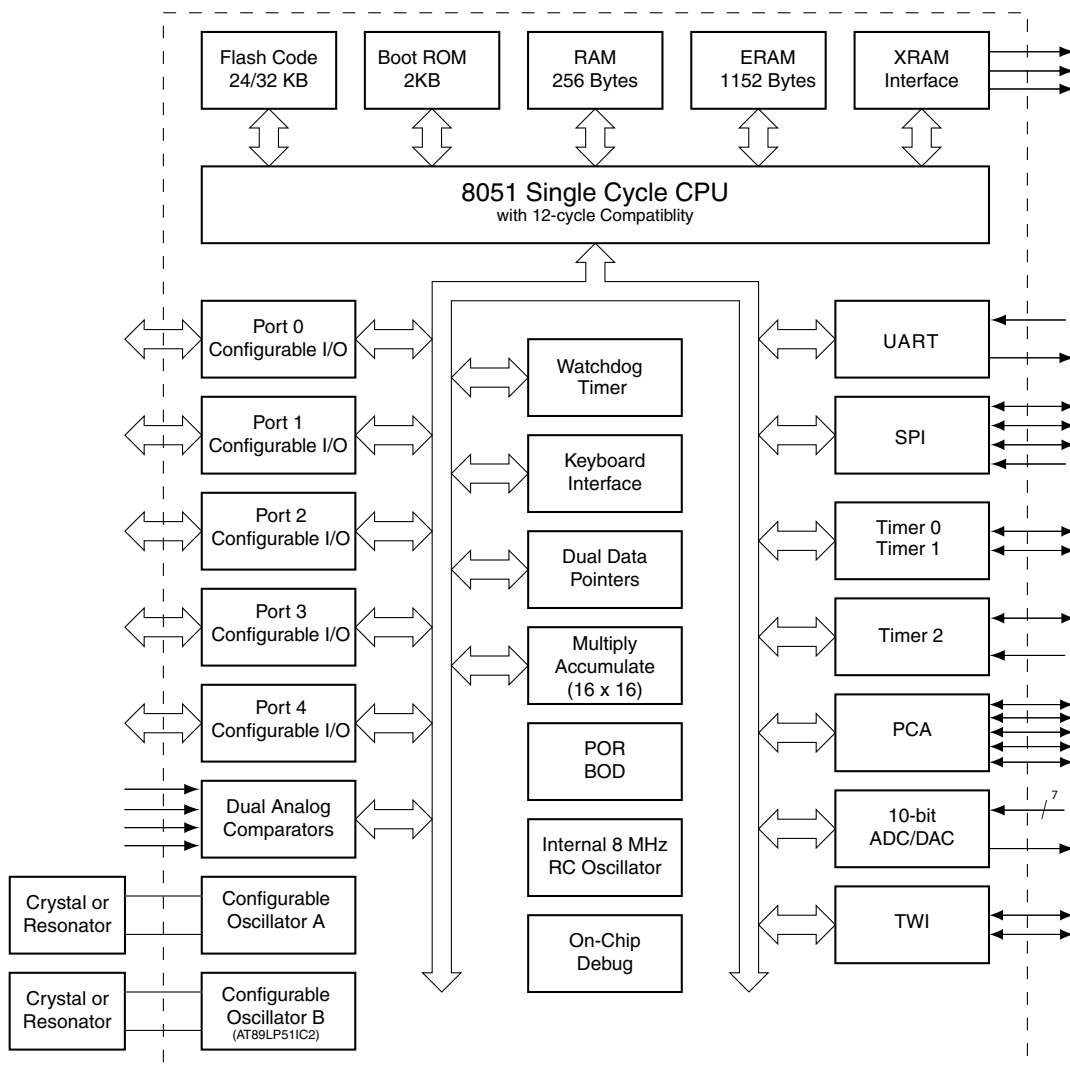
The AT89LP51RB2/RC2/IC2 includes an On-Chip Debug (OCD) interface that allows read-modify-write capabilities of the system state and program flow control, and programming of the internal memories. The on-chip Flash may also be programmed through the UART-based boot-loader or the SPI-based In-System programming interface (ISP).

The TWI and OCD features are not available on the PDIP package. The AT89LP51IC2 is also not available in PDIP.

The features of the AT89LP51RB2/RC2/IC2 make it a powerful choice for applications that need pulse width modulation, high speed I/O, and counting capabilities such as alarms, motor control, corded phones, and smart card readers.

2.1 Block Diagram

Figure 2-1. Atmel AT89LP51RB2/RC2/IC2 Block Diagram



2.2 System Configuration

The AT89LP51RB2/RC2/IC2 supports several system configuration options. Nonvolatile options are set through user fuses that must be programmed through the flash programming interface. Volatile options are controlled by software through individual bits of special function registers (SFRs). The AT89LP51RB2/RC2/IC2 must be properly configured before correct operation can occur.

2.2.1 Fuse Options

Table 2-1 lists the fusible options for the AT89LP51RB2/RC2/IC2. These options maintain their state even when the device is powered off. Some may be changed through the FLash API but others can only be changed with an external device programmer. For more information, see datasheet.

2.3.4 Timer/Counters

A common prescaler is available to divide the time base for Timer 0, Timer 1, Timer 2 and the WDT. The TPS_{3-0} bits in the CLKREG SFR control the prescaler. In Compatibility mode TPS_{3-0} defaults to 0101B, which causes the timers to count once every machine cycle. The counting rate can be adjusted linearly from the system clock rate to 1/16 of the system clock rate by changing TPS_{3-0} . In Fast mode TPS_{3-0} defaults to 0000B, or the system clock rate. TPS does not affect Timer 2 in Clock Out or Baud Generator modes.

In Compatibility mode the sampling of the external Timer/Counter pins: T0, T1, T2 and T2EX; and the external interrupt pins, $\overline{INT0}$ and $\overline{INT1}$, is also controlled by the prescaler. In Fast mode these pins are always sampled at the system clock rate.

Both Timer 0 and Timer 1 can toggle their respective counter pins, T0 and T1, when they overflow by setting the output enable bits in TCONB.

2.3.5 Interrupt Handling

Fast mode allows for faster interrupt response due to the shorter instruction execution times.

2.3.6 Keyboard Interface

The AT89LP51RB2/RC2/IC2 does not clear the keyboard flag register (KBF) after a read. Each bit must be cleared in software. This allows the interrupt to be generate once per flag when multiple flags are set, if desired. To mimic the old behavior the service routine must clear the whole register.

The keyboard can also support general edge-triggered interrupts with the addition of the KBMOD register.

2.3.7 Serial Port

The timer prescaler increases the range of achievable baud rates when using Timer 1 to generate the baud rate in UART Modes 1 or 3, including an increase in the maximum baud rate available in Compatibility mode. Additional features include automatic address recognition and framing error detection.

The shift register mode (Mode 0) has been enhanced with more control of the polarity, phase and frequency of the clock and full-duplex operation. This allows emulation of master serial peripheral (SPI) and two-wire (TWI) interfaces.

2.3.8 I/O Ports

The P0, P1, P2 and P3 I/O ports of the AT89LP51RB2/RC2/IC2 may be configured in four different modes. The default setting depends on the Tristate-Port User Fuse. When the fuse is set all the I/O ports revert to input-only (tristated) mode at power-up or reset. When the fuse is not active, ports P1, P2 and P3 start in quasi-bidirectional mode and P0 starts in open-drain mode. P4 always operates in quasi-bidirectional mode. P0 can be configured to have internal pull-ups by placing it in quasi-bidirectional or output modes. This can reduce system cost by removing the need for external pull-ups on Port 0.

The P4.4–P4.7 pins are additional I/Os that replace the normally dedicated ALE, PSEN, XTAL1 and XTAL2 pins of the AT89C51RB2/RC2/IC2. These pins can be used as additional I/Os depending on the configuration of the clock and external memory.

2.3.9 Security

The AT89LP51RB2/RC2/IC2 does not support the external access pin ($\overline{EA}$). Therefore it is not possible to execute from external program memory in address range 0000H–1FFFFH. When the third Lockbit is enabled (Lock Mode 4) external program execution is disabled for all addresses above 1FFFFH. This differs from AT89C51RB2/RC2/IC2 where Lock Mode 4 prevents $\overline{EA}$ from being sampled low, but may still allow external execution at addresses outside the 8K internal space.

2.3.10 Programming

The AT89LP51RB2/RC2/IC2 supports a richer command set for In-System Programming (ISP). Existing AT89C51RB2/RC2 programmers should be able to program the AT89LP51RB2/RC2/IC2 in byte mode. In page mode the AT89LP51RB2/RC2/IC2 only supports programming of a half-page of 64 bytes and therefore requires an extra address byte as compared to AT89C51RB2/RC2. Furthermore the device signature is located at addresses 0000H, 0001H and 0003H instead of 0000H, 0100H and 0200H.

Table 2-3. Compatibility Mode versus Fast Mode Summary

Feature	Compatibility	Fast
Instruction Fetch in System Clocks	3	1
Instruction Execution Time in System Clocks	6, 12, 18 or 24	1, 2, 3, 4 or 5
Default System Clock Divisor	2	1
Default Timer Prescaler Divisor	6	1
Pin Sampling Rate ($\overline{INT0}$, $\overline{INT1}$, T0, T1, T2, T2EX)	Prescaler Rate	System Clock
Minimum RST input pulse in System Clocks	12	2

3. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 3-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

Table 3-1. Atmel AT89LP51RB2/RC2/IC2 SFR Map and Reset Values

	8	9	A	B	C	D	E	F	
0F8H		CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		0FFH
0F0H	B 0000 0000		RL0 0000 0000	RL1 0000 0000	RH0 0000 0000	RH1 0000 0000	PAGE 0000 0000	BX 0000 0000	0F7H
0E8H		CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000	SPX xxxx x000	0EFH
0E0H	ACC 0000 0000	AX 0000 0000	DSPR 0000 0000	FIRD 0000 0000	MACL 0000 0000	MACH 0000 0000	P0M0 (2)	P0M1 0000 0000	0E7H
0D8H	CCON 00x0 0000	CMOD 00xx x000	CCAPM0 x000 0000	CCAPM1 x000 0000	CCAPM2 x000 0000	CCAPM3 x000 0000	CCAPM4 x000 0000		0DFH
0D0H	PSW 0000 0000	FCON xxxx 0000			DPLB 0000 0000	DPHB 0000 0000	P1M0 (2)	P1M1 0000 0000	0D7H
0C8H	T2CON 0000 0000	T2MOD 0000 0000	RCAP2L 0000 000	RCAP2H 0000 0000	TL2 0000 000	TH2 0000 0000	P2M0 (2)	P2M1 0000 0000	0CFH
0C0H	P4 1111 1111			SPCON 0001 0100	SPSTA 0000 0000	SPDAT xxxx xxxx	P3M0 (2)	P3M1 0000 0000	0C7H
0B8H	IPL0 xx00 0000	SADEN 0000 0000				AREF 0000 0000	P4M0 (2)	P4M1 0000 0000	0BFH
0B0H	P3 1111 1111	IEN1 xxxx 0000	IPL1 xxxx 0000	IPH1 xxxx 0000				IPH0 xx00 0000	0B7H
0A8H	IEN0 0x00 0000	SADDR 0000 0000		ACSRB 0000 0000	DADL 0000 0000	DADH 0000 0000	CLKREG 0101 xxxx	CKCON1 xxxx xxx0	0AFH
0A0H	P2 1111 1111	DPCF 0000 0000	AUXR1 0000 00x0	ACSRA 0000 0000	DADC 0000 0000	DADI 0000 0000	WDTRST (write-only)	WDTPRG 0000 0xx0	0A7H
98H	SCON 0000 0000	SBUF xxxx xxxx	BRL 0000 0000	BDRCON xxx0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000	KBMOD 0000 0000	9FH
90H	P1 1111 1111	TCONB 0010 0100	BMSEL xxxx xxx0	SSCON 0000 0000	SSCS 1111 1000	SSDAT 1111 1111	SSADR 1111 1110	CKRL 1111 1111	97H
88H	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 0000 0000	CKCON0 0000 0000	8FH
80H	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000		CKSEL xxxx xxx0	OSCCON xxxx x001	PCON 000x 0000	87H
	0	1	2	3	4	5	6	7	

- Notes:
1. All SFRs in the left-most column are bit-addressable.
 2. Reset value is 1111 1111B when Tristate-Port Fuse is enabled and 0000 0000B when disabled.
 3. Reset value is 0101 0010B when Compatibility mode is enabled and 0000 0000B when disabled.

Table 3-5. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	–	–	EADC	ECMP	–	ESPI	ETWI	EKB
IPH0	B7h	Interrupt Priority Control High 0	IP1D	PPCH	PT2H	PHS	PT1H	PX1H	PT0H	PX0H
IPL0	B8h	Interrupt Priority Control Low 0	IP0D	PPCL	PT2L	PLS	PT1L	PX1L	PT0L	PX0L
IPH1	B3h	Interrupt Priority Control High 1	IP3D	–	PADL	PCMPL	–	SPIH	PTWL	PKBH
IPL1	B2h	Interrupt Priority Control Low 1	IP2D	–	PADH	PCMPH	–	SPIH	PTWH	PKBL

Table 3-6. Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	8-bit Port 0								
P1	90h	8-bit Port 1								
P2	A0h	8-bit Port 2								
P3	B0h	8-bit Port 3								
P4	C0h	8-bit Port 4								
P0M0	E6h	Port 0 Mode 0								
P0M1	E7h	Port 0 Mode 1								
P1M0	D6h	Port 1 Mode 0								
P1M1	D7h	Port 1 Mode 1								
P2M0	CEh	Port 2 Mode 0								
P2M1	CFh	Port 2 Mode 1								
P3M0	C6h	Port 3 Mode 0								
P3M1	C7h	Port 3 Mode 1								
P4M0	BEh	Port 4 Mode 0								
P4M1	BFh	Port 4 Mode 1								

Table 3-7. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								
BDRCON	9Bh	Baud Rate Control	–	–	–	BRR	TBCK	RBCK	SPD	SRC
BRL	9Ah	Baud Rate Reload								

Table 3-8. Timer SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TCON	88h	Timer/Counter 0 and 1 Control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1	M11	M01	GATE0	C/T0	M10	M00
TCONB	91h	Timer/Counter 0 and 1 Mode B								
TL0	8Ah	Timer/Counter 0 Low Byte								
TH0	8Ch	Timer/Counter 0 High Byte								
TL1	8Bh	Timer/Counter 1 Low Byte								
TH1	8Dh	Timer/Counter 1 High Byte								
RL0	F2h	Timer/Counter 0 Reload Low								
RH0	F3h	Timer/Counter 0 Reload High								
RTL1	F4h	Timer/Counter 1 Reload Low								
RH1	F5h	Timer/Counter 1 Reload High								
WDRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program						WTO2	WTO1	WTO0
T2CON	C8h	Timer/Counter 2 control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
T2MOD	C9h	Timer/Counter 2 Mode	—	—	—	—	—	—	T2OE	DCEN
RCAP2H	CBh	Timer/Counter 2 Reload/Capture High Byte								
RCAP2L	CAh	Timer/Counter 2 Reload/Capture Low Byte								
TH2	CDh	Timer/Counter 2 High Byte								
TL2	CCh	Timer/Counter 2 Low Byte								

Table 3-9. SPI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SPCON	C3h	SPI Control	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
SPSTA	C4h	SPI Status	SPIF	WCOL	SSERR	MODF				
SPDAT	C5h	SPI Data	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Table 3-10. TWI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SSCON	93h	Synchronous Serial Control	SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
SSCS	94h	Synchronous Serial Status	SSC4	SSC3	SSC2	SSC1	SSC0	0	0	0
SSDAT	95h	Synchronous Serial Data								
SSADR	96h	Synchronous Serial Address	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSGC

Table 3-11. Keyboard Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBLS	9Ch	Keyboard Level Selector	KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS1	KBLS0
KBE	9Dh	Keyboard Input Enable	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0
KBF	9Eh	Keyboard Flag Register	KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0
KBMOD	9Fh	Keyboard Mode Register	KBM7	KBM6	KBM5	KBM4	KBM3	KBM2	KBM1	KBM0

Table 3-12. Flash Memory SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
BMSEL	92h	Bank Mode Select Register	–	–	–	–	–	–	–	FBS
FCON	D2h	Flash Control Register	FPSL3	FPSL2	FPSL1	FPSL0	FPS	FMOD1	FMOD0	FBUSY

Table 3-13. Analog Comparator SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACSRA	A3h	Comparator A Control Register								
ACSRB	ABh	Comparator B Control Register								
AREF	BDh	Comparator Reference Register								

Table 3-14. ADC Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
DADC	A4h	DAC/ADC Control Register								
DADI	A5h	DAC/ADC Input Register								
DADL	ACH	DAC/ADC Data Low Register								
DADH	ADh	DAC/ADC Data High Register								

Table 3-15. PCA SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CCON	D8h	PCA Timer/Counter Control	CF	CR		CCF4	CCF3	CCF2	CCF1	CCF0
CMOD	D9h	PCA Timer/Counter Mode	CIDL	WDTE				CPS1	CPS0	ECF
CL	E9h	PCA Timer/Counter Low Byte								
CH	F9h	PCA Timer/Counter High Byte								
CCAPM0	DAh	PCA Timer/Counter Mode 0		ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
CCAPM1	DBh	PCA Timer/Counter Mode 1		ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
CCAPM2	DCh	PCA Timer/Counter Mode 2		ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
CCAPM3	DDh	PCA Timer/Counter Mode 3		ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3

4. Ordering Information

4.1 Green Package Option (Pb/Halide-free)

Supply Voltage	Speed ⁽¹⁾	Temperature Range	Code Flash	# Oscillators	Ordering Code	Package	Packing
2.4V to 5.5V	20 MHz	Industrial (-40° C to 85° C)	24KB	1	AT89LP51RB2-20AAU	44AA (LQFP)	Tray
					AT89LP51RB2-20AAUR		Reel
					AT89LP51RB2-20AU	44A (TQFP)	Tray
					AT89LP51RB2-20AUR		Reel
					AT89LP51RB2-20JU	44J (PLCC)	Stick
					AT89LP51RB2-20JUR		Reel
					AT89LP51RB2-20MU	44M1 (VQFN)	Tray
					AT89LP51RB2-20MUR		Reel
					AT89LP51RB2-20PU	40P6 (PDIP)	Stick
			32KB	1	AT89LP51RC2-20AAU	44AA (LQFP)	Tray
					AT89LP51RC2-20AAUR		Reel
					AT89LP51RC2-20AU	44A (TQFP)	Tray
					AT89LP51RC2-20AUR		Reel
					AT89LP51RC2-20JU	44J (PLCC)	Stick
					AT89LP51RC2-20JUR		Reel
					AT89LP51RC2-20MU	44M1 (VQFN)	Tray
					AT89LP51RC2-20MUR		Reel
					AT89LP51RC2-20PU	40P6 (PDIP)	Stick
			32KB	2	AT89LP51IC2-20AAU	44AA (LQFP)	Tray
					AT89LP51IC2-20AAUR		Reel
					AT89LP51IC2-20AU	44A (TQFP)	Tray
					AT89LP51IC2-20AUR		Reel
					AT89LP51IC2-20JU	44J (PLCC)	Stick
					AT89LP51IC2-20JUR		Reel
					AT89LP51IC2-20MU	44M1 (VQFN)	Tray
					AT89LP51IC2-20MUR		Reel

- Notes: 1. Speed is specified for single-cycle Fast Mode with X2 clock
2. See Table 4-1 on page 19 for a cross reference between AT89C51RB2/RC2/IC2 and AT89LP51RB2/RC2/IC2

Package Types	
44AA	44-lead, Very Thin Plastic Quad Flat Package, 1.2 mm Thickness (VQFP/LQFP)
44A	44-lead, Thin Plastic Quad Flat Package, 1.0 mm Thickness (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
44M1	44-pad, 7 x 7 x 1.0 mm Body, Plastic Very Thin Quad Flat No Lead Package (VQFN/MLF)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

4.2 Cross Reference with AT89C51RB2/RC2/IC2

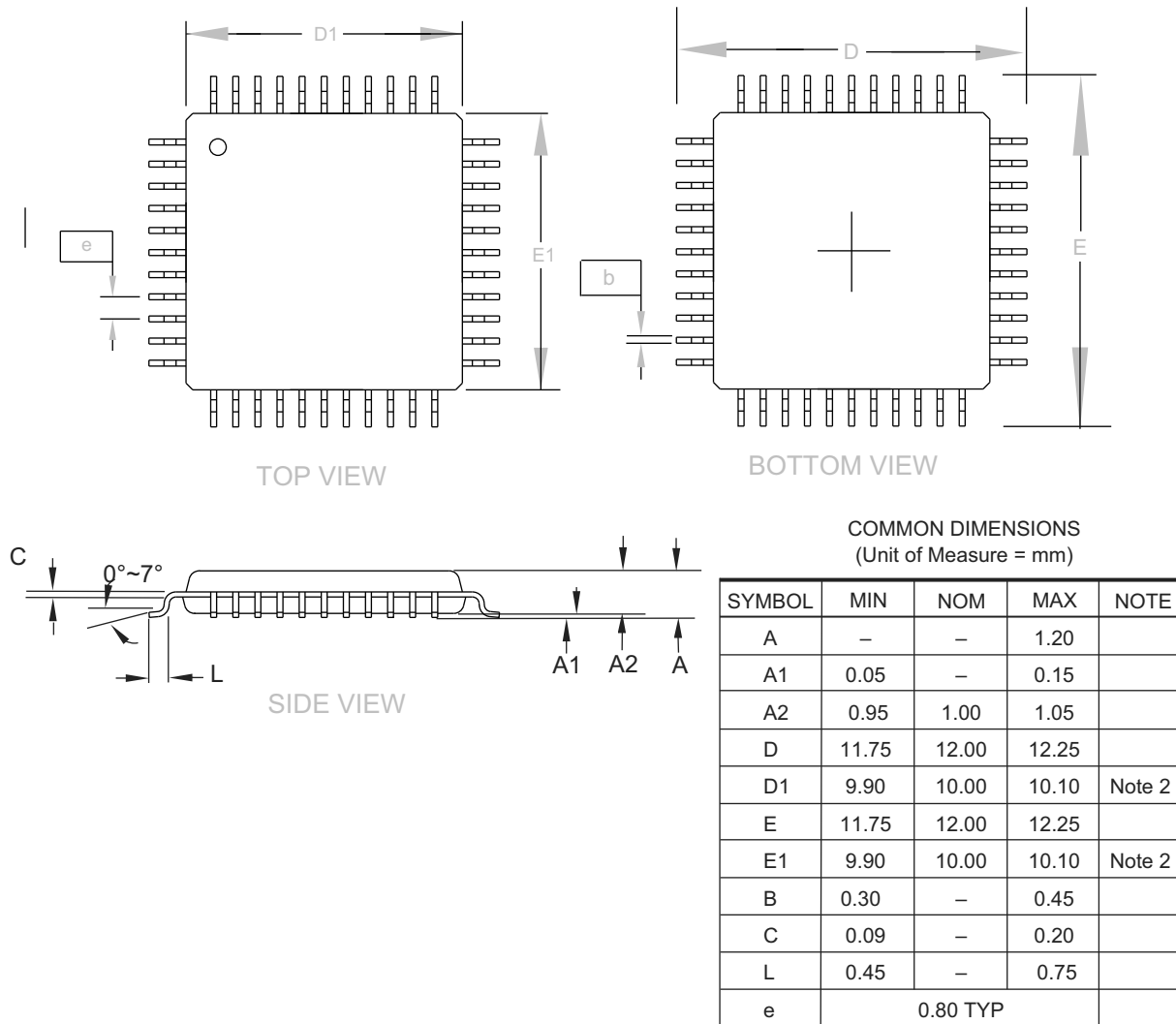
Table 4-1. Ordering Cross Reference AT89C51RB2/RC2/IC2 to AT89LP51RB2/RC2/IC2

Device Migration	Package	Packing	Previous Ordering Code	New Ordering Code
AT89C51RB2 to AT89LP51RB2	PLCC44	Stick	AT89C51RB2-SLSUM	AT89LP51RB2-20JU
		Reel	AT89C51RB2-SLRUM	AT89LP51RB2-20JU + SL383
	VQFP44	Tray	AT89C51RB2-RLTUM	AT89LP51RB2-20AAU
		Reel	AT89C51RB2-RLRUM	AT89LP51RB2-20AAU + SL383
AT89C51RC2 to AT89LP51RC2	PLCC44	Stick	AT89C51RC2-SLSUM	AT89LP51RC2-20JU
		Reel	AT89C51RC2-SLRUM	AT89LP51RC2-20JU + SL383
	VQFP44	Tray	AT89C51RC2-RLTUM	AT89LP51RC2-20AAU
		Reel	AT89C51RC2-RLRUM	AT89LP51RC2-20AAU + SL383
AT89C51IC2 to AT89LP51IC2	PLCC44	Stick	AT89C51IC2-SLSUM	AT89LP51IC2-20JU
		Reel	AT89C51IC2-SLRUM	AT89LP51IC2-20JU + SL383
	VQFP44	Tray	AT89C51IC2-RLTUM	AT89LP51IC2-20AAU
		Reel	AT89C51IC2-RLRUM	AT89LP51IC2-20AAU + SL383

Table 4-2. Packages Not Found in AT89C51RB2/RC2/IC2

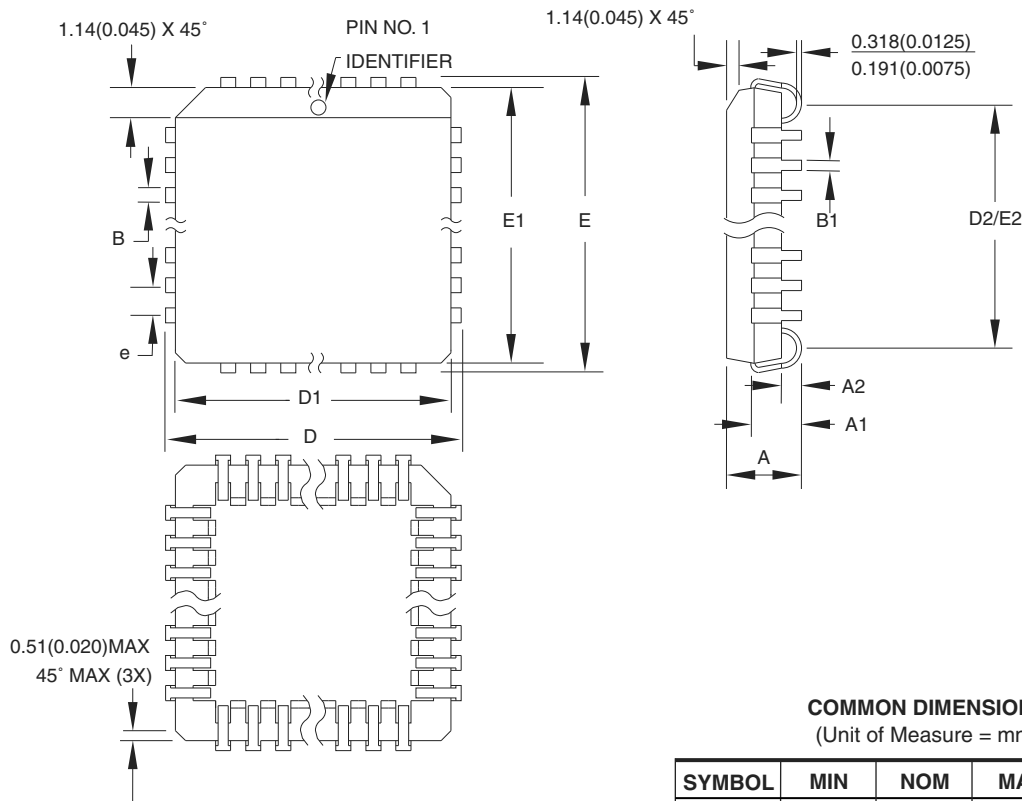
Device	Package	Packing	Ordering Code
AT89C51RB2 to AT89LP51RB2	TQFP44	Tray	AT89LP51RD2-20AU
		Reel	AT89LP51RD2-20AUR
	VQFN44	Tray	AT89LP51RD2-20MU
		Reel	AT89LP51RD2-20MUR
AT89C51RC2 to AT89LP51RC2	TQFP44	Tray	AT89LP51ED2-20AU
		Reel	AT89LP51ED2-20AUR
	VQFN44	Tray	AT89LP51ED2-20MU
		Reel	AT89LP51ED2-20MUR
AT89C51IC2 to AT89LP51IC2	TQFP44	Tray	AT89LP51ID2-20AU
		Reel	AT89LP51ID2-20AUR
	VQFN44	Tray	AT89LP51ID2-20MU
		Reel	AT89LP51ID2-20MUR

5.2 44A – TQFP



- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

5.3 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

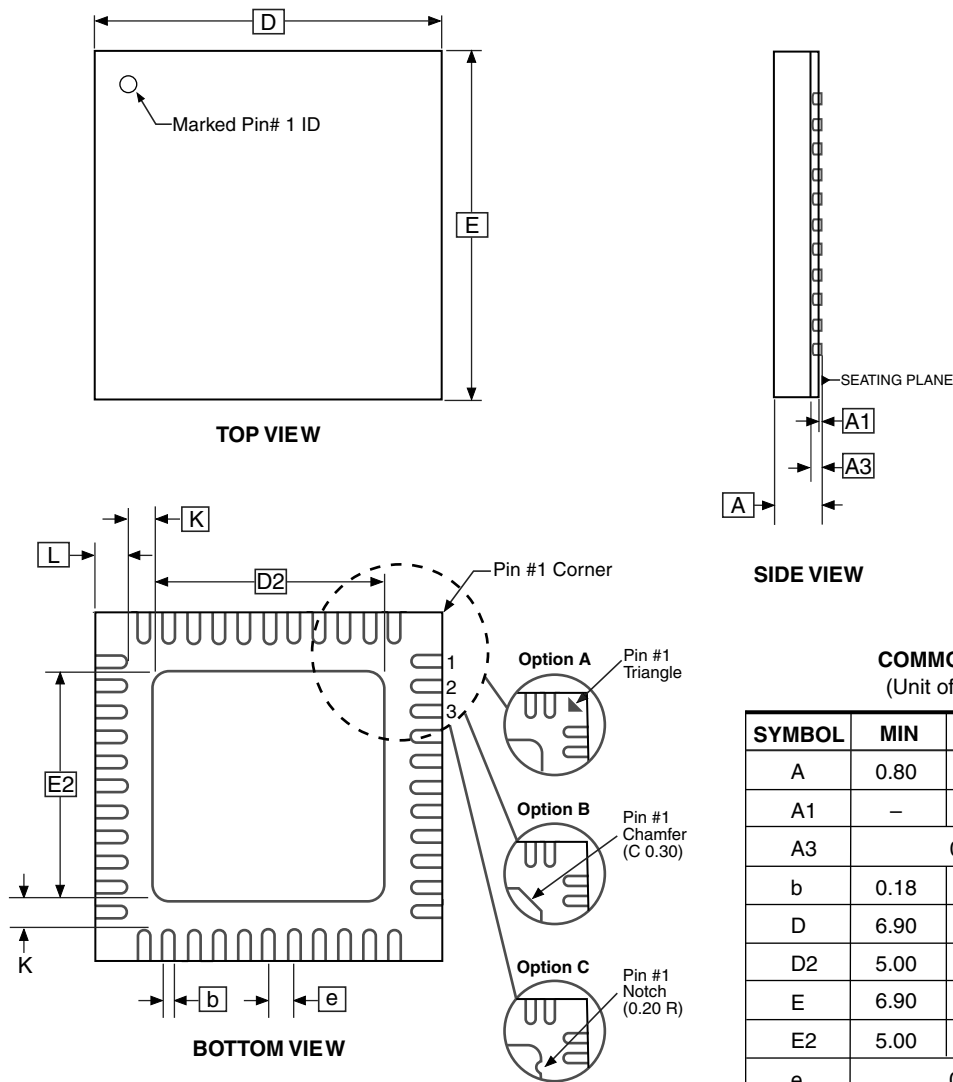
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

2325 Orchard Parkway San Jose, CA 95131	TITLE 44J , 44-lead, Plastic J-leaded Chip Carrier (PLCC)	DRAWING NO. 44J	REV. B
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5.4 44M1 – VQFN/MLF



Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

9/26/08

Package Drawing Contact:
packagedrawings@atmel.com

TITLE
44M1, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)

GPC

ZWS

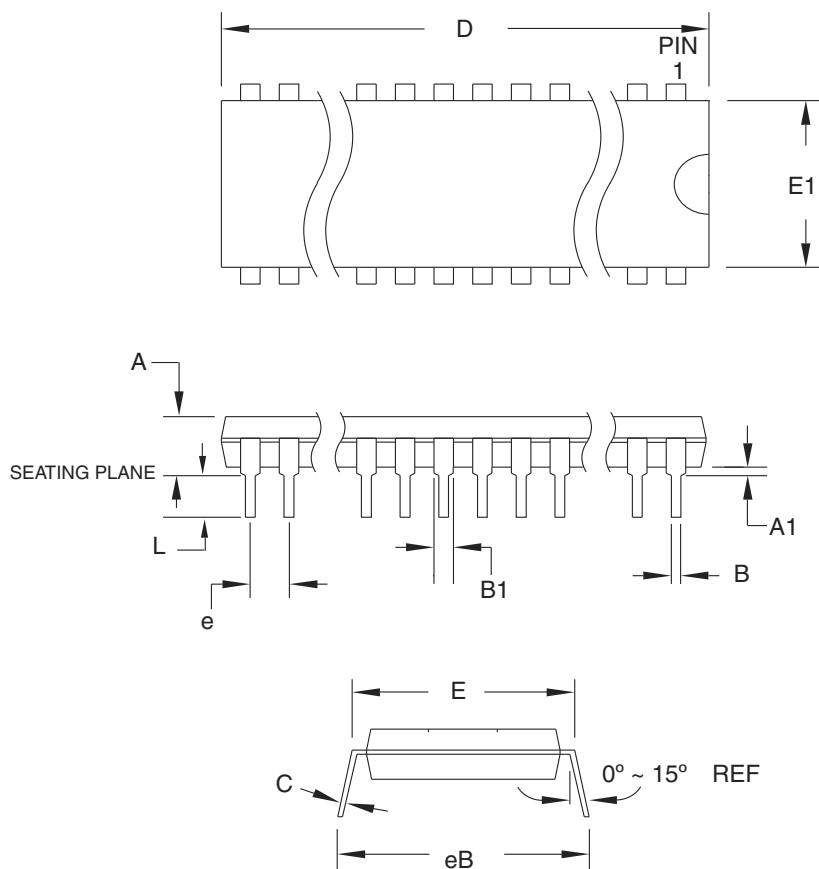
DRAWING NO.

44M1

REV.

H

5.5 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
 2. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

2325 Orchard Parkway San Jose, CA 95131	TITLE 40P6 , 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO. 40P6	REV. B
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6. Revision History

Revision No.	History
Revision A – October 2011	Initial Release

**Atmel Corporation**

2325 Orchard Parkway
San Jose, CA 95131
USA

Tel: (+1) (408) 441-0311

Fax: (+1) (408) 487-2600

www.atmel.com

8051@atmel.com

Atmel Asia Limited

Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG

Tel: (+852) 2245-6100

Fax: (+852) 2722-1369

Atmel Munich GmbH

Business Campus
Packring 4
D-85748 Garching b. Munich
GERMANY

Tel: (+49) 89-31970-0

Fax: (+49) 89-3194621

Atmel Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
JAPAN

Tel: (+81) (3) 3523-3551

Fax: (+81) (3) 3523-7581

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