Atmel - AT89LP51RC2-20MU Datasheet

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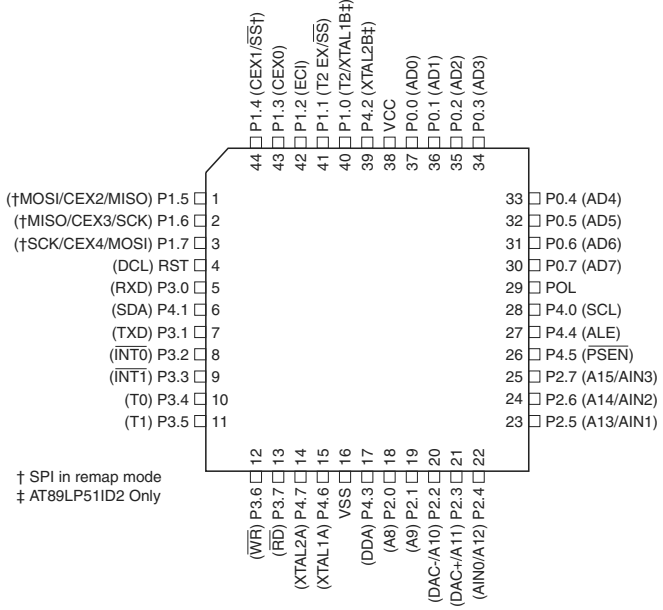
Applications of "Embedded - Microcontrollers"

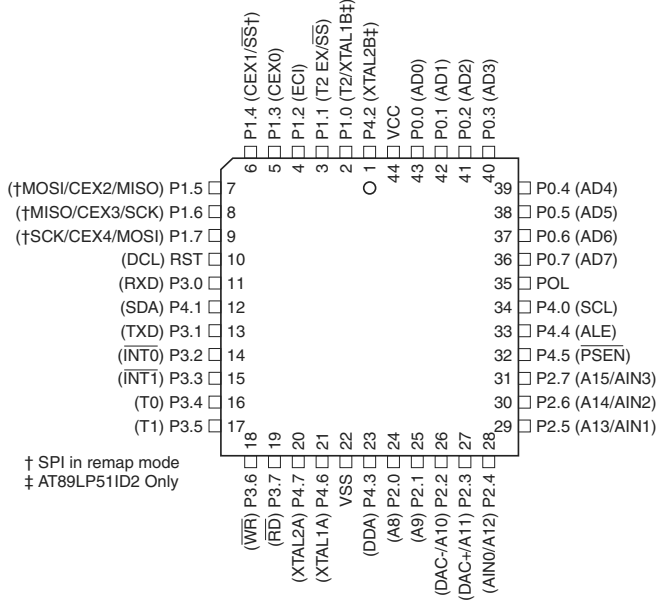
Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.375K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at89lp51rc2-20mu

1. Pin Configurations

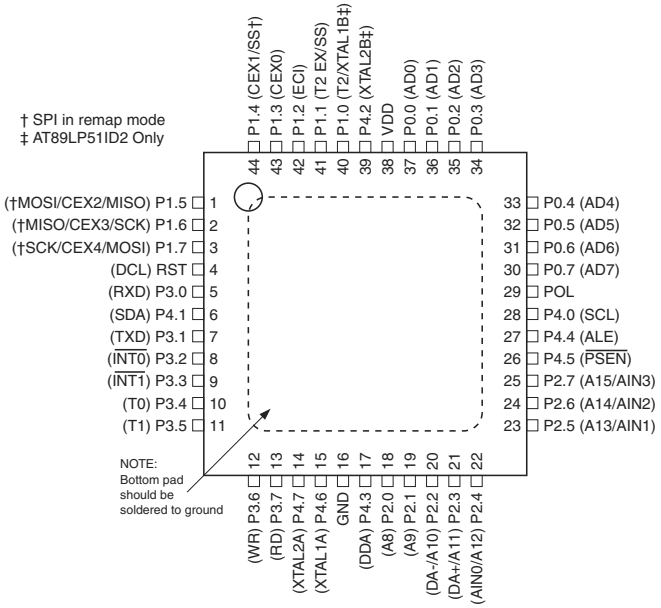
1.1 44-lead VQFP



1.2 44-lead PLCC



1.3 44-pad VQFN/QFN/MLF



1.4 40-pin PDIP

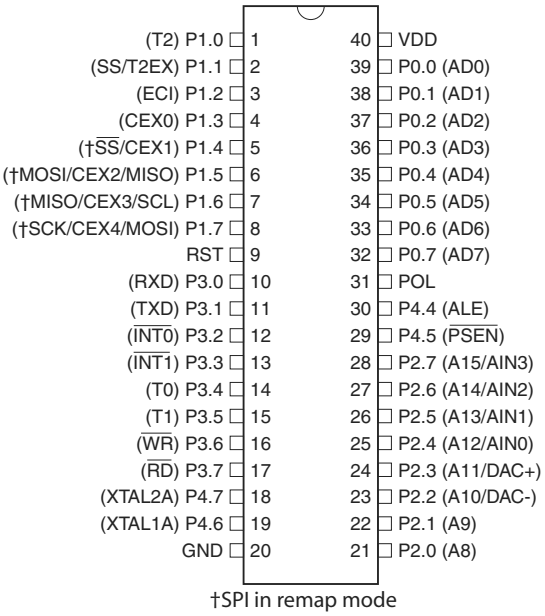


Table 1-1. Atmel AT89LP51RB2/RC2/IC2 Pin Description

Pin Number			Symbol	Type	Description
VQFP VQFN	PLCC	PDIP			
16	22	20	GND	I	Ground
17	23		P4.3	I/O I/O	**P4.3**: User-configurable I/O Port 4bit 3. **DDA**: Bidirectional Debug Data line for the On-Chip Debug Interface when OCD is enabled.
18	24	21	P2.0	I/O O	**P2.0**: User-configurable I/O Port 2 bit 0. **A8**: External memory interface Address bit 8.
19	25	22	P2.1	I/O O	**P2.1**: User-configurable I/O Port 2 bit 1. **A9**: External memory interface Address bit 9.
20	26	23	P2.1	I/O O O	**P2.2**: User-configurable I/O Port 2 bit 2. **DA-**: DAC negative differential output. **A10**: External memory interface Address bit 10.
21	27	24	P2.3	I/O O O	**P2.3**: User-configurable I/O Port 2 bit 3. **DA+-**: DAC positive differential output. **A11**: External memory interface Address bit 11.
22	28	25	P2.4	I/O I O	**P2.4**: User-configurable I/O Port 2 bit 5. **AIN0**: Analog Comparator Input 0. **A12**: External memory interface Address bit 12.
23	29	26	P2.5	I/O I O	**P2.5**: User-configurable I/O Port 2 bit 5. **AIN1**: Analog Comparator Input 1. **A13**: External memory interface Address bit 13.
24	30	27	P2.6	I/O I O	**P2.6**: User-configurable I/O Port 2 bit 6. **AIN2**: Analog Comparator Input 2. **A14**: External memory interface Address bit 14.
25	31	28	P2.7	I/O I O	**P2.7**: User-configurable I/O Port 2 bit 7. **AIN3**: Analog Comparator Input 3. **A15**: External memory interface Address bit 15.
26	32	29	P4.5	I/O O	**P4.5**: User-configurable I/O Port 4 bit 5. **$\overline{\text{PSEN}}$**: External memory interface Program Store Enable (active-low).
27	33	30	P4.4	I/O I/O	**P4.4**: User-configurable I/O Port 4 bit 4. **ALE**: External memory interface Address Latch Enable.
28	34		P4.0	I/O	**P4.0**: User-configurable I/O Port 4 bit 0. **SCL**: TWI Serial Clock line. This line is an output in mater mode and an input in slave mode.
29	35	31	POL	I	**POL**: Reset polarity
30	36	32	P0.7	I/O I/O	**P0.7**: User-configurable I/O Port 0 bit 7. **AD7**: External memory interface Address/Data bit 7.
31	37	33	P0.6	I/O I/O I	**P0.6**: User-configurable I/O Port 0 bit 6. **AD6**: External memory interface Address/Data bit 6. **ADC6**: ADC analog input 6.
32	38	34	P0.5	I/O I/O I	**P0.5**: User-configurable I/O Port 0 bit 5. **AD5**: External memory interface Address/Data bit 5. **ADC5**: ADC analog input 5.
33	39	35	P0.4	I/O I/O I	**P0.4**: User-configurable I/O Port 0 bit 4. **AD4**: External memory interface Address/Data bit 4. **ADC4**: ADC analog input 4.
34	40	36	P0.3	I/O I/O I	**P0.3**: User-configurable I/O Port 0 bit 3. **AD3**: External memory interface Address/Data bit 3. **ADC3**: ADC analog input 3.

Table 1-1. Atmel AT89LP51RB2/RC2/IC2 Pin Description

Pin Number			Symbol	Type	Description
VQFP VQFN	PLCC	PDIP			
35	41	37	P0.2	I/O I/O I	**P0.2**: User-configurable I/O Port 0 bit 2. **AD2**: External memory interface Address/Data bit 2. **ADC2**: ADC analog input 2.
36	42	38	P0.1	I/O I/O I	**P0.1**: User-configurable I/O Port 0 bit 1. **AD1**: External memory interface Address/Data bit 1. **ADC1**: ADC analog input 1.
37	43	39	P0.0	I/O I/O I	**P0.0**: User-configurable I/O Port 0 bit 0. **AD0**: External memory interface Address/Data bit 0. **ADC0**: ADC analog input 0.
38	44	40	VDD	I	Supply Voltage
39	1		P4.2	I/O	**P4.2**: User-configurable I/O Port 4bit 2. **XTAL2B**: Output from low-frequency inverting oscillator amplifier B (AT89LP51IC2 only). It may be used as a port pin if the internal RC oscillator or external clock is selected as the clock source B.
40	2	1	P1.0	I/O I/O	**P1.0**: User-configurable I/O Port 1 bit 0. **T2**: Timer 2 External Input or Clock Output. **XTAL1B**: Input to the low-frequency inverting oscillator amplifier B and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source B.
41	3	2	P1.1	I/O I I	**P1.1**: User-configurable I/O Port 1 bit 1. **T2EX**: Timer 2 External Capture/Reload Input. **$\overline{SS}$**: SPI Slave-Select.
42	4	3	P1.2	I/O	**P1.2**: User-configurable I/O Port 1 bit 2.
43	5	4	P1.3	I/O I/O	**P1.3**: User-configurable I/O Port 1 bit 3. **CEX0**: Capture/Compare external I/O for PCA module 0.
44	6	5	P1.4	I/O I I/O	**P1.4**: User-configurable I/O Port 1 bit 4. **$\overline{SS}$**: SPI Slave-Select (Remap Mode). This pin is an input for In-System Programming **CEX1**: Capture/Compare external I/O for PCA module 1.

2. Overview

The Atmel® AT89LP51RB2/RC2/IC2 is a low-power, high-performance CMOS 8-bit 8051 microcontroller with 64KB of In-System Programmable Flash program memory. The devices are manufactured using Atmel's high-density nonvolatile memory technology and are compatible with the industry-standard 80C51 instruction set.

The AT89LP51RB2/RC2/IC2 is built around an enhanced CPU core that can fetch a single byte from memory every clock cycle. In the classic 8051 architecture, each fetch requires 6 clock cycles, forcing instructions to execute in 12, 24 or 48 clock cycles. In the AT89LP51RB2/RC2/IC2 CPU, standard instructions need only one to four clock cycles providing six to twelve times more throughput than the standard 8051. Seventy percent of instructions need only as many clock cycles as they have bytes to execute, and most of the remaining instructions require only one additional clock. The enhanced CPU core is capable of 20 MIPS throughput whereas the classic 8051 CPU can deliver only 4 MIPS at the same current consumption. Conversely, at the same throughput as the classic 8051, the new CPU core runs at a much lower speed and thereby greatly reducing power consumption and EMI. The AT89LP51RB2/RC2/IC2 also includes a compatibility mode that will enable classic 12 clock per machine cycle operation for true timing compatibility with the Atmel AT89C51RB2/RC2.

The AT89LP51RB2/RC2/IC2 retains all of the standard features of the AT89C51RB2/RC2, including: 64KB of In-System Programmable Flash program memory, 256 bytes of RAM, 1152 bytes of expanded RAM, up to 40 I/O lines, three 16-bit timer/counters, a Programmable Counter Array, a programmable hardware watchdog timer, a keyboard interface, a full-duplex enhanced serial port, a serial peripheral interface (SPI), on-chip crystal oscillator, and a four-level, ten-vector interrupt system. A block diagram is shown in Figure 2-1.

In addition, the Atmel® AT89LP51RB2/RC2/IC2 provides a Two-Wire Interface (TWI) for up to 400KB/s serial transfer; a 10-bit, 8-channel Analog-to-Digital Converter (ADC) with temperature sensor and digital-to-analog (DAC) mode; two analog comparators; and an 8MHz internal oscillator.

Some standard features on the AT89LP51RB2/RC2/IC2 are enhanced with new modes or operations. Mode 0 of Timer 0 or Timer 1 acts as a variable 9–16 bit timer/counter and Mode 1 acts as a 16-bit auto-reload timer/counter. In addition, each timer/counter may independently drive an 8-bit precision pulse width modulation output. Mode 0 (synchronous mode) of the serial port allows flexibility in the phase/polarity relationship between clock and data.

The I/O ports of the AT89LP51RB2/RC2/IC2 can be independently configured in one of four operating modes. In quasi-bidirectional mode, the ports operate as in the classic 8051. In input-only mode, the ports are tristated. Push-pull output mode provides full CMOS drivers and open-drain mode provides just a pull-down. Unlike other 8051s, this allows Port 0 to operate with on-chip pull-ups if desired.

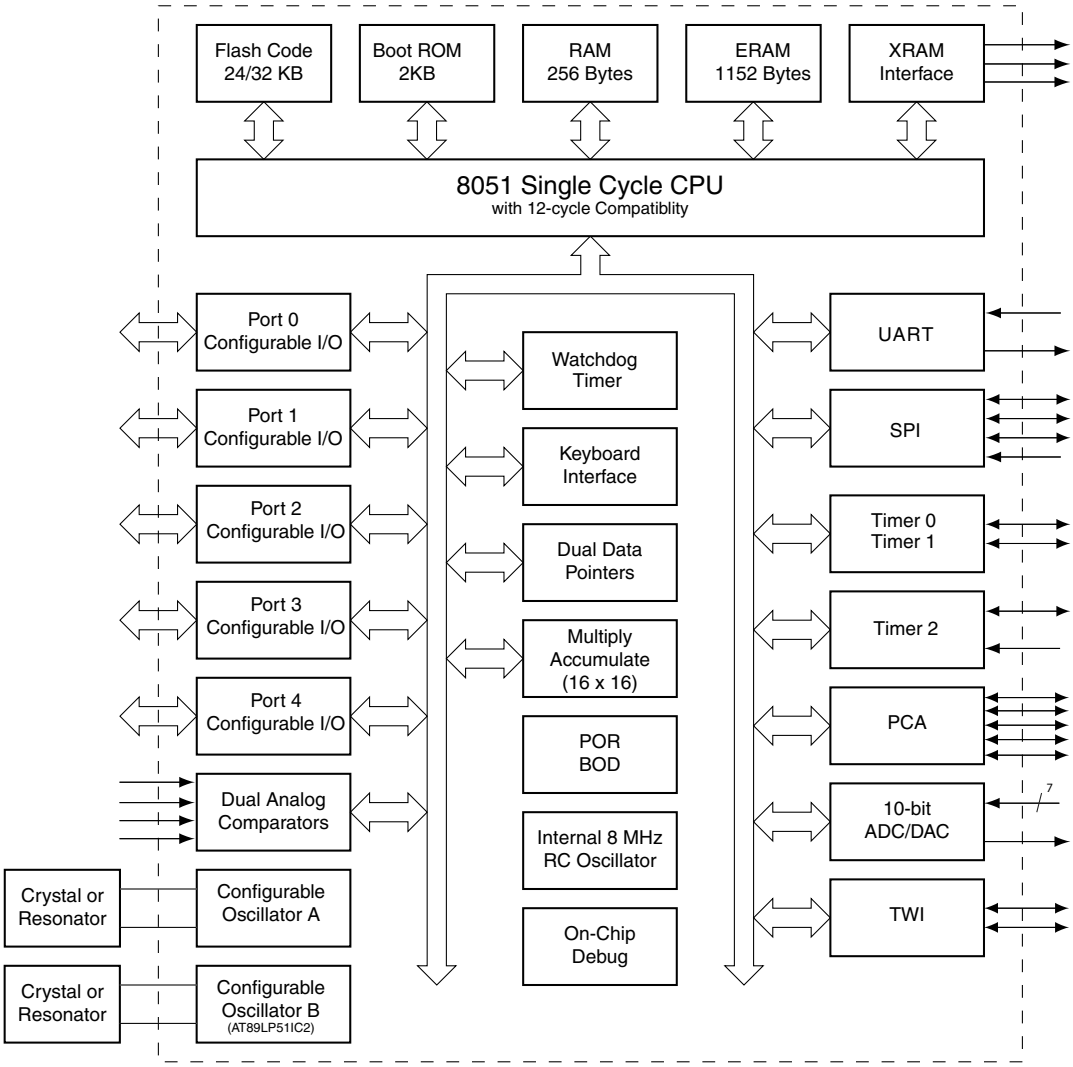
The AT89LP51RB2/RC2/IC2 includes an On-Chip Debug (OCD) interface that allows read-modify-write capabilities of the system state and program flow control, and programming of the internal memories. The on-chip Flash may also be programmed through the UART-based bootloader or the SPI-based In-System programming interface (ISP).

The TWI and OCD features are not available on the PDIP package. The AT89LP51IC2 is also not available in PDIP.

The features of the AT89LP51RB2/RC2/IC2 make it a powerful choice for applications that need pulse width modulation, high speed I/O, and counting capabilities such as alarms, motor control, corded phones, and smart card readers.

2.1 Block Diagram

Figure 2-1. Atmel AT89LP51RB2/RC2/IC2 Block Diagram



2.2 System Configuration

The AT89LP51RB2/RC2/IC2 supports several system configuration options. Nonvolatile options are set through user fuses that must be programmed through the flash programming interface. Volatile options are controlled by software through individual bits of special function registers (SFRs). The AT89LP51RB2/RC2/IC2 must be properly configured before correct operation can occur.

2.2.1 Fuse Options

Table 2-1 lists the fusible options for the AT89LP51RB2/RC2/IC2. These options maintain their state even when the device is powered off. Some may be changed through the FLash API but others can only be changed with an external device programmer. For more information, see datasheet.

Table 2-1. User Configuration Fuses

Fuse Name	Description
Clock Source A	Selects between the High Speed Crystal Oscillator, Low Power Crystal Oscillator, External Clock on XTAL1A or Internal RC Oscillator for the source of the system clock when oscillator A is selected.
Clock Source B	Selects between the 32 kHzCrystal Oscillator, External Clock on XTAL1B or Internal RC Oscillator for the source of the system clock when oscillator B is selected (AT89LP51IC2 Only).
Oscillator Select	Selects whether oscillator A or B is enabled to boot the device. (AT89LP51IC2 Only)
X2 Mode	Selects the default state of whether the clock source is divided by two (X1) or not (X2) to generate the system clock.
Start-up Time	Selects time-out delay for the POR/BOD/PWD wake-up period.
Compatibility Mode	Configures the CPU in 12-clock compatibility or single-cycle fast execution mode.
XRAM Configuration	Configures if access to on-chip memories that are mapped to the external data memory address space is enabled/disabled by default.
Bootloader Jump Bit	Enables or disables the on-ship bootloader.
On-Chip Debug Enable	Enables or disables On-Chip Debug. OCD must be enabled prior to using an in-circuit debugger with the device.
In-System Programming Enable	Enables or disables In-System Programming.
User Signature Programming Enable	Enables or disables programming of User Signature array.
Default Port State	Configures the default port state as input-only mode (tristated) or quasi-bidirectional mode (weakly pulled high).
Low Power Mode	Enables or disables power reduction features for lower system frequencies.

2.2.2 Software Options

Table 2-2 lists some important software configuration bits that affect operation at the system level. These can be changed by the application software but are set to their default values upon any reset. Most peripherals also have multiple configuration bits that are not listed here.

Table 2-2. Important Software Configuration Bits

Bit(s)	SFR Location	Description
PxM0.y PxM1.y	P0M0, P0M1, P1M0, P1M1, P2M0, P2M1, P3M0, P3M1, P4M0, P4M1	Configures the I/O mode of Port x Pin y to be one of input-only, quasi-bidirectional, push-pull output or open-drain. The default state is controlled by the Default Port State fuse above
CKRL	CKRL	Selects the division ratio between the oscillator and the system clock
TPS_{3-0}	CLKREG.7-4	Selects the division ratio between the system clock and the timers
ALES	AUXR.0	Enables/disables toggling of ALE
EXRAM	AUXR.1	Enables/disables access to on-chip memories that are mapped to the external data memory address space
WS_{1-0}	AUXR.6-5	Selects the number of wait states when accessing external data memory
XSTK	AUXR1.4	Configures the hardware stack to be in RAM or extra RAM
ENBOOT	AUXR1.5	Enables/disables access to the on-chip Flash API

2.3 Comparison to the Atmel AT89C51RB2/RC2/IC2

The Atmel® AT89LP51RB2/RC2/IC2 is part of a family of devices with enhanced features that are fully binary compatible with the 8051 instruction set. The AT89LP51RB2/RC2/IC2 has two modes of operations, Compatibility mode and Fast mode. In Compatibility mode the instruction timing, peripheral behavior, SFR addresses, bit assignments and pin functions are identical to the existing Atmel AT89C51RB2/RC2/IC2 product. Additional enhancements are transparent to the user and can be used if desired. Fast mode allows greater performance, but with some differences in behavior. The major enhancements from the AT89C51RB2/RC2/IC2 are outlined in the following paragraphs and may be useful to users migrating to the AT89LP51RB2/RC2/IC2 from older devices. A summary of the differences between Compatibility and Fast modes is given in Table 2-3 on page 11. See also the Application note “Migrating from AT89C51RB2/RC2/IC2 to AT89LP51RB2/RC2/IC2.”

2.3.1 Instruction Execution

In Compatibility mode the Atmel® AT89LP51RB2/RC2/IC2 CPU uses the six-state machine cycle of the standard 8051 where instruction bytes are fetched every three system clock cycles. Execution times in this mode are identical to the Atmel AT89C51RB2/RC2/IC2. For greater performance the user can enable Fast mode by disabling the Compatibility fuse. In Fast mode the CPU fetches one code byte from memory every clock cycle instead of every three clock cycles. This greatly increases the throughput of the CPU. Each standard instruction executes in only one to four clock cycles. See datasheet for more details. Any software delay loops or instruction-based timing operations may need to be retuned to achieve the desired results in Fast mode.

2.3.2 System Clock

The system clock source is not limited to a crystal or external clock. The system clock source is selectable between the crystal oscillator, an externally driven clock and an internal 8.0MHz RC oscillator for AT89LP51RB2/RC2 and clock source A of AT89LP51IC2. Clock source B of AT89LP51IC2 is not limited to a 32 kHz crystal. The clock source B is selectable between the 32 kHz crystal oscillator, an externally driven clock and an internal 8.0MHz RC oscillator. Unlike AT89C51IC2, the X2 and CKRL features will also affect the OSCB source.

By default in Compatibility mode the system clock frequency is divided by 2 from the externally supplied XTAL1 frequency for compatibility with standard 8051s (12 clocks per machine cycle). The System Clock Divider can scale the system clock versus the oscillator source. The divide-by-2 can be disabled to operate in X2 mode (6 clocks per machine cycle) or the clock may be further divided to reduce the operating frequency. In Fast mode the clock divider defaults to divide by 1.

2.3.3 Reset

The RST pin of the AT89LP51RB2/RC2/IC2 has selectable polarity using the POL pin (formerly $\overline{EA}$). When POL is high the RST pin is active high with a pull-down resistor and when POL is low the RST pin is active low with a pull-up resistor. For existing AT89C51RB2/RC2/IC2 sockets where $\overline{EA}$ is tied to VDD, replacing AT89C51RB2/RC2 with AT89LP51RB2/RC2/IC2 will maintain the active high reset. Note that forcing external execution by tying $\overline{EA}$ low is not supported.

The AT89LP51RB2/RC2/IC2 includes an on-chip Power-On Reset and Brown-out Detector circuit that ensures that the device is reset from system power up. In most cases a RC startup circuit is not required on the RST pin, reducing system cost, and the RST pin may be left unconnected if a board-level reset is not present.

2.3.9 Security

The AT89LP51RB2/RC2/IC2 does not support the external access pin ($\overline{EA}$). Therefore it is not possible to execute from external program memory in address range 0000H–1FFFH. When the third Lockbit is enabled (Lock Mode 4) external program execution is disabled for all addresses above 1FFFH. This differs from AT89C51RB2/RC2/IC2 where Lock Mode 4 prevents $\overline{EA}$ from being sampled low, but may still allow external execution at addresses outside the 8K internal space.

2.3.10 Programming

The AT89LP51RB2/RC2/IC2 supports a richer command set for In-System Programming (ISP). Existing AT89C51RB2/RC2 programmers should be able to program the AT89LP51RB2/RC2/IC2 in byte mode. In page mode the AT89LP51RB2/RC2/IC2 only supports programming of a half-page of 64 bytes and therefore requires an extra address byte as compared to AT89C51RB2/RC2. Furthermore the device signature is located at addresses 0000H, 0001H and 0003H instead of 0000H, 0100H and 0200H.

Table 2-3. Compatibility Mode versus Fast Mode Summary

Feature	Compatibility	Fast
Instruction Fetch in System Clocks	3	1
Instruction Execution Time in System Clocks	6, 12, 18 or 24	1, 2, 3, 4 or 5
Default System Clock Divisor	2	1
Default Timer Prescaler Divisor	6	1
Pin Sampling Rate ($\overline{INT0}$, $\overline{INT1}$, T0, T1, T2, T2EX)	Prescaler Rate	System Clock
Minimum RST input pulse in System Clocks	12	2

3. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 3-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

Table 3-1. Atmel AT89LP51RB2/RC2/IC2 SFR Map and Reset Values

	8	9	A	B	C	D	E	F	
0F8H		CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		0FFH
0F0H	B 0000 0000		RL0 0000 0000	RL1 0000 0000	RH0 0000 0000	RH1 0000 0000	PAGE 0000 0000	BX 0000 0000	0F7H
0E8H		CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000	SPX xxxx x000	0EFH
0E0H	ACC 0000 0000	AX 0000 0000	DSPR 0000 0000	FIRD 0000 0000	MACL 0000 0000	MACH 0000 0000	P0M0 (2)	P0M1 0000 0000	0E7H
0D8H	CCON 00x0 0000	CMOD 00xx x000	CCAPM0 x000 0000	CCAPM1 x000 0000	CCAPM2 x000 0000	CCAPM3 x000 0000	CCAPM4 x000 0000		0DFH
0D0H	PSW 0000 0000	FCON xxxx 0000			DPLB 0000 0000	DPHB 0000 0000	P1M0 (2)	P1M1 0000 0000	0D7H
0C8H	T2CON 0000 0000	T2MOD 0000 0000	RCAP2L 0000 000	RCAP2H 0000 0000	TL2 0000 000	TH2 0000 0000	P2M0 (2)	P2M1 0000 0000	0CFH
0C0H	P4 1111 1111			SPCON 0001 0100	SPSTA 0000 0000	SPDAT xxxx xxxx	P3M0 (2)	P3M1 0000 0000	0C7H
0B8H	IPL0 xx00 0000	SADEN 0000 0000				AREF 0000 0000	P4M0 (2)	P4M1 0000 0000	0BFH
0B0H	P3 1111 1111	IEN1 xxxx 0000	IPL1 xxxx 0000	IPH1 xxxx 0000				IPH0 xx00 0000	0B7H
0A8H	IEN0 0x00 0000	SADDR 0000 0000		ACSRB 0000 0000	DADL 0000 0000	DADH 0000 0000	CLKREG 0101 xxxx	CKCON1 xxxx xxx0	0AFH
0A0H	P2 1111 1111	DPCF 0000 0000	AUXR1 0000 00x0	ACSRA 0000 0000	DADC 0000 0000	DADI 0000 0000	WDTRST (write-only)	WDTPRG 0000 0xx0	0A7H
98H	SCON 0000 0000	SBUF xxxx xxxx	BRL 0000 0000	BDRCON xxx0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000	KBMOD 0000 0000	9FH
90H	P1 1111 1111	TCONB 0010 0100	BMSEL xxxx xxx0	SSCON 0000 0000	SSCS 1111 1000	SSDAT 1111 1111	SSADR 1111 1110	CKRL 1111 1111	97H
88H	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 0000 0000	CKCON0 0000 0000	8FH
80H	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000		CKSEL xxxx xxx0	OSCCON xxxx x001	PCON 000x 0000	87H
	0	1	2	3	4	5	6	7	

Notes: 1. All SFRs in the left-most column are bit-addressable.

2. Reset value is 1111 1111B when Tristate-Port Fuse is enabled and 0000 0000B when disabled.

3. Reset value is 0101 0010B when Compatibility mode is enabled and 0000 0000B when disabled.

Table 3-2. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer								
SPX	EFh	Extended Stack Pointer	–	–	–	–	SP11	SP10	SP9	SP8
DPL	82h	Data Pointer Low Byte								
DPH	83h	Data Pointer High Byte								
DPLB	D4h	Alternate Data Pointer Low Byte								
DPHB	D5h	Alternate Data Pointer High Byte								
PAGE	F6h	ERAM Page Register	–	–	–	–				

Table 3-3. Digital Signal Processing SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
AX	E1h	Extended Accumulator								
BX	F7h	Extended B Register								
DSPR	E2h	DSP Control Register	MRW1	MRW0	SMLB	SMLA	CBE1	CBE0	MVCD	DPRB
FIRD	E3h	FIFO Depth								
MACL	E4h	MAC Low Byte								
MACH	E5h	MAC High Byte								

Table 3-4. System Management SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1	SMOD0	PWDEX	POF	GF1	GF0	PD	IDL
AUXR	8Eh	Auxiliary Register 0	DPU	WS1	WS0/M0	XRS2	XRS1	XRS0	EXTRAM	AO
AUXR1	A2h	Auxiliary Register 1	–	–	ENBOOT	XSTK	GF3	0	–	DPS
DPCR	A3h	Datapointer Config Register	DPU1	DPU0	DPD1	DPD0	–	–	–	–
CKRL	97h	Clock Reload Register								
CKCKON0	8Fh	Clock Control Register 0	TWIX2	WDTX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2
CKCKON1	AFh	Clock Control Register 1	–	–	–	–	–	–	–	SPIX2
CKSEL[1]	85h	Clock Selection Register	–	–	–	–	–	–	–	CKS
CLKREG	AEh	Clock Register	TPS3	TPS2	TPS1	TPS0	–	–	–	–
OSCCON[1]	85h	Oscillator Control Register	–	–	–	–	–	SCLKT0	OscBEn	OscAEn

Note: 1. Present on AT89LP51IC2 Only

Table 3-5. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	–	–	EADC	ECMP	–	ESPI	ETWI	EKB
IPH0	B7h	Interrupt Priority Control High 0	IP1D	PPCH	PT2H	PHS	PT1H	PX1H	PT0H	PX0H
IPL0	B8h	Interrupt Priority Control Low 0	IP0D	PPCL	PT2L	PLS	PT1L	PX1L	PT0L	PX0L
IPH1	B3h	Interrupt Priority Control High 1	IP3D	–	PADL	PCMPL	–	SPIH	PTWL	PKBH
IPL1	B2h	Interrupt Priority Control Low 1	IP2D	–	PADH	PCMPH	–	SPIL	PTWH	PKBL

Table 3-6. Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	8-bit Port 0								
P1	90h	8-bit Port 1								
P2	A0h	8-bit Port 2								
P3	B0h	8-bit Port 3								
P4	C0h	8-bit Port 4								
P0M0	E6h	Port 0 Mode 0								
P0M1	E7h	Port 0 Mode 1								
P1M0	D6h	Port 1 Mode 0								
P1M1	D7h	Port 1 Mode 1								
P2M0	CEh	Port 2 Mode 0								
P2M1	CFh	Port 2 Mode 1								
P3M0	C6h	Port 3 Mode 0								
P3M1	C7h	Port 3 Mode 1								
P4M0	BEh	Port 4 Mode 0								
P4M1	BFh	Port 4 Mode 1								

Table 3-7. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								
BDRCON	9Bh	Baud Rate Control	–	–	–	BRR	TBCK	RBCK	SPD	SRC
BRL	9Ah	Baud Rate Reload								

Table 3-8. Timer SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TCON	88h	Timer/Counter 0 and 1 Control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/$\overline{T1}$	M11	M01	GATE0	C/$\overline{T0}$	M10	M00
TCONB	91h	Timer/Counter 0 and 1 Mode B								
TL0	8Ah	Timer/Counter 0 Low Byte								
TH0	8Ch	Timer/Counter 0 High Byte								
TL1	8Bh	Timer/Counter 1 Low Byte								
TH1	8Dh	Timer/Counter 1 High Byte								
RL0	F2h	Timer/Counter 0 Reload Low								
RH0	F3h	Timer/Counter 0 Reload High								
RTL1	F4h	Timer/Counter 1 Reload Low								
RH1	F5h	Timer/Counter 1 Reload High								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program						WTO2	WTO1	WTO0
T2CON	C8h	Timer/Counter 2 control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9h	Timer/Counter 2 Mode	–	–	–	–	–	–	T2OE	DCEN
RCAP2H	CBh	Timer/Counter 2 Reload/Capture High Byte								
RCAP2L	CAh	Timer/Counter 2 Reload/Capture Low Byte								
TH2	CDh	Timer/Counter 2 High Byte								
TL2	CCh	Timer/Counter 2 Low Byte								

Table 3-9. SPI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SPCON	C3h	SPI Control	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
SPSTA	C4h	SPI Status	SPIF	WCOL	SSERR	MODF				
SPDAT	C5h	SPI Data	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Table 3-10. TWI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SSCON	93h	Synchronous Serial Control	SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
SSCS	94h	Synchronous Serial Status	SSC4	SSC3	SSC2	SSC1	SSC0	0	0	0
SSDAT	95h	Synchronous Serial Data								
SSADR	96h	Synchronous Serial Address	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSGC

Table 3-11. Keyboard Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBLS	9Ch	Keyboard Level Selector	KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS1	KBLS0
KBE	9Dh	Keyboard Input Enable	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0
KBF	9Eh	Keyboard Flag Register	KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0
KBMOD	9Fh	Keyboard Mode Register	KBM7	KBM6	KBM5	KBM4	KBM3	KBM2	KBM1	KBM0

Table 3-12. Flash Memory SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
BMSEL	92h	Bank Mode Select Register	–	–	–	–	–	–	–	FBS
FCON	D2h	Flash Control Register	FPSL3	FPSL2	FPSL1	FPSL0	FPS	FMOD1	FMOD0	FBUSY

Table 3-13. Analog Comparator SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACSRA	A3h	Comparator A Control Register								
ACSRB	ABh	Comparator B Control Register								
AREF	BDh	Comparator Reference Register								

Table 3-14. ADC Controller SFRs

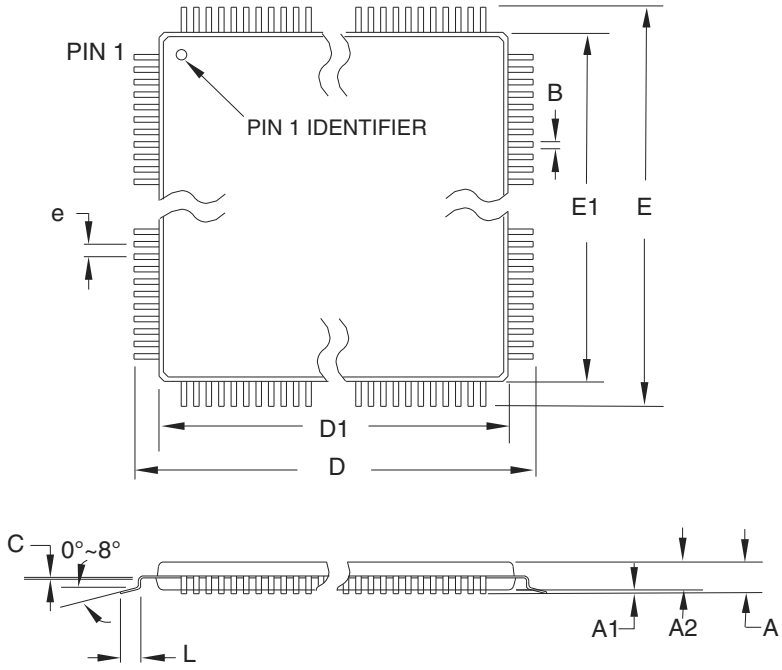
Mnemonic	Add	Name	7	6	5	4	3	2	1	0
DADC	A4h	DAC/ADC Control Register								
DADI	A5h	DAC/ADC Input Register								
DADL	ACh	DAC/ADC Data Low Register								
DADH	ADh	DAC/ADC Data High Register								

Table 3-15. PCA SFRs

Mnemo-nic	Add	Name	7	6	5	4	3	2	1	0
CCON	D8h	PCA Timer/Counter Control	CF	CR		CCF4	CCF3	CCF2	CCF1	CCF0
CMOD	D9h	PCA Timer/Counter Mode	CIDL	WDTE				CPS1	CPS0	ECF
CL	E9h	PCA Timer/Counter Low Byte								
CH	F9h	PCA Timer/Counter High Byte								
CCAPM0	DAh	PCA Timer/Counter Mode 0		ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
CCAPM1	DBh	PCA Timer/Counter Mode 1		ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
CCAPM2	DCh	PCA Timer/Counter Mode 2		ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
CCAPM3	DDh	PCA Timer/Counter Mode 3		ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3

5. Packaging Information

5.1 44AA – VQFP/LQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

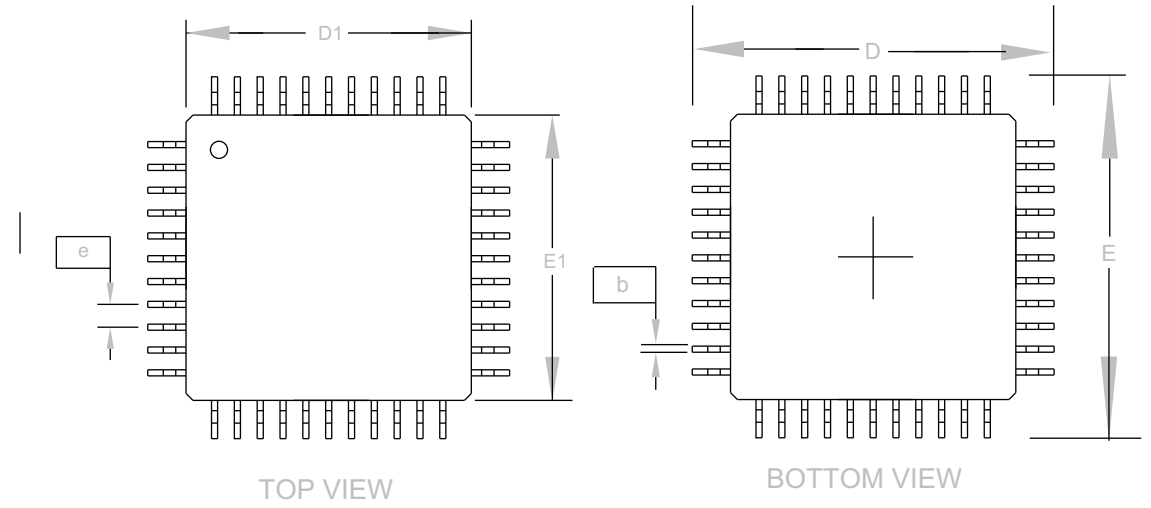
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	0.05	–	0.15	
A2	0.95	1.40	1.05	
D	11.9	12.00	12.10	
D1	9.90	10.00	10.10	Note 2
E	11.9	12.00	12.10	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

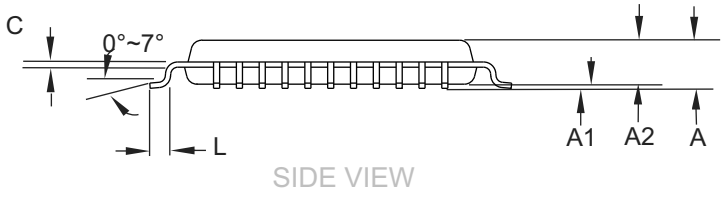
Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.102 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44AA,** 44-lead, 10 x 10 mm Body Size, 1.4 mm Body Thickness, 0.8 mm Lead Pitch, Low Profile Plastic Quad Flat Package (VQFP)	44AA	B

5.2 44A – TQFP



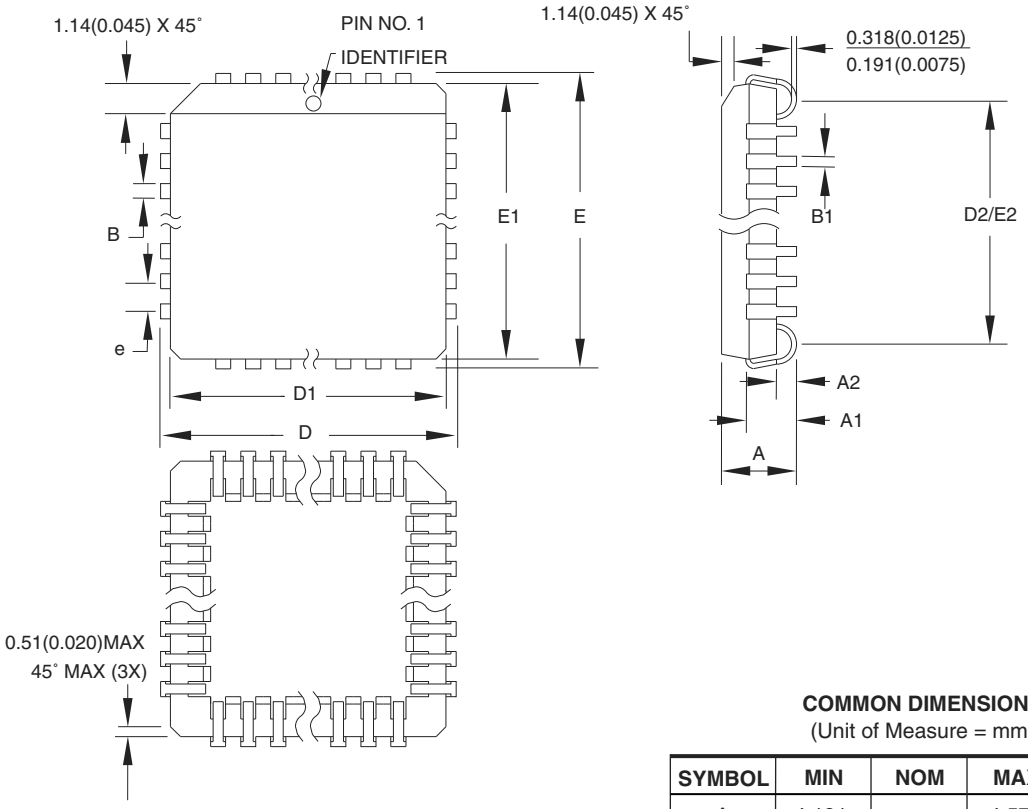


COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

5.3 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

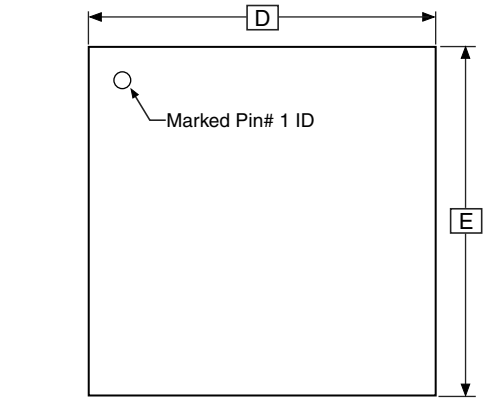
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

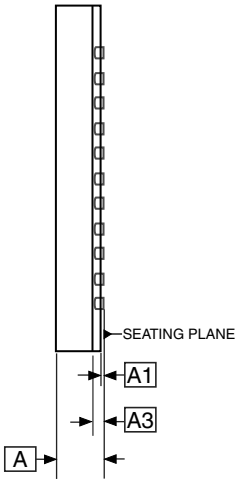
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

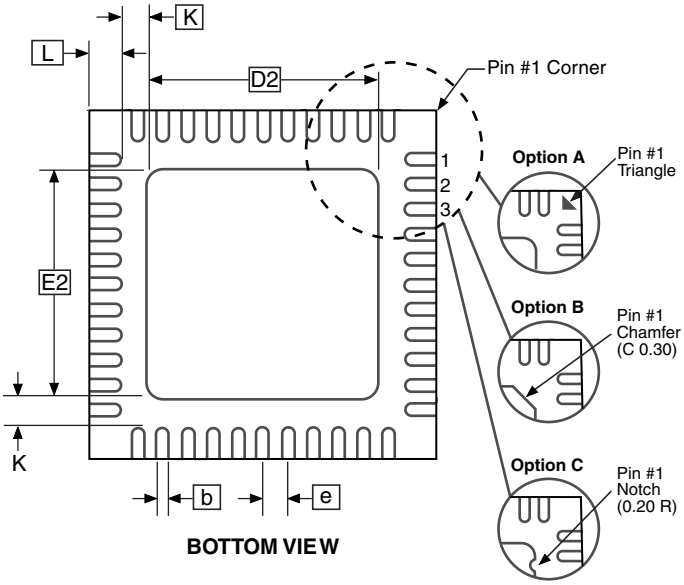
5.4 44M1 – VQFN/MLF



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

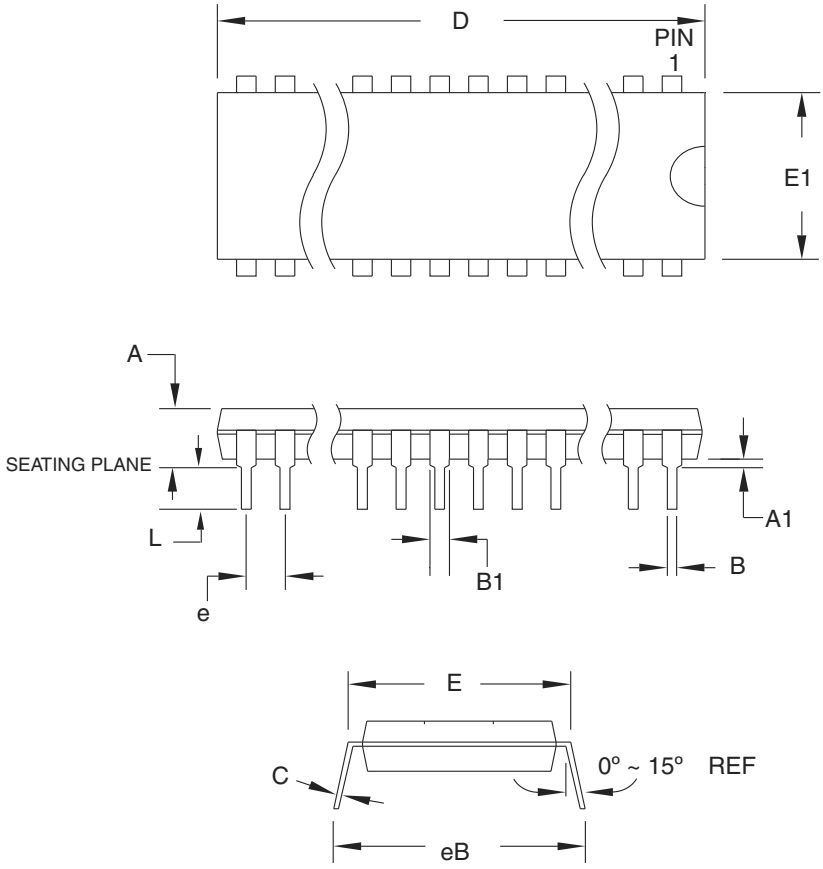
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

9/26/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	44M1, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)	ZWS	44M1	H

5.5 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

6. Revision History

Revision No.	History
Revision A – October 2011	• Initial Release

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3722AS–MICRO–10/11