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#### Details

|                            |   |
|----------------------------|---|
| Product Status             | Active  |
| Core Processor             | 8051  |
| Core Size                  | 8-Bit   |
| Speed                      | 20MHz   |
| Connectivity               | EBI/EMI, I <sup>2</sup> C, SPI, UART/USART  |
| Peripherals                | Brown-out Detect/Reset, POR, PWM, WDT   |
| Number of I/O              | 37  |
| Program Memory Size        | 32KB (32K x 8)  |
| Program Memory Type        | FLASH   |
| EEPROM Size                | -   |
| RAM Size                   | 1.375K x 8  |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.5V   |
| Data Converters            | A/D 7x10b   |
| Oscillator Type            | Internal  |
| Operating Temperature      | -40°C ~ 85°C (TA)   |
| Mounting Type              | Through Hole  |
| Package / Case             | 40-DIP (0.600", 15.24mm)  |
| Supplier Device Package    | 40-PDIP   |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/atmel/at89lp51rc2-20pu">https://www.e-xfl.com/product-detail/atmel/at89lp51rc2-20pu</a> |



**Table 1-1. Atmel AT89LP51RB2/RC2/IC2 Pin Description**

| Pin Number   |      |      | Symbol | Type            | Description  |
|--------------|------|------|--------|-----------------|--|
| VQFP<br>VQFN | PLCC | PDIP |        |                 |  |
| 16           | 22   | 20   | GND    | I               | Ground   |
| 17           | 23   |      | P4.3   | I/O<br>I/O      | <b>P4.3:</b> User-configurable I/O Port 4 bit 3.<br><b>DDA:</b> Bidirectional Debug Data line for the On-Chip Debug Interface when OCD is enabled.         |
| 18           | 24   | 21   | P2.0   | I/O<br>O        | <b>P2.0:</b> User-configurable I/O Port 2 bit 0.<br><b>A8:</b> External memory interface Address bit 8.  |
| 19           | 25   | 22   | P2.1   | I/O<br>O        | <b>P2.1:</b> User-configurable I/O Port 2 bit 1.<br><b>A9:</b> External memory interface Address bit 9.  |
| 20           | 26   | 23   | P2.1   | I/O<br>O<br>O   | <b>P2.2:</b> User-configurable I/O Port 2 bit 2.<br><b>DA-:</b> DAC negative differential output.<br><b>A10:</b> External memory interface Address bit 10. |
| 21           | 27   | 24   | P2.3   | I/O<br>O<br>O   | <b>P2.3:</b> User-configurable I/O Port 2 bit 3.<br><b>DA+:</b> DAC positive differential output.<br><b>A11:</b> External memory interface Address bit 11. |
| 22           | 28   | 25   | P2.4   | I/O<br>I<br>O   | <b>P2.4:</b> User-configurable I/O Port 2 bit 5.<br><b>AIN0:</b> Analog Comparator Input 0.<br><b>A12:</b> External memory interface Address bit 12.       |
| 23           | 29   | 26   | P2.5   | I/O<br>I<br>O   | <b>P2.5:</b> User-configurable I/O Port 2 bit 5.<br><b>AIN1:</b> Analog Comparator Input 1.<br><b>A13:</b> External memory interface Address bit 13.       |
| 24           | 30   | 27   | P2.6   | I/O<br>I<br>O   | <b>P2.6:</b> User-configurable I/O Port 2 bit 6.<br><b>AIN2:</b> Analog Comparator Input 2.<br><b>A14:</b> External memory interface Address bit 14.       |
| 25           | 31   | 28   | P2.7   | I/O<br>I<br>O   | <b>P2.7:</b> User-configurable I/O Port 2 bit 7.<br><b>AIN3:</b> Analog Comparator Input 3.<br><b>A15:</b> External memory interface Address bit 15.       |
| 26           | 32   | 29   | P4.5   | I/O<br>O        | <b>P4.5:</b> User-configurable I/O Port 4 bit 5.<br><b>PSEN:</b> External memory interface Program Store Enable (active-low).                              |
| 27           | 33   | 30   | P4.4   | I/O<br>I/O      | <b>P4.4:</b> User-configurable I/O Port 4 bit 4.<br><b>ALE:</b> External memory interface Address Latch Enable.  |
| 28           | 34   |      | P4.0   | I/O             | <b>P4.0:</b> User-configurable I/O Port 4 bit 0.<br><b>SCL:</b> TWI Serial Clock line. This line is an output in master mode and an input in slave mode.   |
| 29           | 35   | 31   | POL    | I               | <b>POL:</b> Reset polarity   |
| 30           | 36   | 32   | P0.7   | I/O<br>I/O      | <b>P0.7:</b> User-configurable I/O Port 0 bit 7.<br><b>AD7:</b> External memory interface Address/Data bit 7.  |
| 31           | 37   | 33   | P0.6   | I/O<br>I/O<br>I | <b>P0.6:</b> User-configurable I/O Port 0 bit 6.<br><b>AD6:</b> External memory interface Address/Data bit 6.<br><b>ADC6:</b> ADC analog input 6.          |
| 32           | 38   | 34   | P0.5   | I/O<br>I/O<br>I | <b>P0.5:</b> User-configurable I/O Port 0 bit 5.<br><b>AD5:</b> External memory interface Address/Data bit 5.<br><b>ADC5:</b> ADC analog input 5.          |
| 33           | 39   | 35   | P0.4   | I/O<br>I/O<br>I | <b>P0.4:</b> User-configurable I/O Port 0 bit 4.<br><b>AD4:</b> External memory interface Address/Data bit 4.<br><b>ADC4:</b> ADC analog input 4.          |
| 34           | 40   | 36   | P0.3   | I/O<br>I/O<br>I | <b>P0.3:</b> User-configurable I/O Port 0 bit 3.<br><b>AD3:</b> External memory interface Address/Data bit 3.<br><b>ADC3:</b> ADC analog input 3.          |

**Table 1-1.** Atmel AT89LP51RB2/RC2/IC2 Pin Description

| Pin Number   |      |      | Symbol | Type            | Description  |
|--------------|------|------|--------|-----------------|--|
| VQFP<br>VQFN | PLCC | PDIP |        |                 |  |
| 35           | 41   | 37   | P0.2   | I/O<br>I/O<br>I | <b>P0.2:</b> User-configurable I/O Port 0 bit 2.<br><b>AD2:</b> External memory interface Address/Data bit 2.<br><b>ADC2:</b> ADC analog input 2.  |
| 36           | 42   | 38   | P0.1   | I/O<br>I/O<br>I | <b>P0.1:</b> User-configurable I/O Port 0 bit 1.<br><b>AD1:</b> External memory interface Address/Data bit 1.<br><b>ADC1:</b> ADC analog input 1.  |
| 37           | 43   | 39   | P0.0   | I/O<br>I/O<br>I | <b>P0.0:</b> User-configurable I/O Port 0 bit 0.<br><b>AD0:</b> External memory interface Address/Data bit 0.<br><b>ADC0:</b> ADC analog input 0.  |
| 38           | 44   | 40   | VDD    | I               | Supply Voltage   |
| 39           | 1    |      | P4.2   | I/O             | <b>P4.2:</b> User-configurable I/O Port 4bit 2.<br><b>XTAL2B:</b> Output from low-frequency inverting oscillator amplifier B (AT89LP51IC2 only). It may be used as a port pin if the internal RC oscillator or external clock is selected as the clock source B.   |
| 40           | 2    | 1    | P1.0   | I/O<br>I/O      | <b>P1.0:</b> User-configurable I/O Port 1 bit 0.<br><b>T2:</b> Timer 2 External Input or Clock Output.<br><b>XTAL1B:</b> Input to the low-frequency inverting oscillator amplifier B and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source B. |
| 41           | 3    | 2    | P1.1   | I/O<br>I<br>I   | <b>P1.1:</b> User-configurable I/O Port 1 bit 1.<br><b>T2EX:</b> Timer 2 External Capture/Reload Input.<br><b>SS:</b> SPI Slave-Select.  |
| 42           | 4    | 3    | P1.2   | I/O             | <b>P1.2:</b> User-configurable I/O Port 1 bit 2.   |
| 43           | 5    | 4    | P1.3   | I/O<br>I/O      | <b>P1.3:</b> User-configurable I/O Port 1 bit 3.<br><b>CEX0:</b> Capture/Compare external I/O for PCA module 0.  |
| 44           | 6    | 5    | P1.4   | I/O<br>I<br>I/O | <b>P1.4:</b> User-configurable I/O Port 1 bit 4.<br><b>SS:</b> SPI Slave-Select (Remap Mode). This pin is an input for In-System Programming<br><b>CEX1:</b> Capture/Compare external I/O for PCA module 1.  |

## 2. Overview

The Atmel® AT89LP51RB2/RC2/IC2 is a low-power, high-performance CMOS 8-bit 8051 micro-controller with 64KB of In-System Programmable Flash program memory. The devices are manufactured using Atmel's high-density nonvolatile memory technology and are compatible with the industry-standard 80C51 instruction set.

The AT89LP51RB2/RC2/IC2 is built around an enhanced CPU core that can fetch a single byte from memory every clock cycle. In the classic 8051 architecture, each fetch requires 6 clock cycles, forcing instructions to execute in 12, 24 or 48 clock cycles. In the AT89LP51RB2/RC2/IC2 CPU, standard instructions need only one to four clock cycles providing six to twelve times more throughput than the standard 8051. Seventy percent of instructions need only as many clock cycles as they have bytes to execute, and most of the remaining instructions require only one additional clock. The enhanced CPU core is capable of 20 MIPS throughput whereas the classic 8051 CPU can deliver only 4 MIPS at the same current consumption. Conversely, at the same throughput as the classic 8051, the new CPU core runs at a much lower speed and thereby greatly reducing power consumption and EMI. The AT89LP51RB2/RC2/IC2 also includes a compatibility mode that will enable classic 12 clock per machine cycle operation for true timing compatibility with the Atmel AT89C51RB2/RC2.



The AT89LP51RB2/RC2/IC2 retains all of the standard features of the AT89C51RB2/RC2, including: 64KB of In-System Programmable Flash program memory, 256 bytes of RAM, 1152 bytes of expanded RAM, up to 40 I/O lines, three 16-bit timer/counters, a Programmable Counter Array, a programmable hardware watchdog timer, a keyboard interface, a full-duplex enhanced serial port, a serial peripheral interface (SPI), on-chip crystal oscillator, and a four-level, ten-vector interrupt system. A block diagram is shown in Figure 2-1.

In addition, the Atmel® AT89LP51RB2/RC2/IC2 provides a Two-Wire Interface (TWI) for up to 400KB/s serial transfer; a 10-bit, 8-channel Analog-to-Digital Converter (ADC) with temperature sensor and digital-to-analog (DAC) mode; two analog comparators; and an 8MHz internal oscillator.

Some standard features on the AT89LP51RB2/RC2/IC2 are enhanced with new modes or operations. Mode 0 of Timer 0 or Timer 1 acts as a variable 9–16 bit timer/counter and Mode 1 acts as a 16-bit auto-reload timer/counter. In addition, each timer/counter may independently drive an 8-bit precision pulse width modulation output. Mode 0 (synchronous mode) of the serial port allows flexibility in the phase/polarity relationship between clock and data.

The I/O ports of the AT89LP51RB2/RC2/IC2 can be independently configured in one of four operating modes. In quasi-bidirectional mode, the ports operate as in the classic 8051. In input-only mode, the ports are tristated. Push-pull output mode provides full CMOS drivers and open-drain mode provides just a pull-down. Unlike other 8051s, this allows Port 0 to operate with on-chip pull-ups if desired.

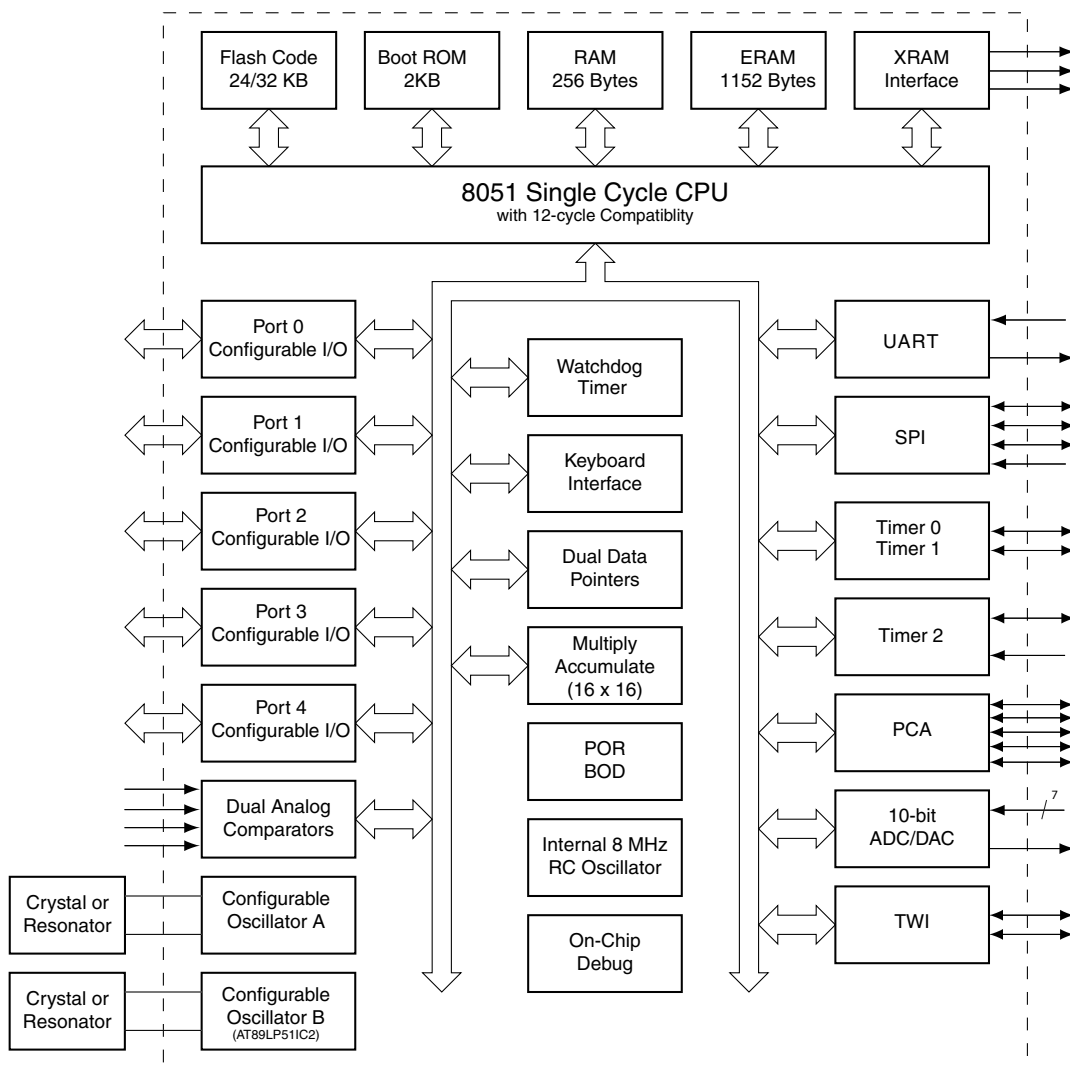
The AT89LP51RB2/RC2/IC2 includes an On-Chip Debug (OCD) interface that allows read-modify-write capabilities of the system state and program flow control, and programming of the internal memories. The on-chip Flash may also be programmed through the UART-based boot-loader or the SPI-based In-System programming interface (ISP).

The TWI and OCD features are not available on the PDIP package. The AT89LP51IC2 is also not available in PDIP.

The features of the AT89LP51RB2/RC2/IC2 make it a powerful choice for applications that need pulse width modulation, high speed I/O, and counting capabilities such as alarms, motor control, corded phones, and smart card readers.

## 2.1 Block Diagram

**Figure 2-1.** Atmel AT89LP51RB2/RC2/IC2 Block Diagram



## 2.2 System Configuration

The AT89LP51RB2/RC2/IC2 supports several system configuration options. Nonvolatile options are set through user fuses that must be programmed through the flash programming interface. Volatile options are controlled by software through individual bits of special function registers (SFRs). The AT89LP51RB2/RC2/IC2 must be properly configured before correct operation can occur.

### 2.2.1 Fuse Options

Table 2-1 lists the fusible options for the AT89LP51RB2/RC2/IC2. These options maintain their state even when the device is powered off. Some may be changed through the FLash API but others can only be changed with an external device programmer. For more information, see datasheet.

**Table 2-1.** User Configuration Fuses

| Fuse Name                         | Description   |
|-----------------------------------|---|
| Clock Source A                    | Selects between the High Speed Crystal Oscillator, Low Power Crystal Oscillator, External Clock on XTAL1A or Internal RC Oscillator for the source of the system clock when oscillator A is selected. |
| Clock Source B                    | Selects between the 32 kHz Crystal Oscillator, External Clock on XTAL1B or Internal RC Oscillator for the source of the system clock when oscillator B is selected (AT89LP51IC2 Only).                |
| Oscillator Select                 | Selects whether oscillator A or B is enabled to boot the device. (AT89LP51IC2 Only)   |
| X2 Mode                           | Selects the default state of whether the clock source is divided by two (X1) or not (X2) to generate the system clock.  |
| Start-up Time                     | Selects time-out delay for the POR/BOD/PWD wake-up period.  |
| Compatibility Mode                | Configures the CPU in 12-clock compatibility or single-cycle fast execution mode.   |
| XRAM Configuration                | Configures if access to on-chip memories that are mapped to the external data memory address space is enabled/disabled by default.  |
| Bootloader Jump Bit               | Enables or disables the on-chip bootloader.   |
| On-Chip Debug Enable              | Enables or disables On-Chip Debug. OCD must be enabled prior to using an in-circuit debugger with the device.   |
| In-System Programming Enable      | Enables or disables In-System Programming.  |
| User Signature Programming Enable | Enables or disables programming of User Signature array.  |
| Default Port State                | Configures the default port state as input-only mode (tristated) or quasi-bidirectional mode (weakly pulled high).  |
| Low Power Mode                    | Enables or disables power reduction features for lower system frequencies.  |

## 2.2.2 Software Options

Table 2-2 lists some important software configuration bits that affect operation at the system level. These can be changed by the application software but are set to their default values upon any reset. Most peripherals also have multiple configuration bits that are not listed here.

**Table 2-2.** Important Software Configuration Bits

| Bit(s)             | SFR Location   | Description  |
|--------------------|--|--|
| PxM0.y<br>PxM1.y   | P0M0, P0M1, P1M0, P1M1,<br>P2M0, P2M1, P3M0, P3M1,<br>P4M0, P4M1 | Configures the I/O mode of Port x Pin y to be one of input-only, quasi-bidirectional, push-pull output or open-drain. The default state is controlled by the Default Port State fuse above |
| CKRL               | CKRL   | Selects the division ratio between the oscillator and the system clock   |
| TPS <sub>3-0</sub> | CLKREG.7-4   | Selects the division ratio between the system clock and the timers   |
| ALES               | AUXR.0   | Enables/disables toggling of ALE   |
| EXRAM              | AUXR.1   | Enables/disables access to on-chip memories that are mapped to the external data memory address space  |
| WS <sub>1-0</sub>  | AUXR.6-5   | Selects the number of wait states when accessing external data memory  |
| XSTK               | AUXR1.4  | Configures the hardware stack to be in RAM or extra RAM  |
| ENBOOT             | AUXR1.5  | Enables/disables access to the on-chip Flash API   |

### 2.3.4 Timer/Counters

A common prescaler is available to divide the time base for Timer 0, Timer 1, Timer 2 and the WDT. The  $TPS_{3-0}$  bits in the CLKREG SFR control the prescaler. In Compatibility mode  $TPS_{3-0}$  defaults to 0101B, which causes the timers to count once every machine cycle. The counting rate can be adjusted linearly from the system clock rate to 1/16 of the system clock rate by changing  $TPS_{3-0}$ . In Fast mode  $TPS_{3-0}$  defaults to 0000B, or the system clock rate. TPS does not affect Timer 2 in Clock Out or Baud Generator modes.

In Compatibility mode the sampling of the external Timer/Counter pins: T0, T1, T2 and T2EX; and the external interrupt pins,  $\overline{INT0}$  and  $\overline{INT1}$ , is also controlled by the prescaler. In Fast mode these pins are always sampled at the system clock rate.

Both Timer 0 and Timer 1 can toggle their respective counter pins, T0 and T1, when they overflow by setting the output enable bits in TCONB.

### 2.3.5 Interrupt Handling

Fast mode allows for faster interrupt response due to the shorter instruction execution times.

### 2.3.6 Keyboard Interface

The AT89LP51RB2/RC2/IC2 does not clear the keyboard flag register (KBF) after a read. Each bit must be cleared in software. This allows the interrupt to be generate once per flag when multiple flags are set, if desired. To mimic the old behavior the service routine must clear the whole register.

The keyboard can also support general edge-triggered interrupts with the addition of the KBMOD register.

### 2.3.7 Serial Port

The timer prescaler increases the range of achievable baud rates when using Timer 1 to generate the baud rate in UART Modes 1 or 3, including an increase in the maximum baud rate available in Compatibility mode. Additional features include automatic address recognition and framing error detection.

The shift register mode (Mode 0) has been enhanced with more control of the polarity, phase and frequency of the clock and full-duplex operation. This allows emulation of master serial peripheral (SPI) and two-wire (TWI) interfaces.

### 2.3.8 I/O Ports

The P0, P1, P2 and P3 I/O ports of the AT89LP51RB2/RC2/IC2 may be configured in four different modes. The default setting depends on the Tristate-Port User Fuse. When the fuse is set all the I/O ports revert to input-only (tristated) mode at power-up or reset. When the fuse is not active, ports P1, P2 and P3 start in quasi-bidirectional mode and P0 starts in open-drain mode. P4 always operates in quasi-bidirectional mode. P0 can be configured to have internal pull-ups by placing it in quasi-bidirectional or output modes. This can reduce system cost by removing the need for external pull-ups on Port 0.

The P4.4–P4.7 pins are additional I/Os that replace the normally dedicated ALE, PSEN, XTAL1 and XTAL2 pins of the AT89C51RB2/RC2/IC2. These pins can be used as additional I/Os depending on the configuration of the clock and external memory.



## 2.3.9 Security

The AT89LP51RB2/RC2/IC2 does not support the external access pin ( $\overline{EA}$ ). Therefore it is not possible to execute from external program memory in address range 0000H–1FFFFH. When the third Lockbit is enabled (Lock Mode 4) external program execution is disabled for all addresses above 1FFFFH. This differs from AT89C51RB2/RC2/IC2 where Lock Mode 4 prevents  $\overline{EA}$  from being sampled low, but may still allow external execution at addresses outside the 8K internal space.

## 2.3.10 Programming

The AT89LP51RB2/RC2/IC2 supports a richer command set for In-System Programming (ISP). Existing AT89C51RB2/RC2 programmers should be able to program the AT89LP51RB2/RC2/IC2 in byte mode. In page mode the AT89LP51RB2/RC2/IC2 only supports programming of a half-page of 64 bytes and therefore requires an extra address byte as compared to AT89C51RB2/RC2. Furthermore the device signature is located at addresses 0000H, 0001H and 0003H instead of 0000H, 0100H and 0200H.

**Table 2-3.** Compatibility Mode versus Fast Mode Summary

| Feature   | Compatibility   | Fast            |
|---|-----------------|-----------------|
| Instruction Fetch in System Clocks  | 3               | 1               |
| Instruction Execution Time in System Clocks                                   | 6, 12, 18 or 24 | 1, 2, 3, 4 or 5 |
| Default System Clock Divisor  | 2               | 1               |
| Default Timer Prescaler Divisor   | 6               | 1               |
| Pin Sampling Rate ( $\overline{INT0}$ , $\overline{INT1}$ , T0, T1, T2, T2EX) | Prescaler Rate  | System Clock    |
| Minimum RST input pulse in System Clocks                                      | 12              | 2               |

**Table 3-2. C51 Core SFRs**

| Mnemonic | Add | Name                             | 7  | 6  | 5  | 4   | 3    | 2    | 1   | 0   |
|----------|-----|----------------------------------|----|----|----|-----|------|------|-----|-----|
| ACC      | E0h | Accumulator                      |    |    |    |     |      |      |     |     |
| B        | F0h | B Register                       |    |    |    |     |      |      |     |     |
| PSW      | D0h | Program Status Word              | CY | AC | F0 | RS1 | RS0  | OV   | F1  | P   |
| SP       | 81h | Stack Pointer                    |    |    |    |     |      |      |     |     |
| SPX      | EFh | Extended Stack Pointer           | –  | –  | –  | –   | SP11 | SP10 | SP9 | SP8 |
| DPL      | 82h | Data Pointer Low Byte            |    |    |    |     |      |      |     |     |
| DPH      | 83h | Data Pointer High Byte           |    |    |    |     |      |      |     |     |
| DPLB     | D4h | Alternate Data Pointer Low Byte  |    |    |    |     |      |      |     |     |
| DPHB     | D5h | Alternate Data Pointer High Byte |    |    |    |     |      |      |     |     |
| PAGE     | F6h | ERAM Page Register               | –  | –  | –  | –   |      |      |     |     |

**Table 3-3. Digital Signal Processing SFRs**

| Mnemonic | Add | Name                 | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|----------|-----|----------------------|------|------|------|------|------|------|------|------|
| AX       | E1h | Extended Accumulator |      |      |      |      |      |      |      |      |
| BX       | F7h | Extended B Register  |      |      |      |      |      |      |      |      |
| DSPR     | E2h | DSP Control Register | MRW1 | MRW0 | SMLB | SMLA | CBE1 | CBE0 | MVCD | DPRB |
| FIRD     | E3h | FIFO Depth           |      |      |      |      |      |      |      |      |
| MACL     | E4h | MAC Low Byte         |      |      |      |      |      |      |      |      |
| MACH     | E5h | MAC High Byte        |      |      |      |      |      |      |      |      |

**Table 3-4. System Management SFRs**

| Mnemonic              | Add | Name                        | 7     | 6     | 5      | 4    | 3    | 2      | 1      | 0      |
|-----------------------|-----|-----------------------------|-------|-------|--------|------|------|--------|--------|--------|
| PCON                  | 87h | Power Control               | SMOD1 | SMOD0 | PWDEX  | POF  | GF1  | GF0    | PD     | IDL    |
| AUXR                  | 8Eh | Auxiliary Register 0        | DPU   | WS1   | WS0/M0 | XRS2 | XRS1 | XRS0   | EXTRAM | AO     |
| AUXR1                 | A2h | Auxiliary Register 1        | –     | –     | ENBOOT | XSTK | GF3  | 0      | –      | DPS    |
| DPCR                  | A3h | Datapointer Config Register | DPU1  | DPU0  | DPD1   | DPD0 | –    | –      | –      | –      |
| CKRL                  | 97h | Clock Reload Register       |       |       |        |      |      |        |        |        |
| CKCKON0               | 8Fh | Clock Control Register 0    | TWIX2 | WDTX2 | PCAX2  | SIX2 | T2X2 | T1X2   | T0X2   | X2     |
| CKCKON1               | AFh | Clock Control Register 1    | –     | –     | –      | –    | –    | –      | –      | SPIX2  |
| CKSEL <sup>(1)</sup>  | 85h | Clock Selection Register    | –     | –     | –      | –    | –    | –      | –      | CKS    |
| CLKREG                | AEh | Clock Register              | TPS3  | TPS2  | TPS1   | TPS0 | –    | –      | –      | –      |
| OSCCON <sup>(1)</sup> | 85h | Oscillator Control Register | –     | –     | –      | –    | –    | SCLKT0 | OscBEn | OscAEn |

Note: 1. Present on AT89LP51IC2 Only

**Table 3-5.** Interrupt SFRs

| Mnemonic | Add | Name                              | 7    | 6    | 5    | 4     | 3    | 2    | 1    | 0    |
|----------|-----|-----------------------------------|------|------|------|-------|------|------|------|------|
| IEN0     | A8h | Interrupt Enable Control 0        | EA   | EC   | ET2  | ES    | ET1  | EX1  | ET0  | EX0  |
| IEN1     | B1h | Interrupt Enable Control 1        | –    | –    | EADC | ECMP  | –    | ESPI | ETWI | EKB  |
| IPH0     | B7h | Interrupt Priority Control High 0 | IP1D | PPCH | PT2H | PHS   | PT1H | PX1H | PT0H | PX0H |
| IPL0     | B8h | Interrupt Priority Control Low 0  | IP0D | PPCL | PT2L | PLS   | PT1L | PX1L | PT0L | PX0L |
| IPH1     | B3h | Interrupt Priority Control High 1 | IP3D | –    | PADL | PCMPL | –    | SPIH | PTWL | PKBH |
| IPL1     | B2h | Interrupt Priority Control Low 1  | IP2D | –    | PADH | PCMPH | –    | SPIH | PTWH | PKBL |

**Table 3-6.** Port SFRs

| Mnemonic | Add | Name          | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----|---------------|---|---|---|---|---|---|---|---|
| P0       | 80h | 8-bit Port 0  |   |   |   |   |   |   |   |   |
| P1       | 90h | 8-bit Port 1  |   |   |   |   |   |   |   |   |
| P2       | A0h | 8-bit Port 2  |   |   |   |   |   |   |   |   |
| P3       | B0h | 8-bit Port 3  |   |   |   |   |   |   |   |   |
| P4       | C0h | 8-bit Port 4  |   |   |   |   |   |   |   |   |
| P0M0     | E6h | Port 0 Mode 0 |   |   |   |   |   |   |   |   |
| P0M1     | E7h | Port 0 Mode 1 |   |   |   |   |   |   |   |   |
| P1M0     | D6h | Port 1 Mode 0 |   |   |   |   |   |   |   |   |
| P1M1     | D7h | Port 1 Mode 1 |   |   |   |   |   |   |   |   |
| P2M0     | CEh | Port 2 Mode 0 |   |   |   |   |   |   |   |   |
| P2M1     | CFh | Port 2 Mode 1 |   |   |   |   |   |   |   |   |
| P3M0     | C6h | Port 3 Mode 0 |   |   |   |   |   |   |   |   |
| P3M1     | C7h | Port 3 Mode 1 |   |   |   |   |   |   |   |   |
| P4M0     | BEh | Port 4 Mode 0 |   |   |   |   |   |   |   |   |
| P4M1     | BFh | Port 4 Mode 1 |   |   |   |   |   |   |   |   |

**Table 3-7.** Serial I/O Port SFRs

| Mnemonic | Add | Name               | 7      | 6   | 5   | 4   | 3    | 2    | 1   | 0   |
|----------|-----|--------------------|--------|-----|-----|-----|------|------|-----|-----|
| SCON     | 98h | Serial Control     | FE/SM0 | SM1 | SM2 | REN | TB8  | RB8  | TI  | RI  |
| SBUF     | 99h | Serial Data Buffer |        |     |     |     |      |      |     |     |
| SADEN    | B9h | Slave Address Mask |        |     |     |     |      |      |     |     |
| SADDR    | A9h | Slave Address      |        |     |     |     |      |      |     |     |
| BDRCON   | 9Bh | Baud Rate Control  | –      | –   | –   | BRR | TBCK | RBCK | SPD | SRC |
| BRL      | 9Ah | Baud Rate Reload   |        |     |     |     |      |      |     |     |

**Table 3-8. Timer SFRs**

| Mnemonic | Add | Name                                     | 7     | 6    | 5    | 4    | 3     | 2    | 1    | 0      |
|----------|-----|--|-------|------|------|------|-------|------|------|--------|
| TCON     | 88h | Timer/Counter 0 and 1 Control            | TF1   | TR1  | TF0  | TR0  | IE1   | IT1  | IE0  | IT0    |
| TMOD     | 89h | Timer/Counter 0 and 1 Modes              | GATE1 | C/T1 | M11  | M01  | GATE0 | C/T0 | M10  | M00    |
| TCONB    | 91h | Timer/Counter 0 and 1 Mode B             |       |      |      |      |       |      |      |        |
| TL0      | 8Ah | Timer/Counter 0 Low Byte                 |       |      |      |      |       |      |      |        |
| TH0      | 8Ch | Timer/Counter 0 High Byte                |       |      |      |      |       |      |      |        |
| TL1      | 8Bh | Timer/Counter 1 Low Byte                 |       |      |      |      |       |      |      |        |
| TH1      | 8Dh | Timer/Counter 1 High Byte                |       |      |      |      |       |      |      |        |
| RL0      | F2h | Timer/Counter 0 Reload Low               |       |      |      |      |       |      |      |        |
| RH0      | F3h | Timer/Counter 0 Reload High              |       |      |      |      |       |      |      |        |
| RTL1     | F4h | Timer/Counter 1 Reload Low               |       |      |      |      |       |      |      |        |
| RH1      | F5h | Timer/Counter 1 Reload High              |       |      |      |      |       |      |      |        |
| WDRST    | A6h | WatchDog Timer Reset                     |       |      |      |      |       |      |      |        |
| WDTPRG   | A7h | WatchDog Timer Program                   |       |      |      |      |       | WTO2 | WTO1 | WTO0   |
| T2CON    | C8h | Timer/Counter 2 control                  | TF2   | EXF2 | RCLK | TCLK | EXEN2 | TR2  | C/T2 | CP/RL2 |
| T2MOD    | C9h | Timer/Counter 2 Mode                     | —     | —    | —    | —    | —     | —    | T2OE | DCEN   |
| RCAP2H   | CBh | Timer/Counter 2 Reload/Capture High Byte |       |      |      |      |       |      |      |        |
| RCAP2L   | CAh | Timer/Counter 2 Reload/Capture Low Byte  |       |      |      |      |       |      |      |        |
| TH2      | CDh | Timer/Counter 2 High Byte                |       |      |      |      |       |      |      |        |
| TL2      | CCh | Timer/Counter 2 Low Byte                 |       |      |      |      |       |      |      |        |

**Table 3-9. SPI Controller SFRs**

| Mnemonic | Add | Name        | 7    | 6    | 5     | 4    | 3    | 2    | 1    | 0    |
|----------|-----|-------------|------|------|-------|------|------|------|------|------|
| SPCON    | C3h | SPI Control | SPR2 | SPEN | SSDIS | MSTR | CPOL | CPHA | SPR1 | SPR0 |
| SPSTA    | C4h | SPI Status  | SPIF | WCOL | SSERR | MODF |      |      |      |      |
| SPDAT    | C5h | SPI Data    | SPD7 | SPD6 | SPD5  | SPD4 | SPD3 | SPD2 | SPD1 | SPD0 |

**Table 3-10. TWI Controller SFRs**

| Mnemonic | Add | Name                       | 7     | 6    | 5     | 4     | 3    | 2    | 1     | 0     |
|----------|-----|----------------------------|-------|------|-------|-------|------|------|-------|-------|
| SSCON    | 93h | Synchronous Serial Control | SSCR2 | SSPE | SSSTA | SSSTO | SSI  | SSAA | SSCR1 | SSCR0 |
| SSCS     | 94h | Synchronous Serial Status  | SSC4  | SSC3 | SSC2  | SSC1  | SSC0 | 0    | 0     | 0     |
| SSDAT    | 95h | Synchronous Serial Data    |       |      |       |       |      |      |       |       |
| SSADR    | 96h | Synchronous Serial Address | SSA7  | SSA6 | SSA5  | SSA4  | SSA3 | SSA2 | SSA1  | SSGC  |

**Table 3-11. Keyboard Interface SFRs**

| Mnemonic | Add | Name                    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|----------|-----|-------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| KBLS     | 9Ch | Keyboard Level Selector | KBLS7 | KBLS6 | KBLS5 | KBLS4 | KBLS3 | KBLS2 | KBLS1 | KBLS0 |
| KBE      | 9Dh | Keyboard Input Enable   | KBE7  | KBE6  | KBE5  | KBE4  | KBE3  | KBE2  | KBE1  | KBE0  |
| KBF      | 9Eh | Keyboard Flag Register  | KBF7  | KBF6  | KBF5  | KBF4  | KBF3  | KBF2  | KBF1  | KBF0  |
| KBMOD    | 9Fh | Keyboard Mode Register  | KBM7  | KBM6  | KBM5  | KBM4  | KBM3  | KBM2  | KBM1  | KBM0  |

**Table 3-12. Flash Memory SFR**

| Mnemonic | Add | Name                      | 7     | 6     | 5     | 4     | 3   | 2     | 1     | 0     |
|----------|-----|---------------------------|-------|-------|-------|-------|-----|-------|-------|-------|
| BMSEL    | 92h | Bank Mode Select Register | –     | –     | –     | –     | –   | –     | –     | FBS   |
| FCON     | D2h | Flash Control Register    | FPSL3 | FPSL2 | FPSL1 | FPSL0 | FPS | FMOD1 | FMOD0 | FBUSY |

**Table 3-13. Analog Comparator SFRs**

| Mnemonic | Add | Name                          | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----|-------------------------------|---|---|---|---|---|---|---|---|
| ACSRA    | A3h | Comparator A Control Register |   |   |   |   |   |   |   |   |
| ACSRB    | ABh | Comparator B Control Register |   |   |   |   |   |   |   |   |
| AREF     | BDh | Comparator Reference Register |   |   |   |   |   |   |   |   |

**Table 3-14. ADC Controller SFRs**

| Mnemonic | Add | Name                       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----|----------------------------|---|---|---|---|---|---|---|---|
| DADC     | A4h | DAC/ADC Control Register   |   |   |   |   |   |   |   |   |
| DADI     | A5h | DAC/ADC Input Register     |   |   |   |   |   |   |   |   |
| DADL     | ACH | DAC/ADC Data Low Register  |   |   |   |   |   |   |   |   |
| DADH     | ADh | DAC/ADC Data High Register |   |   |   |   |   |   |   |   |

**Table 3-15. PCA SFRs**

| Mnemonic | Add | Name                        | 7    | 6     | 5     | 4     | 3    | 2    | 1    | 0     |
|----------|-----|-----------------------------|------|-------|-------|-------|------|------|------|-------|
| CCON     | D8h | PCA Timer/Counter Control   | CF   | CR    |       | CCF4  | CCF3 | CCF2 | CCF1 | CCF0  |
| CMOD     | D9h | PCA Timer/Counter Mode      | CIDL | WDTE  |       |       |      | CPS1 | CPS0 | ECF   |
| CL       | E9h | PCA Timer/Counter Low Byte  |      |       |       |       |      |      |      |       |
| CH       | F9h | PCA Timer/Counter High Byte |      |       |       |       |      |      |      |       |
| CCAPM0   | DAh | PCA Timer/Counter Mode 0    |      | ECOM0 | CAPP0 | CAPN0 | MAT0 | TOG0 | PWM0 | ECCF0 |
| CCAPM1   | DBh | PCA Timer/Counter Mode 1    |      | ECOM1 | CAPP1 | CAPN1 | MAT1 | TOG1 | PWM1 | ECCF1 |
| CCAPM2   | DCh | PCA Timer/Counter Mode 2    |      | ECOM2 | CAPP2 | CAPN2 | MAT2 | TOG2 | PWM2 | ECCF2 |
| CCAPM3   | DDh | PCA Timer/Counter Mode 3    |      | ECOM3 | CAPP3 | CAPN3 | MAT3 | TOG3 | PWM3 | ECCF3 |

**Table 3-15. PCA SFRs (Continued)**

| Mnemo<br>-nic | Add | Name                           | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|---------------|-----|--------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| CCAPM4        | DEh | PCA Timer/Counter Mode 4       |         | ECOM4   | CAPP4   | CAPN4   | MAT4    | TOG4    | PWM4    | ECCF4   |
| CCAP0H        | FAh | PCA Compare Capture Module 0 H | CCAP0H7 | CCAP0H6 | CCAP0H5 | CCAP0H4 | CCAP0H3 | CCAP0H2 | CCAP0H1 | CCAP0H0 |
| CCAP1H        | FBh | PCA Compare Capture Module 1 H | CCAP1H7 | CCAP1H6 | CCAP1H5 | CCAP1H4 | CCAP1H3 | CCAP1H2 | CCAP1H1 | CCAP1H0 |
| CCAP2H        | FCh | PCA Compare Capture Module 2 H | CCAP2H7 | CCAP2H6 | CCAP2H5 | CCAP2H4 | CCAP2H3 | CCAP2H2 | CCAP2H1 | CCAP2H0 |
| CCAP3H        | FDh | PCA Compare Capture Module 3 H | CCAP3H7 | CCAP3H6 | CCAP3H5 | CCAP3H4 | CCAP3H3 | CCAP3H2 | CCAP3H1 | CCAP3H0 |
| CCAP4H        | FEh | PCA Compare Capture Module 4 H | CCAP4H7 | CCAP4H6 | CCAP4H5 | CCAP4H4 | CCAP4H3 | CCAP4H2 | CCAP4H1 | CCAP4H0 |
| CCAP0L        | EAh | PCA Compare Capture Module 0 L | CCAP0L7 | CCAP0L6 | CCAP0L5 | CCAP0L4 | CCAP0L3 | CCAP0L2 | CCAP0L1 | CCAP0L0 |
| CCAP1L        | EBh | PCA Compare Capture Module 1 L | CCAP1L7 | CCAP1L6 | CCAP1L5 | CCAP1L4 | CCAP1L3 | CCAP1L2 | CCAP1L1 | CCAP1L0 |
| CCAP2L        | ECh | PCA Compare Capture Module 2 L | CCAP2L7 | CCAP2L6 | CCAP2L5 | CCAP2L4 | CCAP2L3 | CCAP2L2 | CCAP2L1 | CCAP2L0 |
| CCAP3L        | EDh | PCA Compare Capture Module 3 L | CCAP3L7 | CCAP3L6 | CCAP3L5 | CCAP3L4 | CCAP3L3 | CCAP3L2 | CCAP3L1 | CCAP3L0 |
| CCAP4L        | EEh | PCA Compare Capture Module 4 L | CCAP4L7 | CCAP4L6 | CCAP4L5 | CCAP4L4 | CCAP4L3 | CCAP4L2 | CCAP4L1 | CCAP4L0 |

## 4. Ordering Information

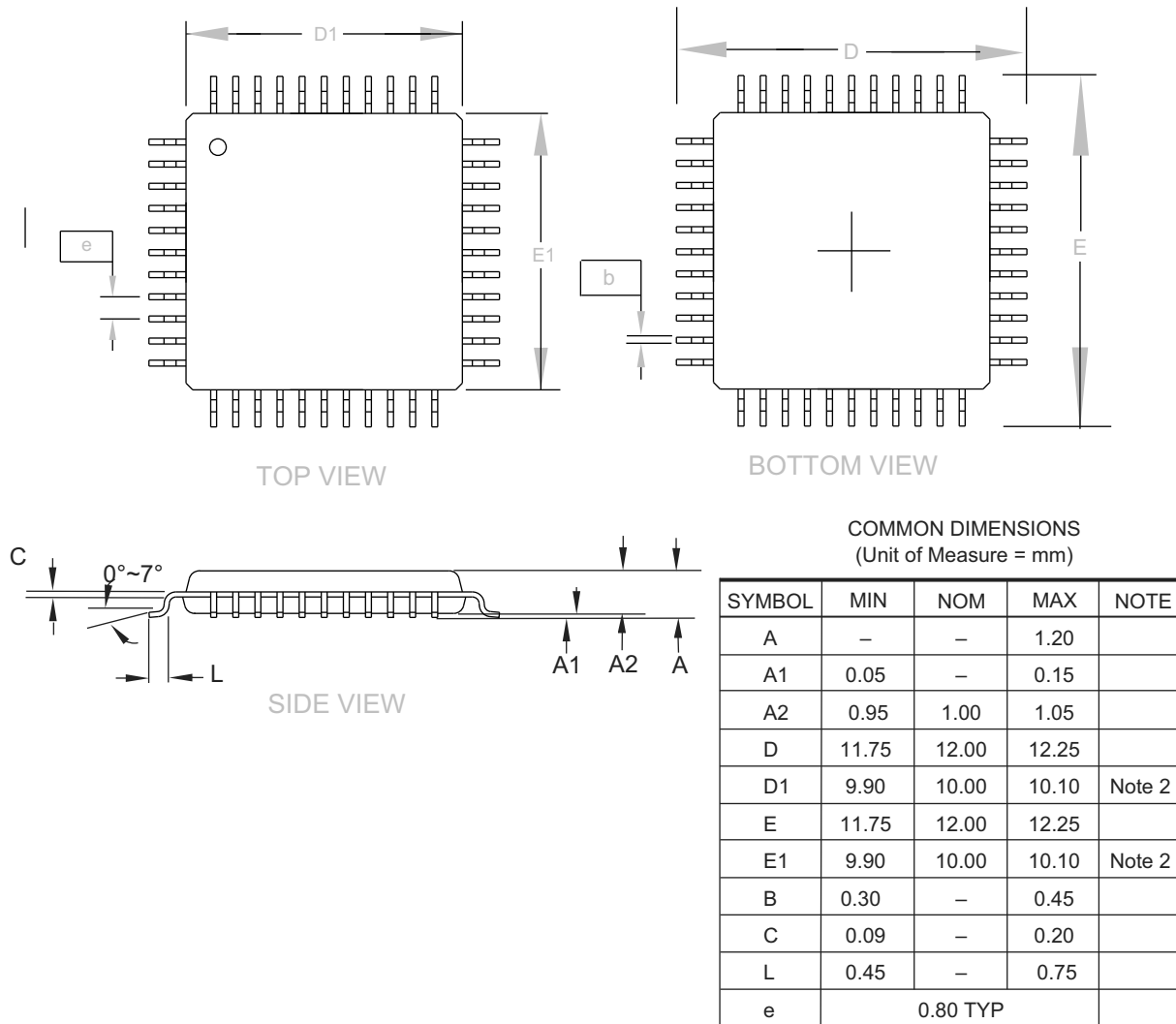
### 4.1 Green Package Option (Pb/Halide-free)

| Supply Voltage | Speed <sup>(1)</sup> | Temperature Range               | Code Flash | # Oscillators | Ordering Code      | Package     | Packing |
|----------------|----------------------|---------------------------------|------------|---------------|--------------------|-------------|---------|
| 2.4V to 5.5V   | 20 MHz               | Industrial<br>(-40° C to 85° C) | 24KB       | 1             | AT89LP51RB2-20AAU  | 44AA (LQFP) | Tray    |
|                |                      |                                 |            |               | AT89LP51RB2-20AAUR |             | Reel    |
|                |                      |                                 |            |               | AT89LP51RB2-20AU   | 44A (TQFP)  | Tray    |
|                |                      |                                 |            |               | AT89LP51RB2-20AUR  |             | Reel    |
|                |                      |                                 |            |               | AT89LP51RB2-20JU   | 44J (PLCC)  | Stick   |
|                |                      |                                 |            |               | AT89LP51RB2-20JUR  |             | Reel    |
|                |                      |                                 |            |               | AT89LP51RB2-20MU   | 44M1 (VQFN) | Tray    |
|                |                      |                                 |            |               | AT89LP51RB2-20MUR  |             | Reel    |
|                |                      |                                 |            |               | AT89LP51RB2-20PU   | 40P6 (PDIP) | Stick   |
|                |                      |                                 | 32KB       | 1             | AT89LP51RC2-20AAU  | 44AA (LQFP) | Tray    |
|                |                      |                                 |            |               | AT89LP51RC2-20AAUR |             | Reel    |
|                |                      |                                 |            |               | AT89LP51RC2-20AU   | 44A (TQFP)  | Tray    |
|                |                      |                                 |            |               | AT89LP51RC2-20AUR  |             | Reel    |
|                |                      |                                 |            |               | AT89LP51RC2-20JU   | 44J (PLCC)  | Stick   |
|                |                      |                                 |            |               | AT89LP51RC2-20JUR  |             | Reel    |
|                |                      |                                 |            |               | AT89LP51RC2-20MU   | 44M1 (VQFN) | Tray    |
|                |                      |                                 |            |               | AT89LP51RC2-20MUR  |             | Reel    |
|                |                      |                                 |            |               | AT89LP51RC2-20PU   | 40P6 (PDIP) | Stick   |
|                |                      |                                 | 32KB       | 2             | AT89LP51IC2-20AAU  | 44AA (LQFP) | Tray    |
|                |                      |                                 |            |               | AT89LP51IC2-20AAUR |             | Reel    |
|                |                      |                                 |            |               | AT89LP51IC2-20AU   | 44A (TQFP)  | Tray    |
|                |                      |                                 |            |               | AT89LP51IC2-20AUR  |             | Reel    |
|                |                      |                                 |            |               | AT89LP51IC2-20JU   | 44J (PLCC)  | Stick   |
|                |                      |                                 |            |               | AT89LP51IC2-20JUR  |             | Reel    |
|                |                      |                                 |            |               | AT89LP51IC2-20MU   | 44M1 (VQFN) | Tray    |
|                |                      |                                 |            |               | AT89LP51IC2-20MUR  |             | Reel    |

- Notes: 1. Speed is specified for single-cycle Fast Mode with X2 clock  
2. See Table 4-1 on page 19 for a cross reference between AT89C51RB2/RC2/IC2 and AT89LP51RB2/RC2/IC2

| Package Types |   |
|---------------|---|
| <b>44AA</b>   | 44-lead, Very Thin Plastic Quad Flat Package, 1.2 mm Thickness (VQFP/LQFP)          |
| <b>44A</b>    | 44-lead, Thin Plastic Quad Flat Package, 1.0 mm Thickness (TQFP)                    |
| <b>44J</b>    | 44-lead, Plastic J-leaded Chip Carrier (PLCC)                                       |
| <b>44M1</b>   | 44-pad, 7 x 7 x 1.0 mm Body, Plastic Very Thin Quad Flat No Lead Package (VQFN/MLF) |
| <b>40P6</b>   | 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)                            |

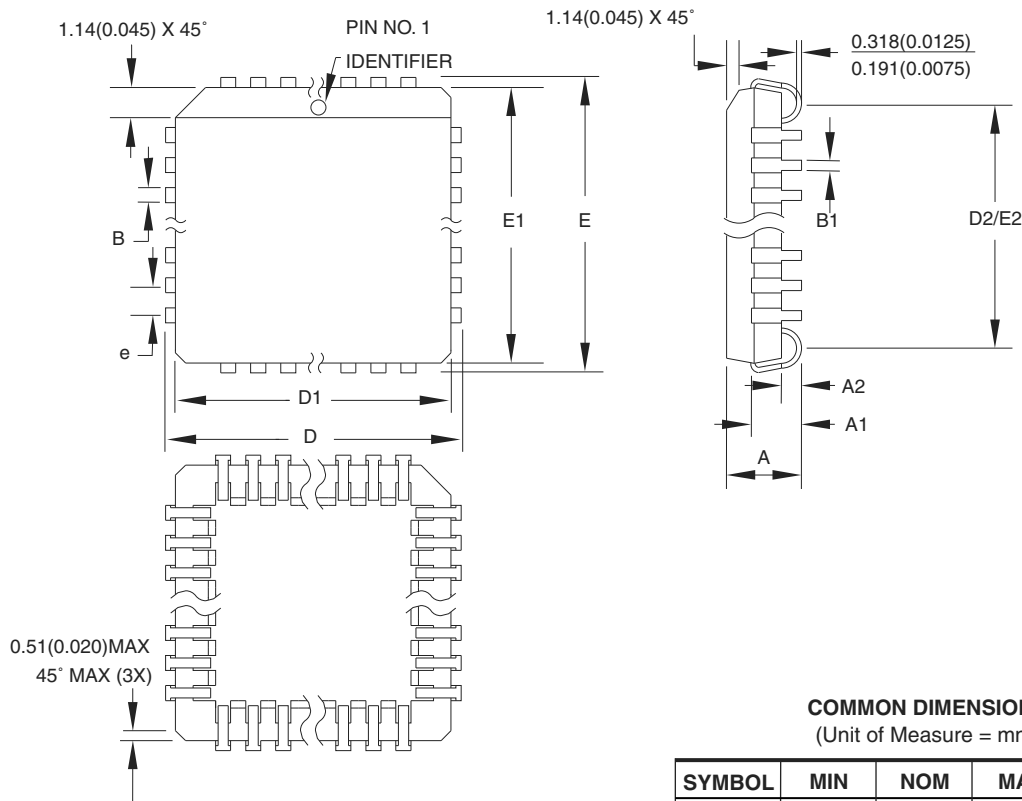
## 5.2 44A – TQFP



- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  3. Lead coplanarity is 0.10 mm maximum.



## 5.3 44J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

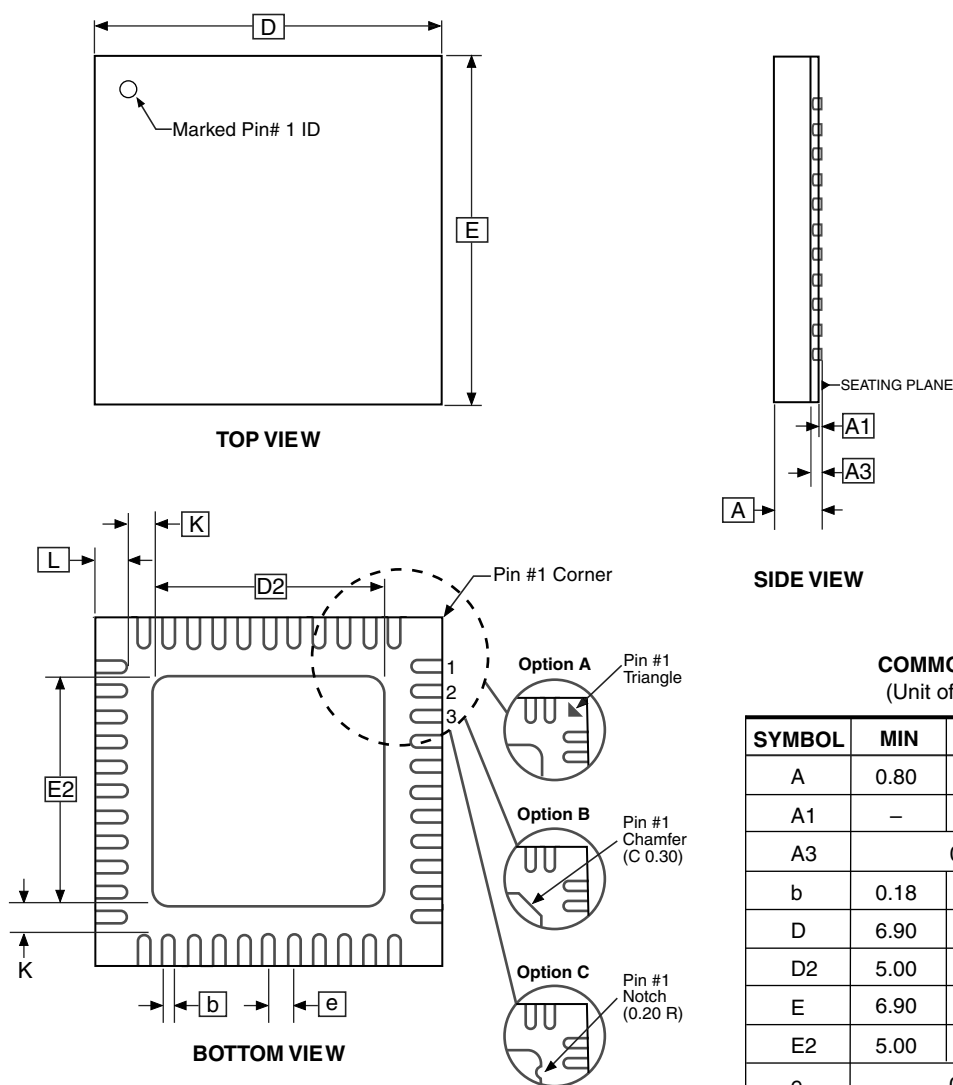
| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | 4.191     | –   | 4.572  |        |
| A1     | 2.286     | –   | 3.048  |        |
| A2     | 0.508     | –   | –      |        |
| D      | 17.399    | –   | 17.653 |        |
| D1     | 16.510    | –   | 16.662 | Note 2 |
| E      | 17.399    | –   | 17.653 |        |
| E1     | 16.510    | –   | 16.662 | Note 2 |
| D2/E2  | 14.986    | –   | 16.002 |        |
| B      | 0.660     | –   | 0.813  |        |
| B1     | 0.330     | –   | 0.533  |        |
| e      | 1.270 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

|  |  |                           |                  |
|--|--|---------------------------|------------------|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | <b>TITLE</b><br><b>44J</b> , 44-lead, Plastic J-leaded Chip Carrier (PLCC) | <b>DRAWING NO.</b><br>44J | <b>REV.</b><br>B |
|--|--|---------------------------|------------------|

## 5.4 44M1 – VQFN/MLF



Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

9/26/08

**Package Drawing Contact:**  
packagedrawings@atmel.com

**TITLE**  
44M1, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)

**GPC**

ZWS

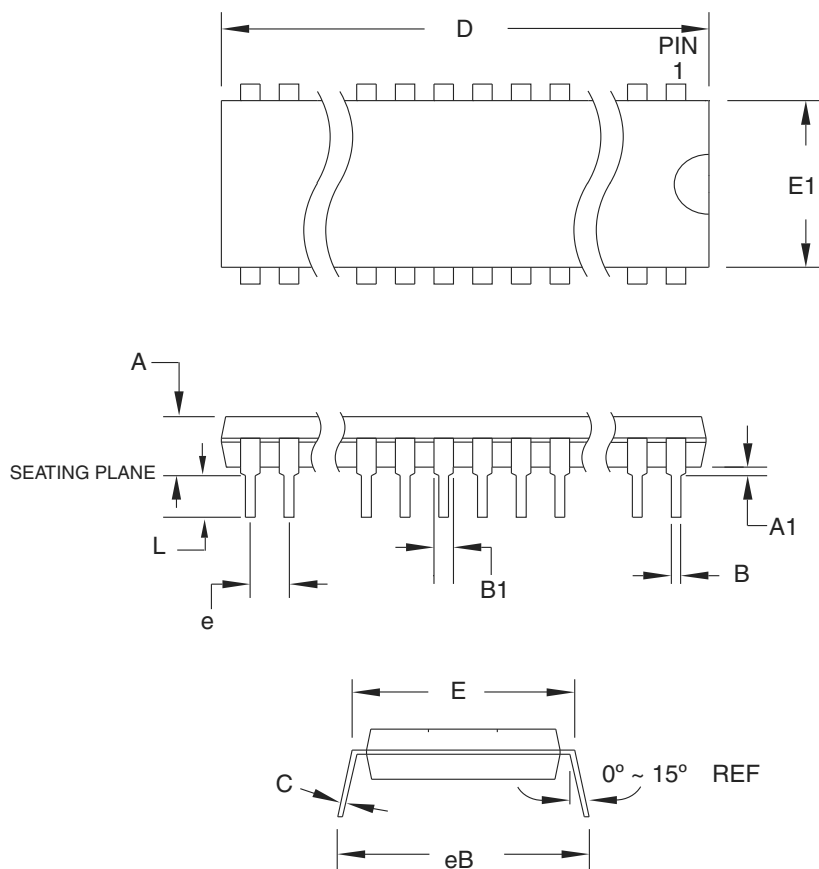
**DRAWING NO.**

44M1

**REV.**

H

## 5.5 40P6 – PDIP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | –         | –   | 4.826  |        |
| A1     | 0.381     | –   | –      |        |
| D      | 52.070    | –   | 52.578 | Note 2 |
| E      | 15.240    | –   | 15.875 |        |
| E1     | 13.462    | –   | 13.970 | Note 2 |
| B      | 0.356     | –   | 0.559  |        |
| B1     | 1.041     | –   | 1.651  |        |
| L      | 3.048     | –   | 3.556  |        |
| C      | 0.203     | –   | 0.381  |        |
| eB     | 15.494    | –   | 17.526 |        |
| e      | 2.540 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
  2. Dimensions D and E1 do not include mold Flash or Protrusion.  
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

|  |  |                            |                  |
|--|--|----------------------------|------------------|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | <b>TITLE</b><br><b>40P6</b> , 40-lead (0.600"/15.24 mm Wide) Plastic Dual<br>Inline Package (PDIP) | <b>DRAWING NO.</b><br>40P6 | <b>REV.</b><br>B |
|--|--|----------------------------|------------------|

## 6. Revision History

| Revision No.              | History   |
|---------------------------|---|
| Revision A – October 2011 | <ul style="list-style-type: none"><li>Initial Release</li></ul> |

**Atmel Corporation**

2325 Orchard Parkway  
San Jose, CA 95131  
USA

**Tel:** (+1) (408) 441-0311

**Fax:** (+1) (408) 487-2600

[www.atmel.com](http://www.atmel.com)

8051@atmel.com

**Atmel Asia Limited**

Unit 01-5 & 16, 19F  
BEA Tower, Millennium City 5  
418 Kwun Tong Road  
Kwun Tong, Kowloon  
HONG KONG

**Tel:** (+852) 2245-6100

**Fax:** (+852) 2722-1369

**Atmel Munich GmbH**

Business Campus  
Packring 4  
D-85748 Garching b. Munich  
GERMANY

**Tel:** (+49) 89-31970-0

**Fax:** (+49) 89-3194621

**Atmel Japan**

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
JAPAN

**Tel:** (+81) (3) 3523-3551

**Fax:** (+81) (3) 3523-7581

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