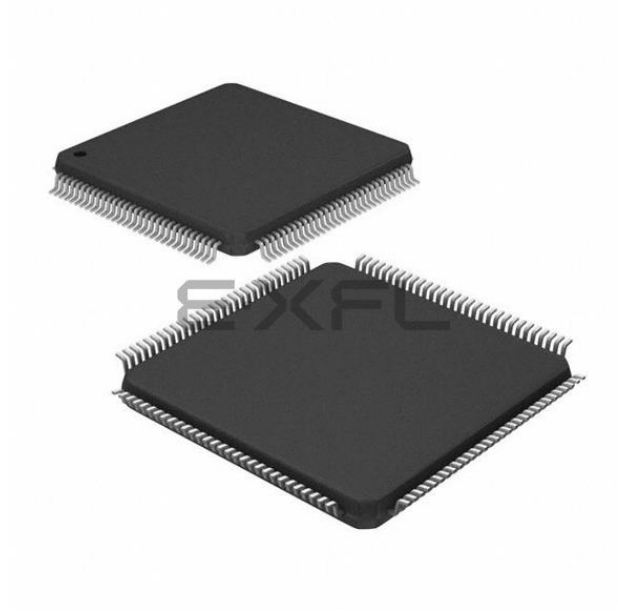
Rohm Semiconductor - ML610Q411P-NNNTB0ARL Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	625kHz
Connectivity	I²C, SSP, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 2x12b, 2x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q411p-nnntb0arl

- Frame frequency selecable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
- Bias voltage multiplying clock selectable (8 types)
- Contrast adjustment (32 steps)
- LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow

- Battery Level Detector
  - Threshold voltages: One of 16 levels
  - Accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed crystal oscillation clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (500 kHz)
    External clock (500kH or less)
  - High-speed Clock gear: 1/2(250kHz), 1/4(125kHz), 1/8(62.5kHz: default)
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, External clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
  - Block Control Function: Resets and completely turns circuits of unused peripherals off.

- Guaranteed operating range
  - Operating temperature: –20°C to +70°C (P version: –40°C to +85°C)
  - Operating voltage: V_{DD} = 1.1V to 3.6V, AV_{DD} = 2.2V to 3.6V

ML610Q412 Block Diagram

Figure 2 show the block diagram of the ML610Q412.
"*" indicates the secondary function of each port.

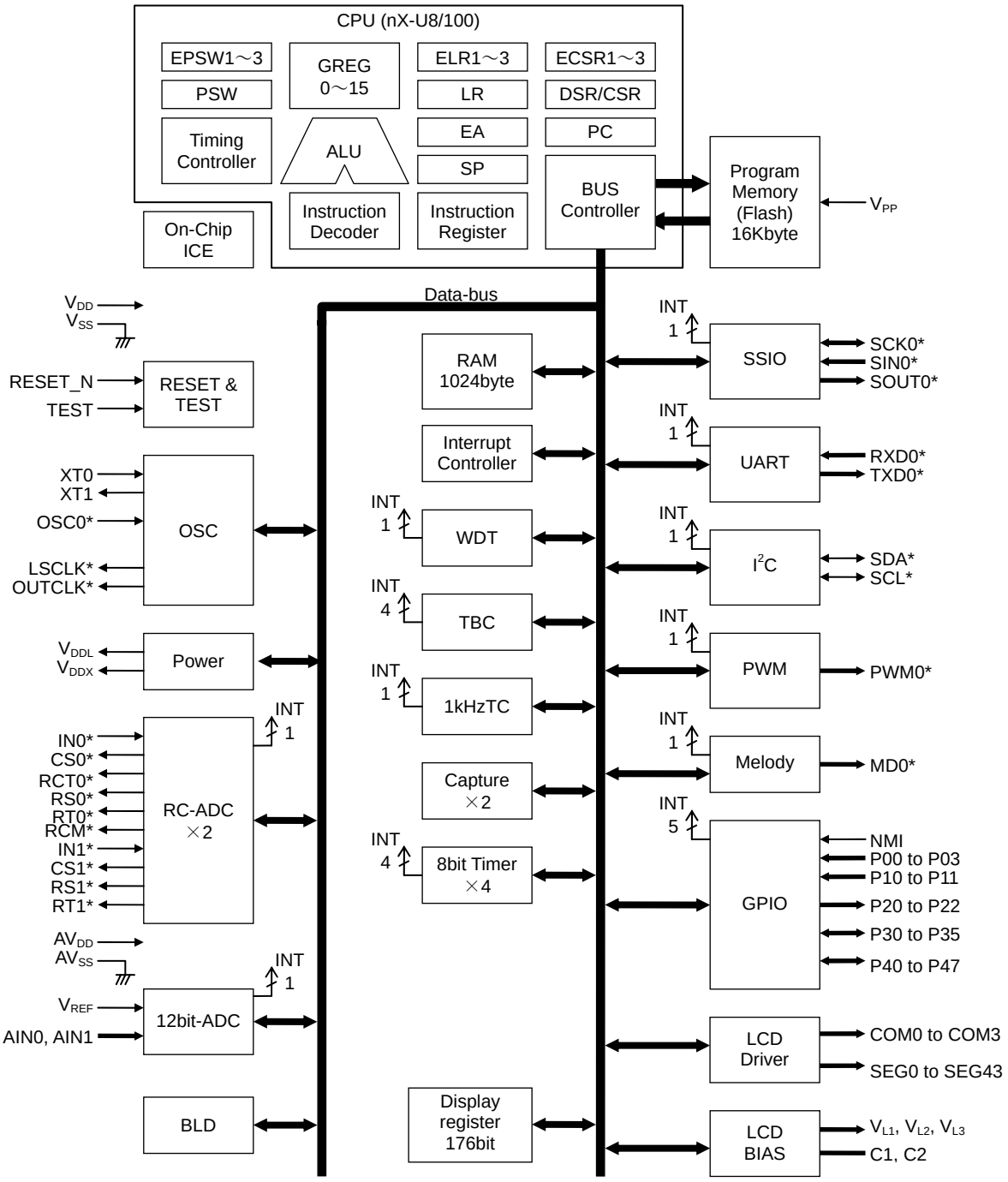
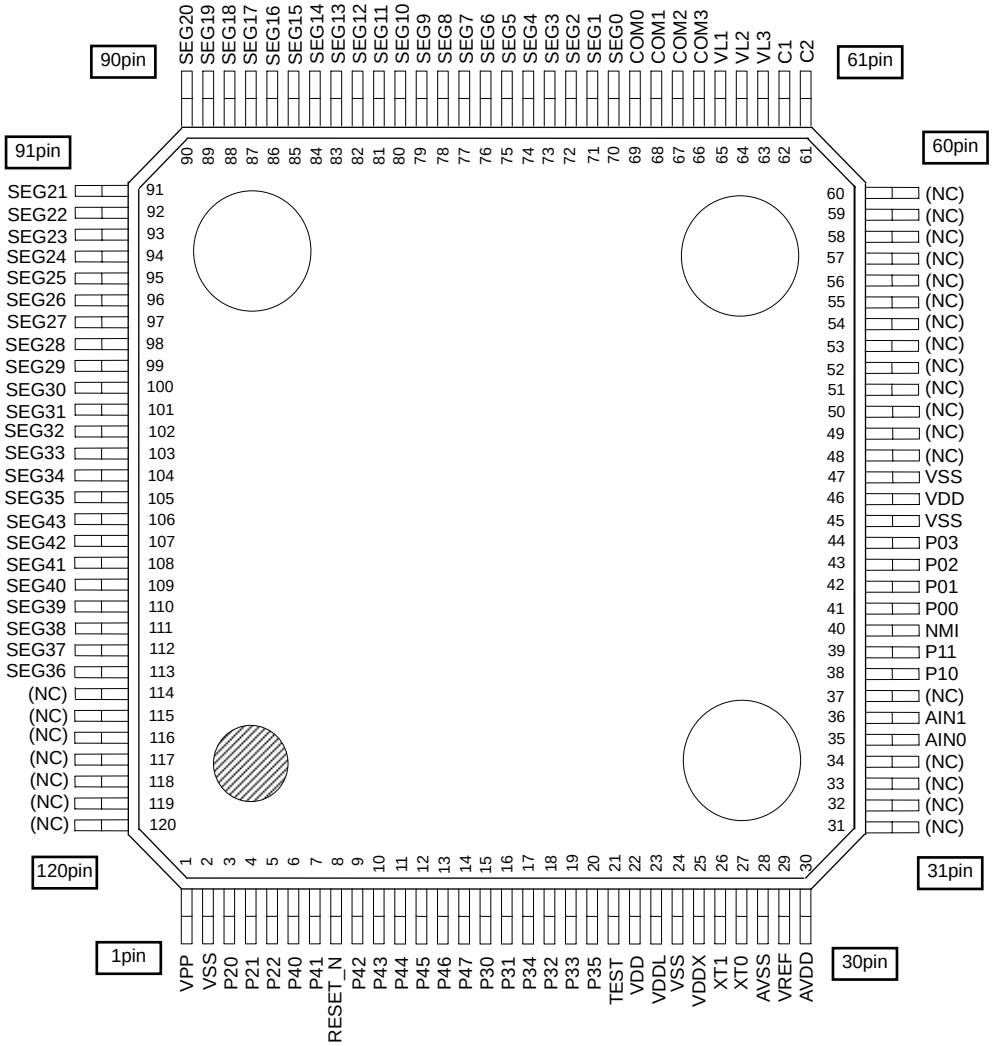


Figure 2 ML610Q412 Block Diagram

ML610Q412 TQFP120 Pin Layout

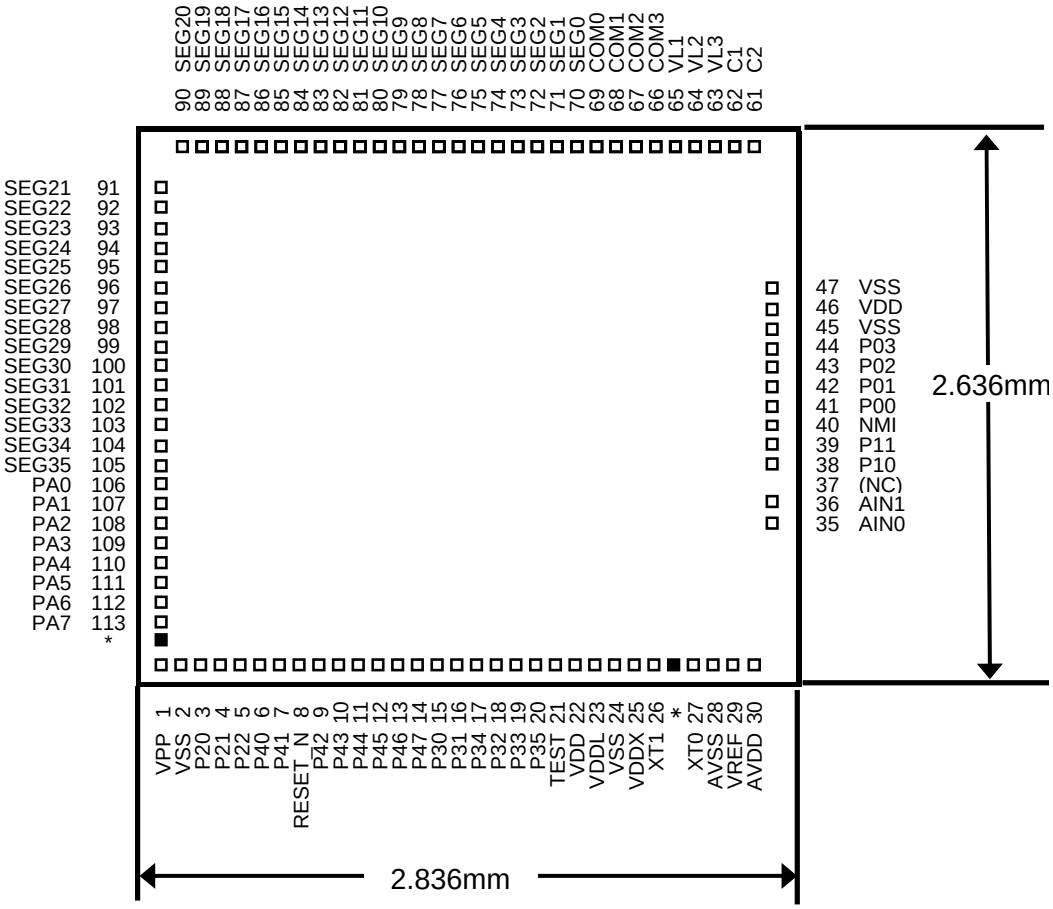


(NC): No Connection

Note:
The assignment of the P30 to P35 are not in order.

Figure 4 ML610Q412 TQFP120 Pin Configuration

ML610Q411 Chip Pin Layout & Dimension



* Dummy pad
Note: These dummy pads are visible and do have any function, they are placed for a mechanical evaluation in LAPIS Semiconductor. Please do NOT implement wire-bonding to the dummy pad.

Chip size:	2.836mm x 2.636mm
PAD count:	95 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 5 ML610Q411 Chip Layout & Dimension

ML610Q411 Pad Coordinates

Table 1 ML610Q411 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	VPP	-1230	-1212	51	(NC)	-	-	101	SEG31	-1312	160
2	VSS	-1150	-1212	52	(NC)	-	-	102	SEG32	-1312	80
3	P20	-1070	-1212	53	(NC)	-	-	103	SEG33	-1312	0
4	P21	-990	-1212	54	(NC)	-	-	104	SEG34	-1312	-80
5	P22	-910	-1212	55	(NC)	-	-	105	SEG35	-1312	-160
6	P40	-830	-1212	56	(NC)	-	-	106	PA0	-1312	-240
7	P41	-750	-1212	57	(NC)	-	-	107	PA1	-1312	-320
8	RESET_N	-670	-1212	58	(NC)	-	-	108	PA2	-1312	-400
9	P42	-590	-1212	59	(NC)	-	-	109	PA3	-1312	-480
10	P43	-510	-1212	60	(NC)	-	-	110	PA4	-1312	-560
11	P44	-430	-1212	61	C2	1220	1212	111	PA5	-1312	-640
12	P45	-350	-1212	62	C1	1140	1212	112	PA6	-1312	-720
13	P46	-270	-1212	63	VL3	1060	1212	113	PA7	-1312	-800
14	P47	-190	-1212	64	VL2	980	1212	--	Dummy	-1312	-908
15	P30	-110	-1212	65	VL1	900	1212				
16	P31	-30	-1212	66	COM3	820	1212				
17	P34	50	-1212	67	COM2	740	1212				
18	P32	130	-1212	68	COM1	660	1212				
19	P33	210	-1212	69	COM0	580	1212				
20	P35	290	-1212	70	SEG0	500	1212				
21	TEST	370	-1212	71	SEG1	420	1212				
22	VDD	450	-1212	72	SEG2	340	1212				
23	VDDL	530	-1212	73	SEG3	260	1212				
24	VSS	610	-1212	74	SEG4	180	1212				
25	VDDX	690	-1212	75	SEG5	100	1212				
26	XT1	770	-1212	76	SEG6	20	1212				
-	Dummy	850	-1212	77	SEG7	-60	1212				
27	XT0	930	-1212	78	SEG8	-140	1212				
28	AVSS	1030	-1212	79	SEG9	-220	1212				
29	VREF	1110	-1212	80	SEG10	-300	1212				
30	AVDD	1190	-1212	81	SEG11	-380	1212				
31	(NC)	-	-	82	SEG12	-460	1212				
32	(NC)	-	-	83	SEG13	-540	1212				
33	(NC)	-	-	84	SEG14	-620	1212				
34	(NC)	-	-	85	SEG15	-700	1212				
35	AIN0	1312	-522	86	SEG16	-780	1212				
36	AIN1	1312	-350	87	SEG17	-860	1212				
37	(NC)	-	-	88	SEG18	-940	1212				
38	P10	1312	-210	89	SEG19	-1020	1212				
39	P11	1312	-130	90	SEG20	-1100	1212				
40	NMI	1312	-50	91	SEG21	-1312	960				
41	P00	1312	30	92	SEG22	-1312	880				
42	P01	1312	110	93	SEG23	-1312	800				
43	P02	1312	190	94	SEG24	-1312	720				
44	P03	1312	270	95	SEG25	-1312	640				
45	VSS	1312	350	96	SEG26	-1312	560				
46	VDD	1312	430	97	SEG27	-1312	480				
47	VSS	1312	510	98	SEG28	-1312	400				
48	(NC)	-	-	99	SEG29	-1312	320				
49	(NC)	-	-	100	SEG30	-1312	240				
50	(NC)	-	-								

ML610Q412 Pad Coordinates

Table 2 ML610Q412 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	VPP	-1230	-1212	51	(NC)	-	-	101	SEG31	-1312	160
2	VSS	-1150	-1212	52	(NC)	-	-	102	SEG32	-1312	80
3	P20	-1070	-1212	53	(NC)	-	-	103	SEG33	-1312	0
4	P21	-990	-1212	54	(NC)	-	-	104	SEG34	-1312	-80
5	P22	-910	-1212	55	(NC)	-	-	105	SEG35	-1312	-160
6	P40	-830	-1212	56	(NC)	-	-	106	SEG43	-1312	-240
7	P41	-750	-1212	57	(NC)	-	-	107	SEG42	-1312	-320
8	RESET_N	-670	-1212	58	(NC)	-	-	108	SEG41	-1312	-400
9	P42	-590	-1212	59	(NC)	-	-	109	SEG40	-1312	-480
10	P43	-510	-1212	60	(NC)	-	-	110	SEG39	-1312	-560
11	P44	-430	-1212	61	C2	1220	1212	111	SEG38	-1312	-640
12	P45	-350	-1212	62	C1	1140	1212	112	SEG37	-1312	-720
13	P46	-270	-1212	63	VL3	1060	1212	113	SEG36	-1312	-800
14	P47	-190	-1212	64	VL2	980	1212	-	Dummy	-1312	-908
15	P30	-110	-1212	65	VL1	900	1212				
16	P31	-30	-1212	66	COM3	820	1212				
17	P34	50	-1212	67	COM2	740	1212				
18	P32	130	-1212	68	COM1	660	1212				
19	P33	210	-1212	69	COM0	580	1212				
20	P35	290	-1212	70	SEG0	500	1212				
21	TEST	370	-1212	71	SEG1	420	1212				
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25	VDDX	690	-1212	75	SEG5	100	1212				
26	XT1	770	-1212	76	SEG6	20	1212				
-	Dummy	850	-1212	77	SEG7	-60	1212				
27	XT0	930	-1212	78	SEG8	-140	1212				
28	AVSS	1030	-1212	79	SEG9	-220	1212				
29	VREF	1110	-1212	80	SEG10	-300	1212				
30	AVDD	1190	-1212	81	SEG11	-380	1212				
31	(NC)	-	-	82	SEG12	-460	1212				
32	(NC)	-	-	83	SEG13	-540	1212				
33	(NC)	-	-	84	SEG14	-620	1212				
34	(NC)	-	-	85	SEG15	-700	1212				
35	AIN0	1312	-522	86	SEG16	-780	1212				
36	AIN1	1312	-350	87	SEG17	-860	1212				
37	(NC)	-	-	88	SEG18	-940	1212				
38	P10	1312	-210	89	SEG19	-1020	1212				
39	P11	1312	-130	90	SEG20	-1100	1212				
40	NMI	1312	-50	91	SEG21	-1312	960				
41	P00	1312	30	92	SEG22	-1312	880				
42	P01	1312	110	93	SEG23	-1312	800				
43	P02	1312	190	94	SEG24	-1312	720				
44	P03	1312	270	95	SEG25	-1312	640				
45	VSS	1312	350	96	SEG26	-1312	560				
46	VDD	1312	430	97	SEG27	-1312	480				
47	VSS	1312	510	98	SEG28	-1312	400				
48	(NC)	-	-	99	SEG29	-1312	320				
49	(NC)	-	-	100	SEG30	-1312	240				
50	(NC)	-	-								

PAD No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
110	PA4(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG39(*2)	O	LCD segment pin	—	—	—	—	—	—
111	PA5(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG38(*2)	O	LCD segment pin	—	—	—	—	—	—
112	PA6(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG37(*2)	O	LCD segment pin	—	—	—	—	—	—
113	PA7(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG36(*2)	O	LCD segment pin	—	—	—	—	—	—
69	COM0	O	LCD common pin	—	—	—	—	—	—
68	COM1	O	LCD common pin	—	—	—	—	—	—
67	COM2	O	LCD common pin	—	—	—	—	—	—
66	COM3	O	LCD common pin	—	—	—	—	—	—
70	SEG0	O	LCD segment pin	—	—	—	—	—	—
71	SEG1	O	LCD segment pin	—	—	—	—	—	—
72	SEG2	O	LCD segment pin	—	—	—	—	—	—
73	SEG3	O	LCD segment pin	—	—	—	—	—	—
74	SEG4	O	LCD segment pin	—	—	—	—	—	—
75	SEG5	O	LCD segment pin	—	—	—	—	—	—
76	SEG6	O	LCD segment pin	—	—	—	—	—	—
77	SEG7	O	LCD segment pin	—	—	—	—	—	—
78	SEG8	O	LCD segment pin	—	—	—	—	—	—
79	SEG9	O	LCD segment pin	—	—	—	—	—	—
80	SEG10	O	LCD segment pin	—	—	—	—	—	—
81	SEG11	O	LCD segment pin	—	—	—	—	—	—
82	SEG12	O	LCD segment pin	—	—	—	—	—	—
83	SEG13	O	LCD segment pin	—	—	—	—	—	—
84	SEG14	O	LCD segment pin	—	—	—	—	—	—
85	SEG15	O	LCD segment pin	—	—	—	—	—	—
86	SEG16	O	LCD segment pin	—	—	—	—	—	—
87	SEG17	O	LCD segment pin	—	—	—	—	—	—
88	SEG18	O	LCD segment pin	—	—	—	—	—	—
89	SEG19	O	LCD segment pin	—	—	—	—	—	—
90	SEG20	O	LCD segment pin	—	—	—	—	—	—
91	SEG21	O	LCD segment pin	—	—	—	—	—	—
92	SEG22	O	LCD segment pin	—	—	—	—	—	—
93	SEG23	O	LCD segment pin	—	—	—	—	—	—
94	SEG24	O	LCD segment pin	—	—	—	—	—	—
95	SEG25	O	LCD segment pin	—	—	—	—	—	—
96	SEG26	O	LCD segment pin	—	—	—	—	—	—
97	SEG27	O	LCD segment pin	—	—	—	—	—	—
98	SEG28	O	LCD segment pin	—	—	—	—	—	—
99	SEG29	O	LCD segment pin	—	—	—	—	—	—
100	SEG30	O	LCD segment pin	—	—	—	—	—	—
101	SEG31	O	LCD segment pin	—	—	—	—	—	—
102	SEG32	O	LCD segment pin	—	—	—	—	—	—
103	SEG33	O	LCD segment pin	—	—	—	—	—	—
104	SEG34	O	LCD segment pin	—	—	—	—	—	—
105	SEG35	O	LCD segment pin	—	—	—	—	—	—

(*1) Pins on ML610Q411.
(*2) Pins on ML610Q412.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} as required.	—	—
OSC0	I	High-speed external clock input pin. This pin is used as the secondary function of the P10.	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port. These pins are for the ML610Q411, but are not provided in the ML610Q412.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	O	I^2C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T02P0CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/ negative
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13P1CK	I	External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Buzzer				
BZ0	O	Buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/ negative
LED drive				
LED0-2	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

Table 3 Termination of Unused Pins

Pin	Recommended pin termination
V_{PP}	Open
AV_{DD}	V_{SS}
AV_{SS}	V_{SS}
V_{REF}	V_{SS}
AIN0, AIN1	Open
V_{L1}, V_{L2}, V_{L3}	Open
C1, C2	Open
RESET_N	Open
TEST	Open
NMI	Open
P00 to P03	V_{DD} or V_{SS}
P10 to P11	V_{DD}
P20 to P22	Open
P30 to P35	Open
P40 to P47	Open
PA0 to PA7	Open
COM0 to 3	Open
SEG0 to 43	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	AV_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 3	V_{PP}	Ta = 25°C	–0.3 to +9.5	V
Power supply voltage 4	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 5	V_{DDX}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 6	V_{L1}	Ta = 25°C	–0.3 to +1.75	V
Power supply voltage 7	V_{L2}	Ta = 25°C	–0.3 to +3.5	V
Power supply voltage 8	V_{L3}	Ta = 25°C	–0.3 to +5.25	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–A, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	1.25	W
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	ML610Q411, ML610Q412,	–20 to +70	°C
		ML610Q411P, ML610Q411PA, ML610Q412P	–40 to +85	
Operating voltage	V_{DD}	—	1.1 to 3.6	V
	AV_{DD}	—	2.2 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.1 to 3.6V	30k to 36k 46.9k to 78.1k	Hz
		V_{DD} = 1.3 to 3.6V	30k to 625k	
			23k to 625k	
Capacitor externally connected to V_{DDL} pin	C_{L0}	—	1.0±30%	µF
	C_{L1}	—	0.1±30%	
Capacitor externally connected to V_{DDX} pin	C_X	—	0.1±30%	µF
Capacitors externally connected to $V_{L1, 2, 3}$ pins	$C_{1, 2, 3}$	—	1.0±30%	µF
Capacitors externally connected across C1 and C2 pins	C_{12}	—	1.0±30%	µF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f_{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R_L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor [*1]	C_{DL}/C_{GL}	C_L=6pF of crystal oscillation [*2]	—	0	—	pF
		C_L=9pF of crystal oscillation	—	6	—	
		C_L=12pF of crystal oscillation	—	12	—	
	C_{GH}	—	—	24	—	

[*1]: The external C_{DL} and C_{GL} need to be adjusted in consideration of variation of internal loading capacitance C_D and C_G, and other additional capacitance such as PCB layout.

[*2]: When using a crystal oscillator C_L = 6pF, there is a possibility that can not be adjusted by external C_{DL} and C_{GL}.

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase[*1]	2.75 to 3.6	V
	V_{DDL}	At write/erase[*1]	2.5 to 2.75	
	V_{PP}	At write/erase[*1]	7.7 to 8.3	
Write cycles	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

[*1]: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and eraseing Flash ROM. V_{PP} pin has an internal pulldown resister.

DC CHARACTERISTICS (3/5)

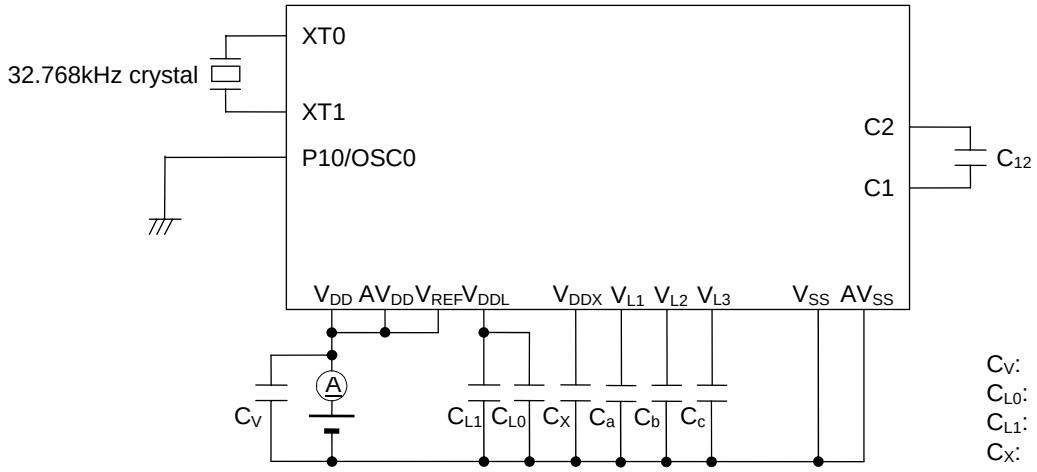
(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified) (3/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	V_{DD} = 1.35 to 3.6V	LD3–0 = 0H	Typ. –2%	1.35	Typ. +2%	V	1
			LD3–0 = 1H		1.4			
			LD3–0 = 2H		1.45			
			LD3–0 = 3H		1.5			
			LD3–0 = 4H		1.6			
			LD3–0 = 5H		1.7			
			LD3–0 = 6H		1.8			
			LD3–0 = 7H		1.9			
			LD3–0 = 8H		2.0			
			LD3–0 = 9H		2.1			
			LD3–0 = 0AH		2.2			
			LD3–0 = 0BH		2.3			
			LD3–0 = 0CH		2.4			
			LD3–0 = 0DH		2.5			
			LD3–0 = 0EH		2.7			
			LD3–0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	V_{DD} = 1.35 to 3.6V		—	0	—	%/°C	
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed RC500kHz oscillation: stopped.	Ta= 25°C	—	0.15	0.5	μA	1
			*5	—	—	2.5		
Supply current 2	IDD2	CPU: In HALT state (LTBC and WDT are Operating. Low speed oscillation stop detector is Stopped).*3*4 High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Stopped.	Ta= 25°C	—	0.5	1.3	μA	
			*5	—	—	3.5		
Supply current 3	IDD3	CPU: In HALT state (LTBC and WDT are Operating. Low speed oscillation stop detector is Stopped).*3 High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	1.28	1.6	μA	
			*5	—	—	11		
Supply current 4	IDD4	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	5.5	7	μA	
			*5	—	—	12		
Supply current 5	IDD5	CPU: In RC 500kHz operating state. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	80	90	μA	1
			*5	—	—	100		
Supply current 6	IDD6	CPU: In RC 500kHz operating state.*2 LCD and BIAS circuits: Operating. *2 A/D: In operating state. V_{DD} = AV_{DD} = 3.0V	Ta= 25°C	—	0.4	0.5	mA	
			*5	—	—	0.6		

*1: When the CPU operating rate is 100% (No HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.
*4 : Significant bits of BLKCON0~BLKCON4 registers are all "1".
*5 : Recommended operating temperature (Ta = –40 to +85°C for P version, Ta = –20 to +70°C for non-P version)

MEASURING CIRCUITS

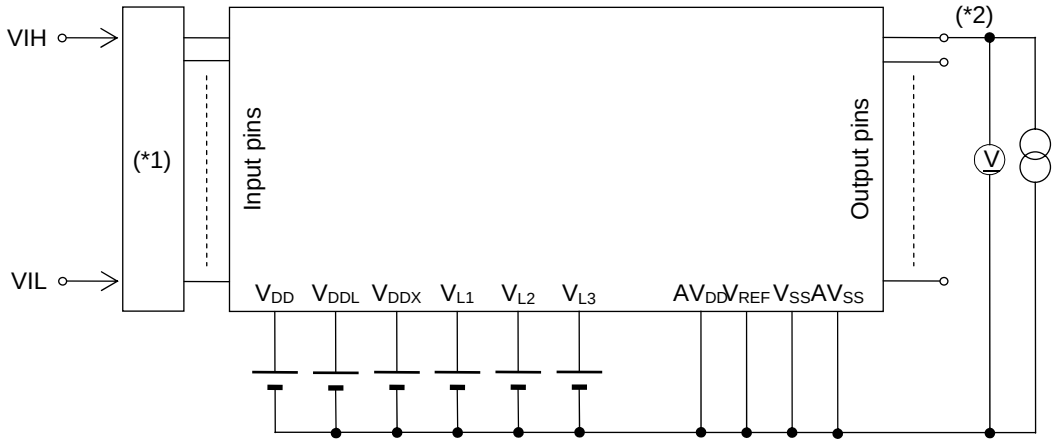
MEASURING CIRCUIT 1



C_V:	1µF
C_{L0}:	1µF
C_{L1}:	0.1µF
C_X:	0.1µF
C_a,C_b,C_c,C_d:	1µF
C_{12},C_{34}:	1µF

32.768kHz crystal:
C-001R (Epson Toyocom)

MEASURING CIRCUIT 2

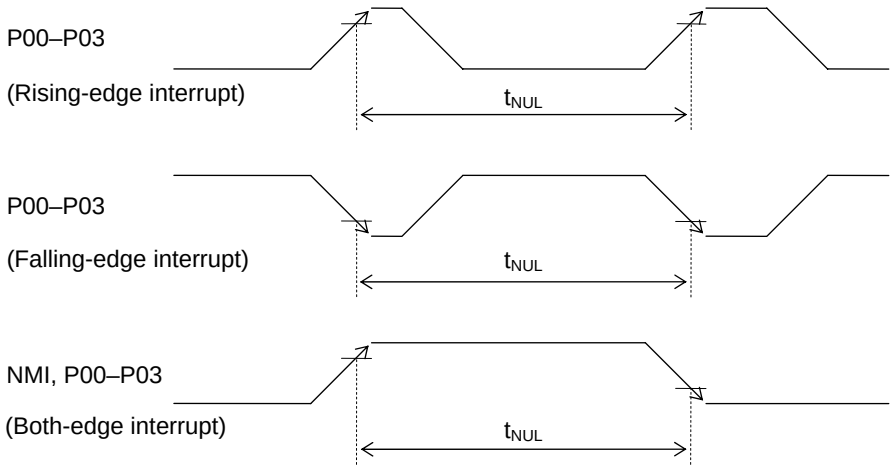


(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	µs

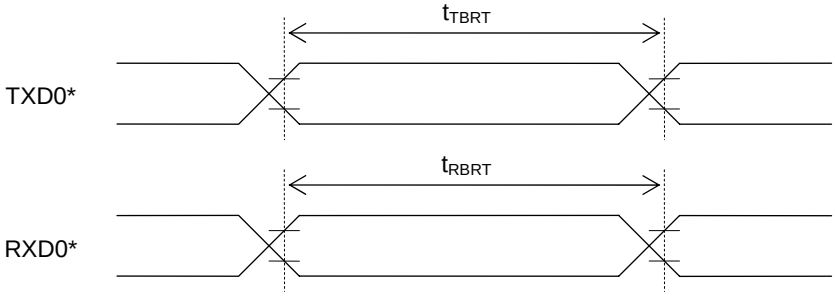


AC CHARACTERISTICS (Serial Port)

(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*[1]	—	s
Receive baud rate	t_{RBRT}	—	BRT*[1] –3%	BRT*[1]	BRT*[1] +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



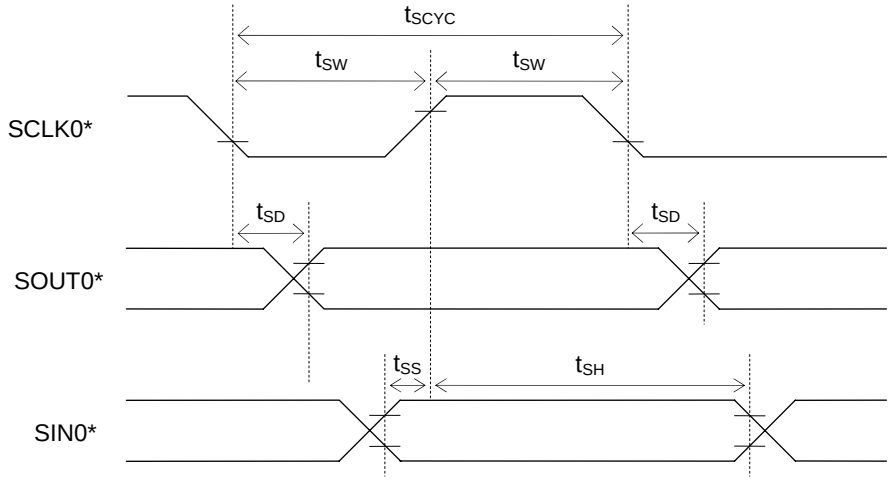
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	µs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*[1]	—	s
SCLK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	µs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*[1] ×0.4	SCLK*[1] ×0.5	SCLK*[1] ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	500	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	500	ns
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	—	500	—	—	ns
SIN input hold time	t_{SH}	—	300	—	—	ns

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)

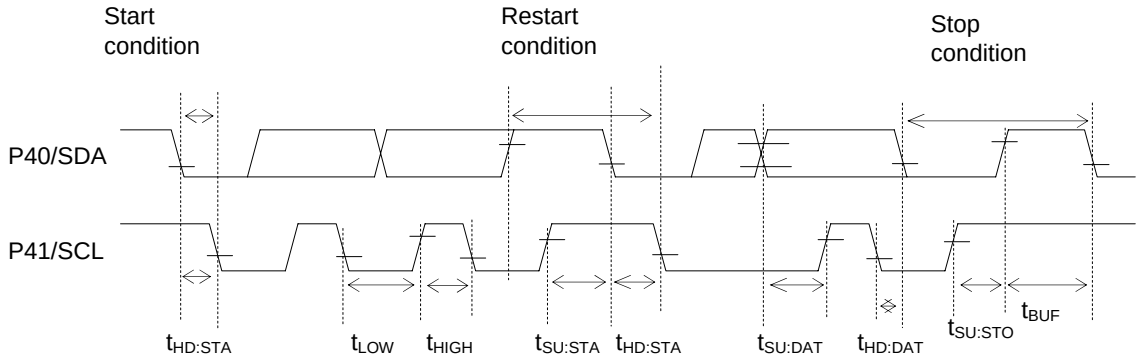


*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I^2C Bus Interface: Standard Mode)

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	—	50	—	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

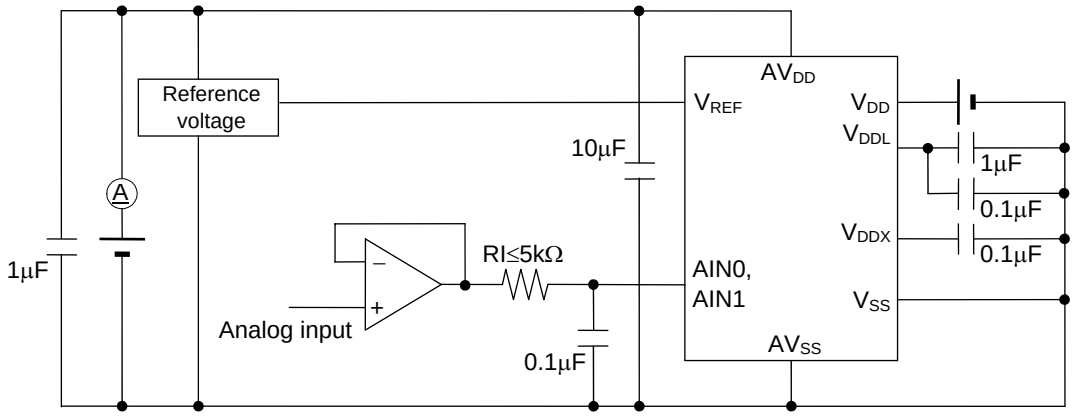


Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified)

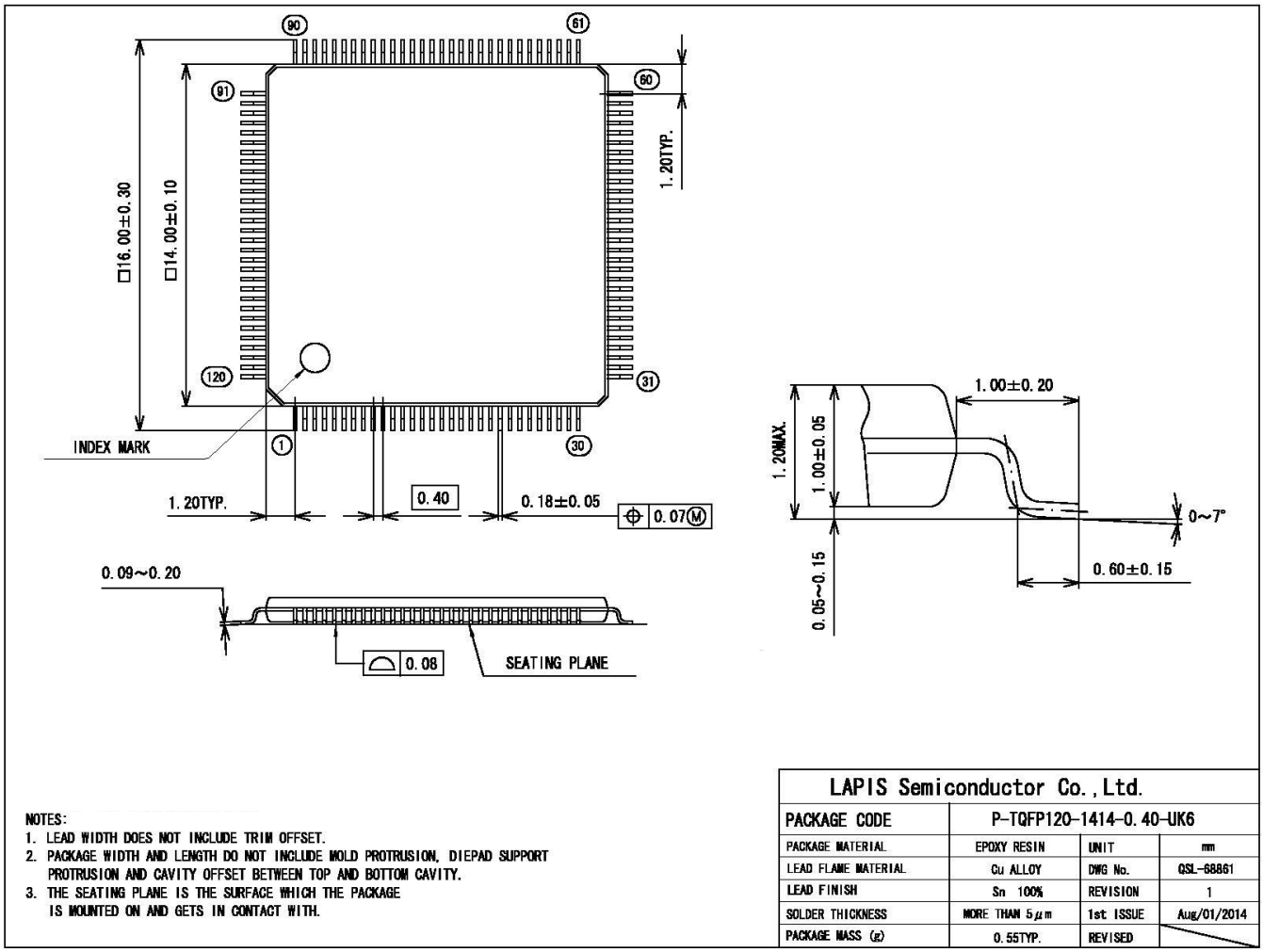
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 3.6V	–4	—	+4	LSB
		2.2V ≤ V_{REF} ≤ 2.7V	–6	—	+6	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 3.6V	–3	—	+3	
		2.2V ≤ V_{REF} ≤ 2.7V	–5	—	+5	
Zero-scale error	V_{OFF}	—	–6	—	+6	
Full-scale error	FSE	—	–6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	—	—	23*[1]	—	ϕ/CH

ϕ: Period of high-speed clock (HSCLK)
*[1]: 2ϕ / CH is required as an interval time for each conversion in the case of consecutive A/D conversion.



PACKAGE DIMENSIONS

(Unit: mm)



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP120-1414-0.40-UK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68861
LEAD FINISH	Sn 100%	REVISION	1
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Aug/01/2014
PACKAGE MASS (g)	0.55TYP.	REVISED	

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q411-01	Jul.17,2010	–	–	Formally edition 1
FEDL610Q411-02	Mar.23,2011	3, 4, 21	3, 4, 21	Add the explanation of ML610Q411PC.
		34	34	Replace the package dimension (Only the format is changed. Package size and material are not changed.)
FEDL610Q411-03	Apr.15,2015	All	All	Change header and footer.
		1~3 5 7 9 11 13 15 16 18~20 21 23 24 25 27	1~3 5 7 9 11 13 15 16 18~20 22 24 25 26 27	Delete ML610Q415 and ML610Q411PC
		4	4	Change from "Shipment" to "Product name ― Supported Function"
		–	21	Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS
		21	22	Change "RESET" to "Reset pulse width (P_{RST}) " and "Power-on reset activation power rise time (T_{POR}) ".
		36	36	Change description in Note.
FEDL610Q411-04	July.13,2015	14	14	Corrected a typo. -PAD No,"37" is corrected to "36". -PAD No,"36" is corrected to "35".