Rohm Semiconductor - ML610Q412-NNNTBZ03A7 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	625kHz
Connectivity	I²C, SSP, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 2x12b, 2x24b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q412-nnntbz03a7

- Frame frequency selecable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
- Bias voltage multiplying clock selectable (8 types)
- Contrast adjustment (32 steps)
- LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow

- Battery Level Detector
  - Threshold voltages: One of 16 levels
  - Accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed crystal oscillation clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (500 kHz)
    External clock (500kH or less)
  - High-speed Clock gear: 1/2(250kHz), 1/4(125kHz), 1/8(62.5kHz: default)
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, External clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
  - Block Control Function: Resets and completely turns circuits of unused peripherals off.

- Guaranteed operating range
  - Operating temperature: –20°C to +70°C (P version: –40°C to +85°C)
  - Operating voltage: V_{DD} = 1.1V to 3.6V, AV_{DD} = 2.2V to 3.6V

• Product name – Supported Function

The line-up of the ML610Q411 and the ML610Q412 is below.

- Chip (Die) -	ROM type	Low-speed oscillation stop detect reset	Operating temperature	Product availability
ML610Q411-xxxWA	Flash ROM	Yes	-20°C to +70°C	Yes
ML610Q411P-xxxWA	Flash ROM	Yes	-40°C to +85°C	Yes
ML610Q411PA-xxxWA	Flash ROM	Selectable to disable always	-40°C to +85°C	Yes
ML610Q412-xxxWA	Flash ROM	Yes	-20°C to +70°C	Yes
ML610Q412P-xxxWA	Flash ROM	Yes	-40°C to +85°C	Yes

-120-pin plastic TQFP -	ROM type	Low-speed oscillation stop detect reset	Operating temperature	Product availability
ML610Q411-xxxTB	Flash ROM	Yes	-20°C to +70°C	Yes
ML610Q411P-xxxTB	Flash ROM	Yes	-40°C to +85°C	Yes
ML610Q411PA-xxxTB	Flash ROM	Selectable to disable always	-40°C to +85°C	Yes
ML610Q412-xxxTB	Flash ROM	Yes	-20°C to +70°C	Yes
ML610Q412P-xxxTB	Flash ROM	Yes	-40°C to +85°C	Yes

xxx : ROM code number (xxx of the blank product is NNN)

Q : Flash ROM version

P : Wide range temperature version

A: Low-speed clock oscillation stop detection reset is selectable to disable always (See chapter3 and chapter4 in the user's manual for more detail).

WA : Chip (Die)

TB : TQFP

BLOCK DIAGRAM

ML610Q411 Block Diagram

Figure 1 show the block diagram of the ML610Q411.
"*" indicates the secondary function of each port.

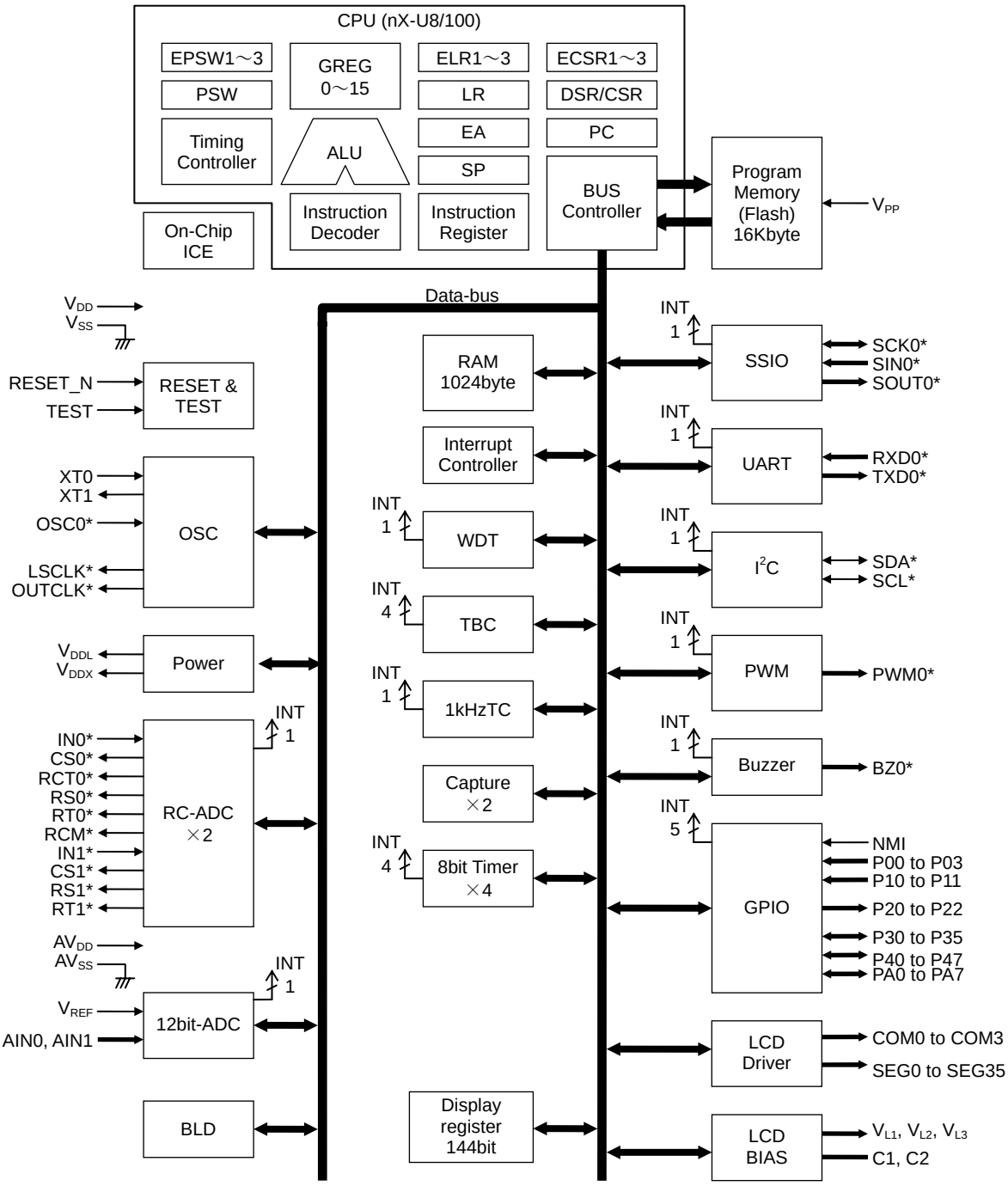


Figure 1 ML610Q411 Block Diagram

ML610Q412 Block Diagram

Figure 2 show the block diagram of the ML610Q412.
"*" indicates the secondary function of each port.

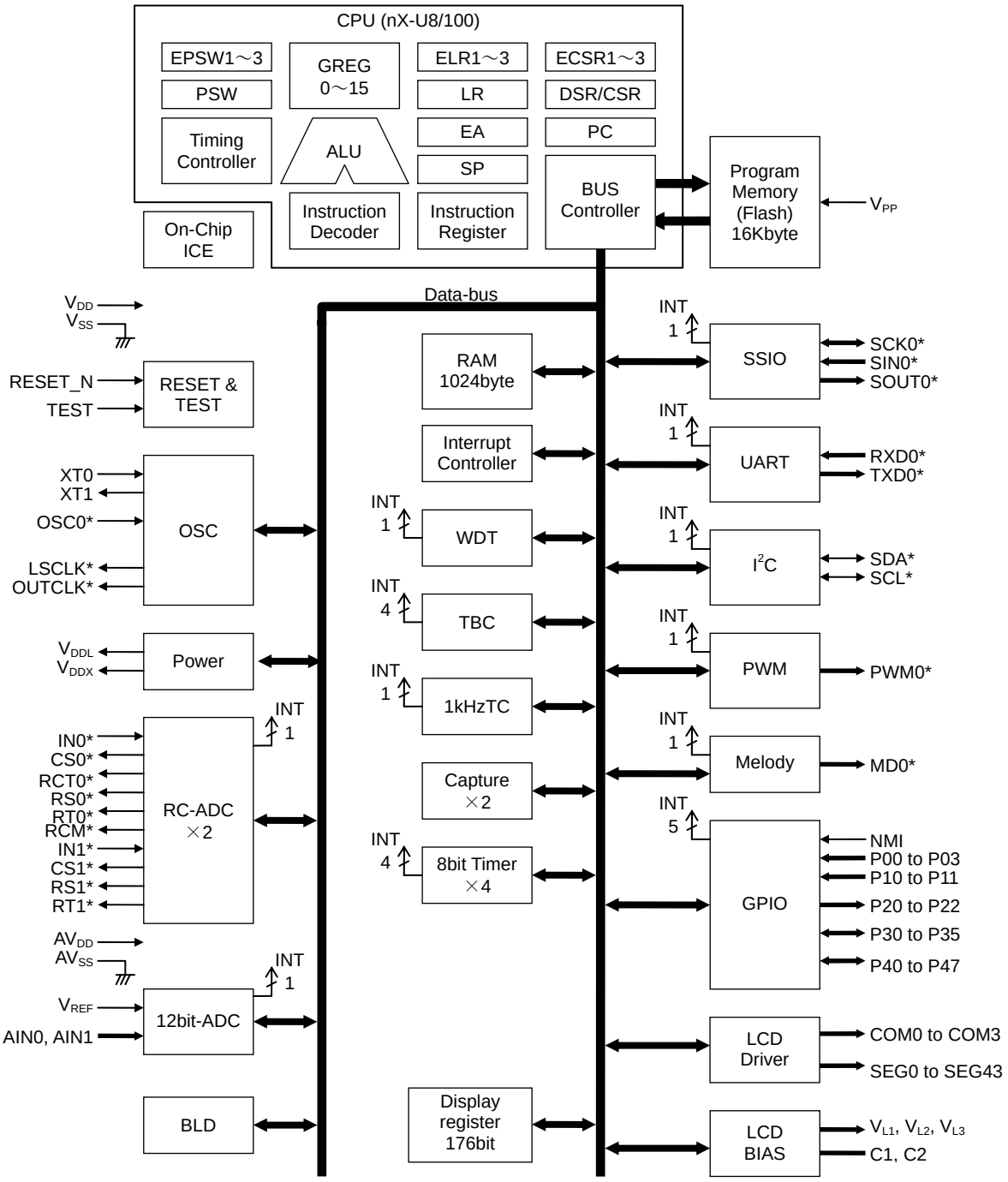
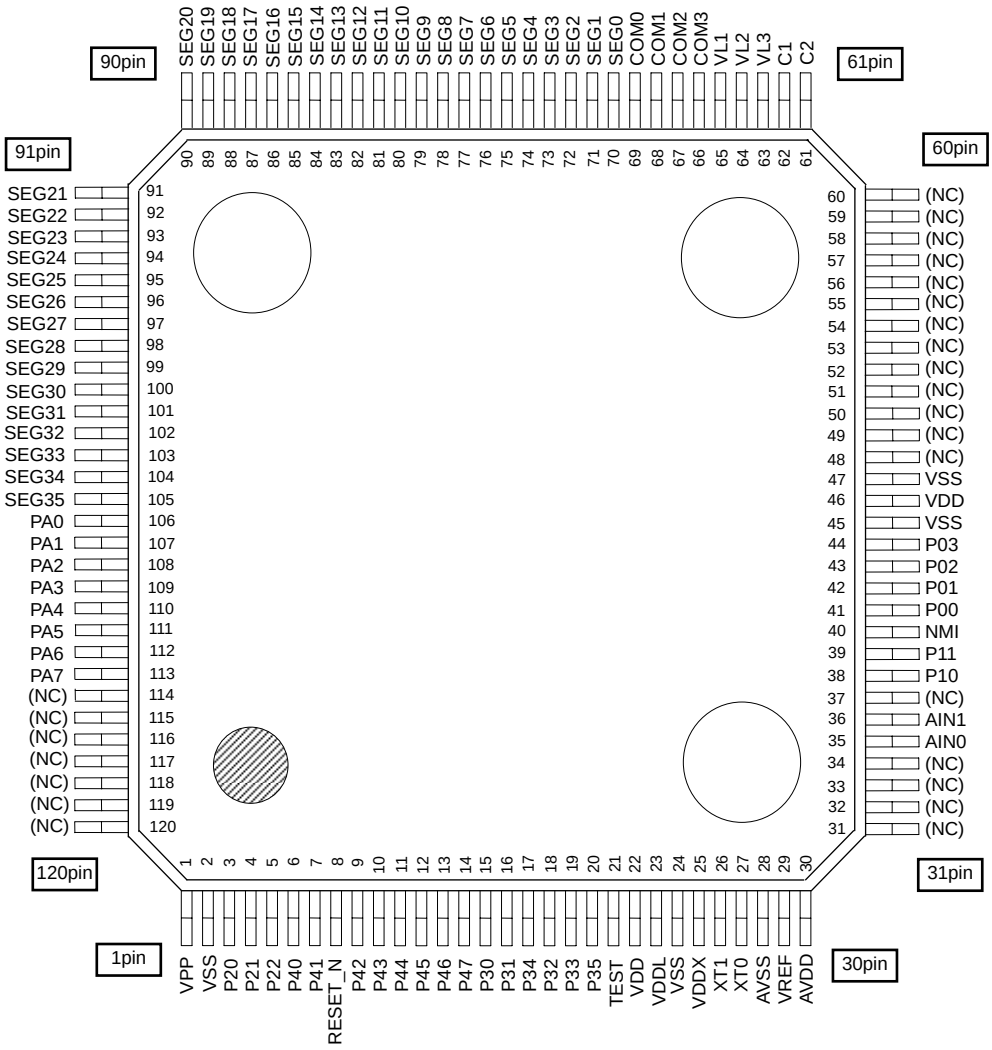


Figure 2 ML610Q412 Block Diagram

PIN CONFIGURATION

ML610Q411 TQFP120 Pin Layout

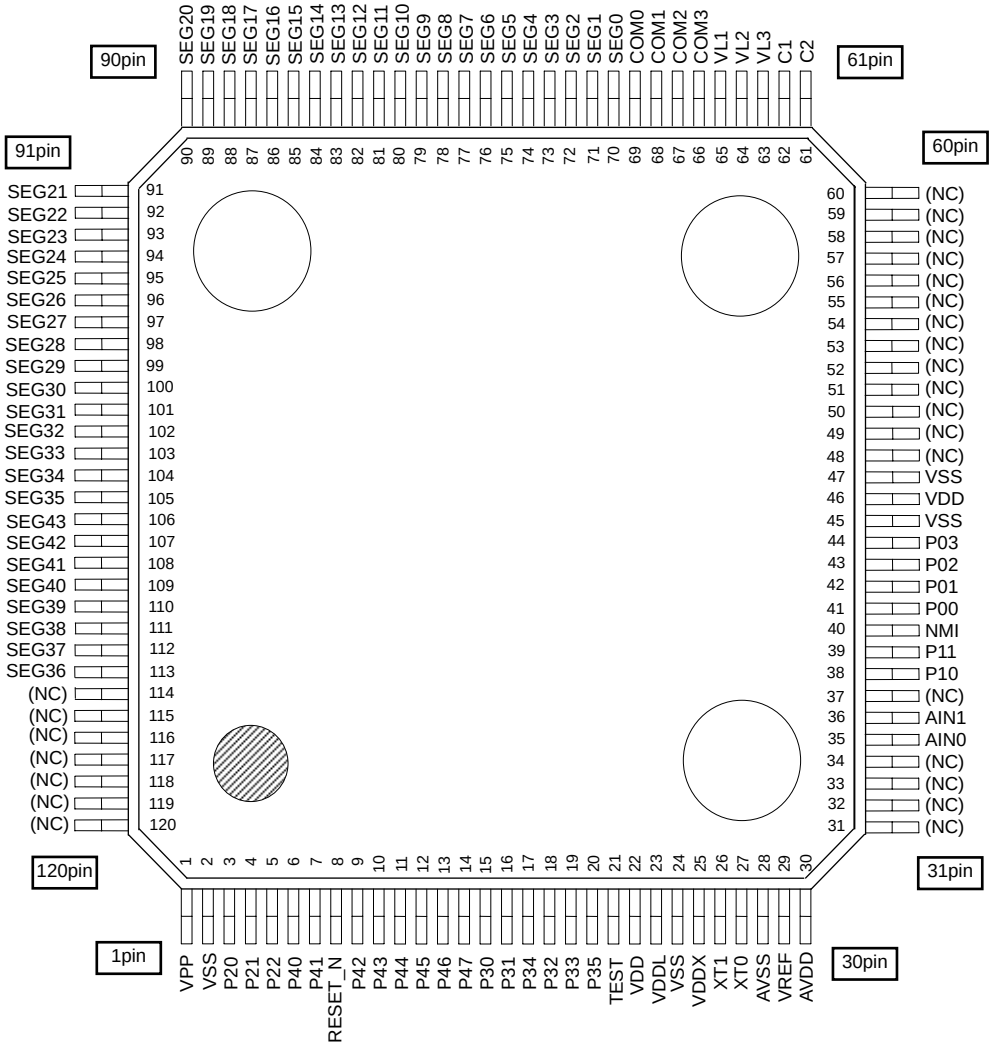


(NC): No Connection

Note:
The assignment of the P30 to P35 are not in order.

Figure 3 ML610Q411 TQFP120 Pin Configuration

ML610Q412 TQFP120 Pin Layout

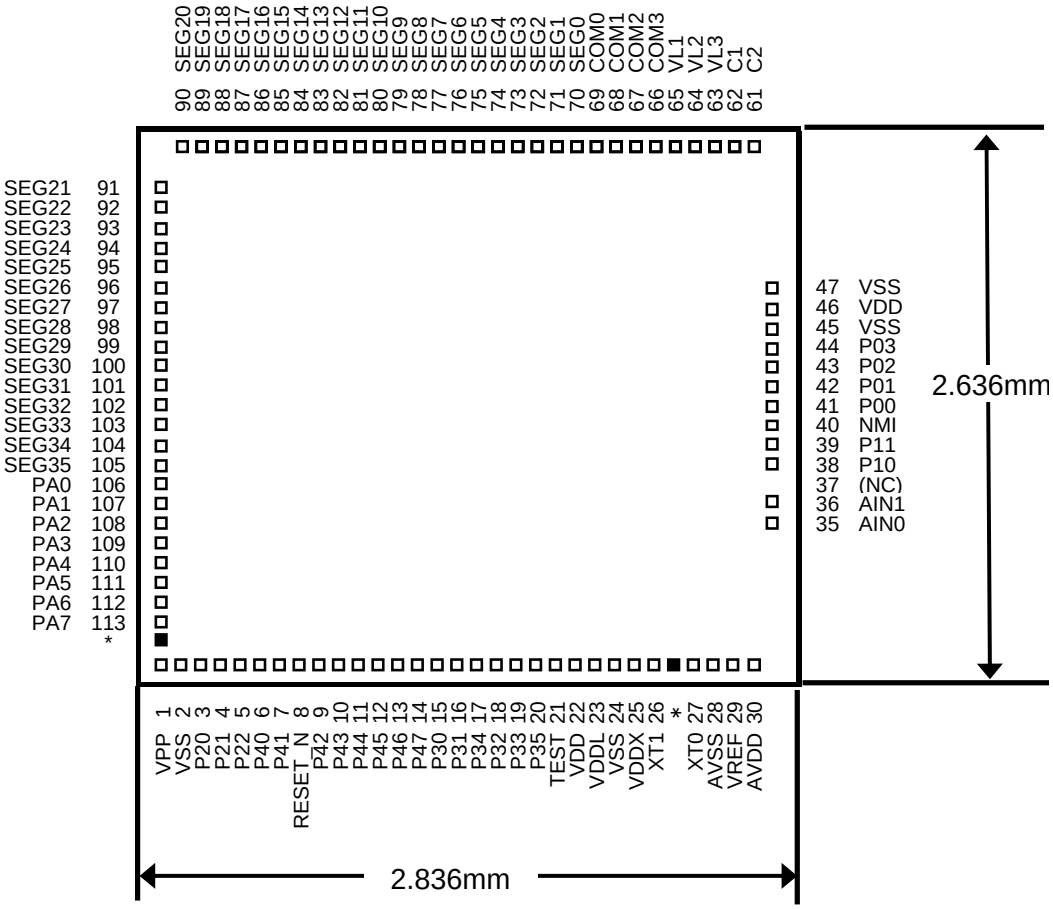


(NC): No Connection

Note:
The assignment of the P30 to P35 are not in order.

Figure 4 ML610Q412 TQFP120 Pin Configuration

ML610Q411 Chip Pin Layout & Dimension



* Dummy pad
Note: These dummy pads are visible and do have any function, they are placed for a mechanical evaluation in LAPIS Semiconductor. Please do NOT implement wire-bonding to the dummy pad.

Chip size:	2.836mm x 2.636mm
PAD count:	95 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 5 ML610Q411 Chip Layout & Dimension

ML610Q411 Pad Coordinates

Table 1 ML610Q411 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	VPP	-1230	-1212	51	(NC)	-	-	101	SEG31	-1312	160
2	VSS	-1150	-1212	52	(NC)	-	-	102	SEG32	-1312	80
3	P20	-1070	-1212	53	(NC)	-	-	103	SEG33	-1312	0
4	P21	-990	-1212	54	(NC)	-	-	104	SEG34	-1312	-80
5	P22	-910	-1212	55	(NC)	-	-	105	SEG35	-1312	-160
6	P40	-830	-1212	56	(NC)	-	-	106	PA0	-1312	-240
7	P41	-750	-1212	57	(NC)	-	-	107	PA1	-1312	-320
8	RESET_N	-670	-1212	58	(NC)	-	-	108	PA2	-1312	-400
9	P42	-590	-1212	59	(NC)	-	-	109	PA3	-1312	-480
10	P43	-510	-1212	60	(NC)	-	-	110	PA4	-1312	-560
11	P44	-430	-1212	61	C2	1220	1212	111	PA5	-1312	-640
12	P45	-350	-1212	62	C1	1140	1212	112	PA6	-1312	-720
13	P46	-270	-1212	63	VL3	1060	1212	113	PA7	-1312	-800
14	P47	-190	-1212	64	VL2	980	1212	--	Dummy	-1312	-908
15	P30	-110	-1212	65	VL1	900	1212				
16	P31	-30	-1212	66	COM3	820	1212				
17	P34	50	-1212	67	COM2	740	1212				
18	P32	130	-1212	68	COM1	660	1212				
19	P33	210	-1212	69	COM0	580	1212				
20	P35	290	-1212	70	SEG0	500	1212				
21	TEST	370	-1212	71	SEG1	420	1212				
22	VDD	450	-1212	72	SEG2	340	1212				
23	VDDL	530	-1212	73	SEG3	260	1212				
24	VSS	610	-1212	74	SEG4	180	1212				
25	VDDX	690	-1212	75	SEG5	100	1212				
26	XT1	770	-1212	76	SEG6	20	1212				
-	Dummy	850	-1212	77	SEG7	-60	1212				
27	XT0	930	-1212	78	SEG8	-140	1212				
28	AVSS	1030	-1212	79	SEG9	-220	1212				
29	VREF	1110	-1212	80	SEG10	-300	1212				
30	AVDD	1190	-1212	81	SEG11	-380	1212				
31	(NC)	-	-	82	SEG12	-460	1212				
32	(NC)	-	-	83	SEG13	-540	1212				
33	(NC)	-	-	84	SEG14	-620	1212				
34	(NC)	-	-	85	SEG15	-700	1212				
35	AIN0	1312	-522	86	SEG16	-780	1212				
36	AIN1	1312	-350	87	SEG17	-860	1212				
37	(NC)	-	-	88	SEG18	-940	1212				
38	P10	1312	-210	89	SEG19	-1020	1212				
39	P11	1312	-130	90	SEG20	-1100	1212				
40	NMI	1312	-50	91	SEG21	-1312	960				
41	P00	1312	30	92	SEG22	-1312	880				
42	P01	1312	110	93	SEG23	-1312	800				
43	P02	1312	190	94	SEG24	-1312	720				
44	P03	1312	270	95	SEG25	-1312	640				
45	VSS	1312	350	96	SEG26	-1312	560				
46	VDD	1312	430	97	SEG27	-1312	480				
47	VSS	1312	510	98	SEG28	-1312	400				
48	(NC)	-	-	99	SEG29	-1312	320				
49	(NC)	-	-	100	SEG30	-1312	240				
50	(NC)	-	-								

ML610Q412 Pad Coordinates

Table 2 ML610Q412 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	VPP	-1230	-1212	51	(NC)	-	-	101	SEG31	-1312	160
2	VSS	-1150	-1212	52	(NC)	-	-	102	SEG32	-1312	80
3	P20	-1070	-1212	53	(NC)	-	-	103	SEG33	-1312	0
4	P21	-990	-1212	54	(NC)	-	-	104	SEG34	-1312	-80
5	P22	-910	-1212	55	(NC)	-	-	105	SEG35	-1312	-160
6	P40	-830	-1212	56	(NC)	-	-	106	SEG43	-1312	-240
7	P41	-750	-1212	57	(NC)	-	-	107	SEG42	-1312	-320
8	RESET_N	-670	-1212	58	(NC)	-	-	108	SEG41	-1312	-400
9	P42	-590	-1212	59	(NC)	-	-	109	SEG40	-1312	-480
10	P43	-510	-1212	60	(NC)	-	-	110	SEG39	-1312	-560
11	P44	-430	-1212	61	C2	1220	1212	111	SEG38	-1312	-640
12	P45	-350	-1212	62	C1	1140	1212	112	SEG37	-1312	-720
13	P46	-270	-1212	63	VL3	1060	1212	113	SEG36	-1312	-800
14	P47	-190	-1212	64	VL2	980	1212	-	Dummy	-1312	-908
15	P30	-110	-1212	65	VL1	900	1212				
16	P31	-30	-1212	66	COM3	820	1212				
17	P34	50	-1212	67	COM2	740	1212				
18	P32	130	-1212	68	COM1	660	1212				
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21	TEST	370	-1212	71	SEG1	420	1212				
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27	XT0	930	-1212	78	SEG8	-140	1212				
28	AVSS	1030	-1212	79	SEG9	-220	1212				
29	VREF	1110	-1212	80	SEG10	-300	1212				
30	AVDD	1190	-1212	81	SEG11	-380	1212				
31	(NC)	-	-	82	SEG12	-460	1212				
32	(NC)	-	-	83	SEG13	-540	1212				
33	(NC)	-	-	84	SEG14	-620	1212				
34	(NC)	-	-	85	SEG15	-700	1212				
35	AIN0	1312	-522	86	SEG16	-780	1212				
36	AIN1	1312	-350	87	SEG17	-860	1212				
37	(NC)	-	-	88	SEG18	-940	1212				
38	P10	1312	-210	89	SEG19	-1020	1212				
39	P11	1312	-130	90	SEG20	-1100	1212				
40	NMI	1312	-50	91	SEG21	-1312	960				
41	P00	1312	30	92	SEG22	-1312	880				
42	P01	1312	110	93	SEG23	-1312	800				
43	P02	1312	190	94	SEG24	-1312	720				
44	P03	1312	270	95	SEG25	-1312	640				
45	VSS	1312	350	96	SEG26	-1312	560				
46	VDD	1312	430	97	SEG27	-1312	480				
47	VSS	1312	510	98	SEG28	-1312	400				
48	(NC)	-	-	99	SEG29	-1312	320				
49	(NC)	-	-	100	SEG30	-1312	240				
50	(NC)	-	-								

PIN LIST

PAD No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
2, 24,45,47	V_{SS}	—	Negative power supply pin	—	—	—	—	—	—
22, 46	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
23	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
25	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
1	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
28	AV_{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
30	AV_{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
65	V_{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
64	V_{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
63	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
62	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
61	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
21	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
8	RESET_N	I	Reset input pin	—	—	—	—	—	—
27	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
26	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
29	V_{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—

PAD No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
35	AIN0	I	Successive approximation type ADC input	—	—	—	—	—	—
36	AIN1	I	Successive approximation type ADC input	—	—	—	—	—	—
40	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
41	P00/EXI0/ CAP0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—	—	—
42	P01/EXI1/ CAP1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—	—	—
43	P02/EXI2/ RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
44	P03/EXI3	I	Input port, External interrupt 3	—	—	—	—	—	—
38	P10 OSC0	I	Input port External clock input	—	—	—	—	—	—
39	P11	I	Input port	—	—	—	—	—	—
3	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
4	P21LED1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
5	P22/LED2	O	Output port	MD0	O	Melody output	—	—	—
15	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
16	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
17	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM output
18	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
19	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
20	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
6	P40	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO data input
7	P41	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO synchronous clock
9	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	I	SSIO data output
10	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
11	P44/T02P0 CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
12	P45/T13P1 CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
13	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
14	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
106	PA0(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG43(*2)	O	LCD segment pin	—	—	—	—	—	—
107	PA1(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG42(*2)	O	LCD segment pin	—	—	—	—	—	—
108	PA2(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG41(*2)	O	LCD segment pin	—	—	—	—	—	—
109	PA3(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG40(*2)	O	LCD segment pin	—	—	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} as required.	—	—
OSC0	I	High-speed external clock input pin. This pin is used as the secondary function of the P10.	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port. These pins are for the ML610Q411, but are not provided in the ML610Q412.	Primary	Positive

DC CHARACTERISTICS (1/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified) (1/5)

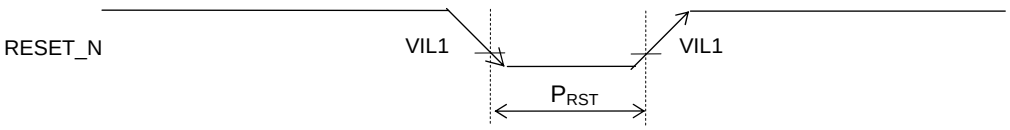
Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
500kHz RC oscillation frequency	f_{RC}	V_{DD} = 1.3 to 3.6V	Ta = 25°C	Typ. –10%	500	Typ. +10%	kHz	1
			*3	Typ. –25%	500	Typ. +25%	kHz	
Low-speed crystal oscillation start time*2	T_{XTL}	—		—	0.3	2	s	
500kHz RC oscillation start time	T_{RC}	—		—	50	500	μs	
Low-speed oscillation stop detect time*1	T_{STOP}	—		0.2	3	20	ms	
Reset pulse width	P_{RST}	—		200	—	—	μs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—		—	—	10	ms	

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

*2 : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.

*3 : Recommended operating temperature (Ta = –40 to +85°C for P version, Ta = –20 to +70°C for non-P version)

[Reset pulse width]



Reset pulse width (P_{RST})

[Power-on reset activation power rise time]

Power-on reset activation power rise time (T_{POR})

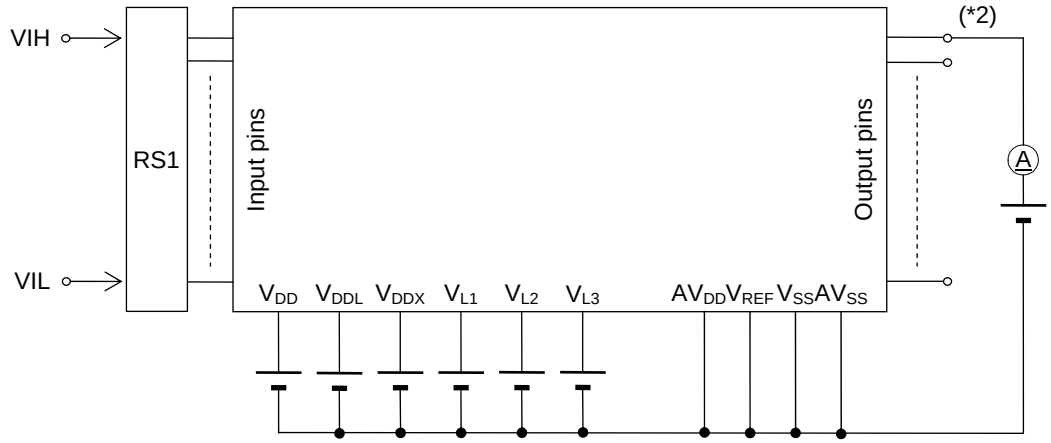
DC CHARACTERISTICS (4/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified) (4/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage 1 (P20–P22/2nd function is selected) (P30–P36) (P40–P47) (PB0–PB7)*1	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD} –0.5	—	—	V	2
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V		V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V		V_{DD} –0.3	—	—		
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.3 to 3.6V		—	—	0.5		
		IOL1 = +0.03mA, V_{DD} = 1.1 to 3.6V		—	—	0.3		
Output voltage 2 (P20–P22/2nd function is Not selected)	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD} –0.5	—	—		
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V		V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V		V_{DD} –0.3	—	—		
	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = +3mA, V_{DD} = 2.0 to 3.6V (when I^2C mode is selected)		—	—	0.4		
Output voltage 4 (COM0–3) (SEG0–35)*1 (SEG0–43) *2	VOH4	IOH4 = –0.2mA, VL1=1.2V		V_{L3} –0.2	—	—		
	VOMH4	IOMH4 = +0.2mA, VL1=1.2V		—	—	V_{L2} +0.2		
	VOM4S	IOM4S = –0.2mA, VL1=1.2V		V_{L2} –0.2	—	—		
	VOML4	IOML4 = +0.2mA, VL1=1.2V		—	—	V_{L1} +0.2		
	VOML4S	IOML4S = –0.2mA, VL1=1.2V		V_{L1} –0.2	—	—		
	VOL4	IOL4 = +0.2mA, VL1=1.2V		—	—	0.2		
Output leakage (P20–P22) (P30–P35) (P40–P47) (PA0–PA7)*1	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}		0	—	1	μA	4
	IIL1	VIL1 = V_{SS}	V_{DD} = 1.3 to 3.6V	–600	–300	-10		
			V_{DD} = 1.1 to 3.6V	–600	–300	-2		
Input current 1 (TEST)	IIH1	VIH1 = V_{DD}	V_{DD} = 1.3 to 3.6V	10	300	600		
			V_{DD} = 1.1 to 3.6V	2	300	600		
	IIL1	VIL1 = V_{ss}		-1	—	—		
Input current 2 (NMI) (P00-P03) (P10-P11) (P30-P35) (P40-P47) (PA0-PA7) *1	IIH2	VIH2 = V_{DD} (when pulled-down)	V_{DD} = 1.3 to 3.6V	0.2	30	200		
			V_{DD} = 1.1 to 3.6V	0.01	30	200		
	IIL2	VIL2 = V_{SS} (when pulled-up)	V_{DD} = 1.3 to 3.6V	–200	–30	-0.2		
			V_{DD} = 1.1 to 3.6V	–200	–30	-0.01		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		–1	—	—		

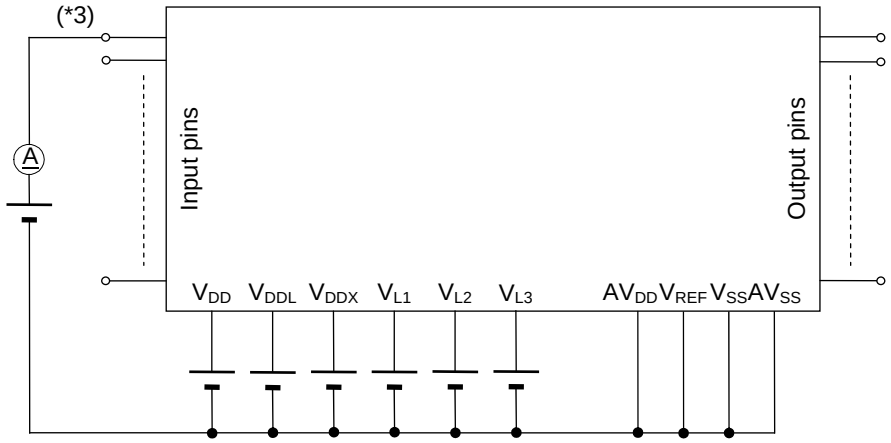
*1: ML610Q411
*2: ML610Q412

MEASURING CIRCUIT 3



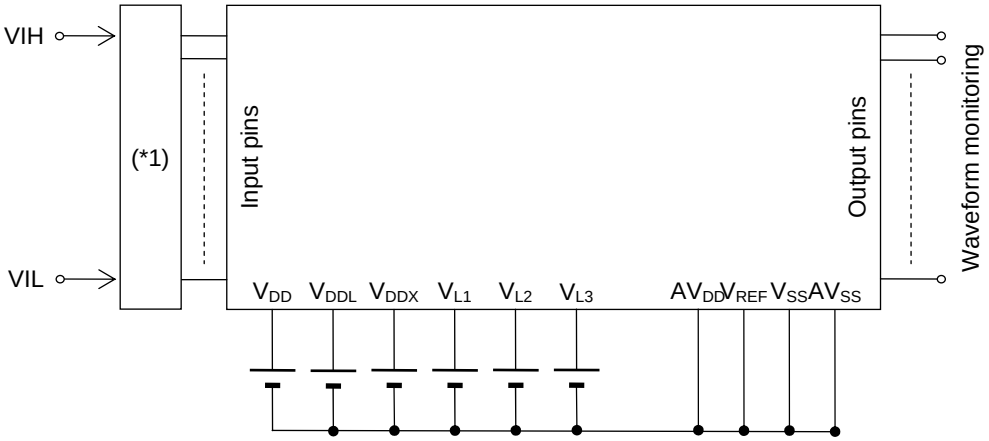
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

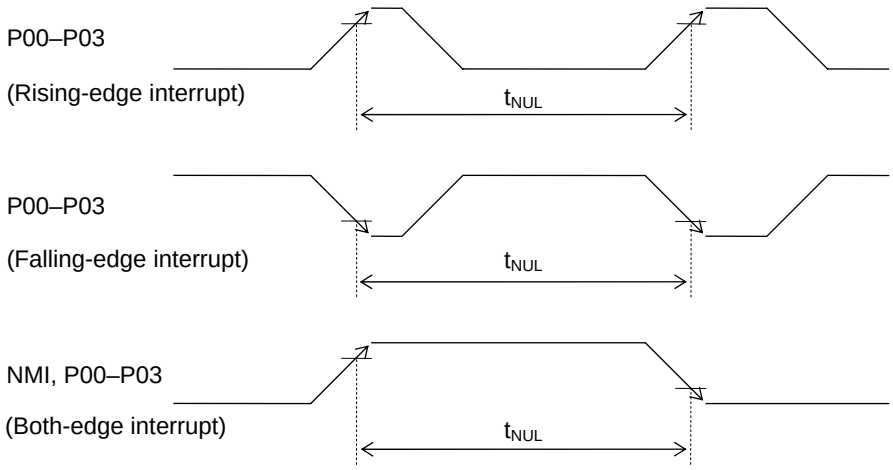


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	µs

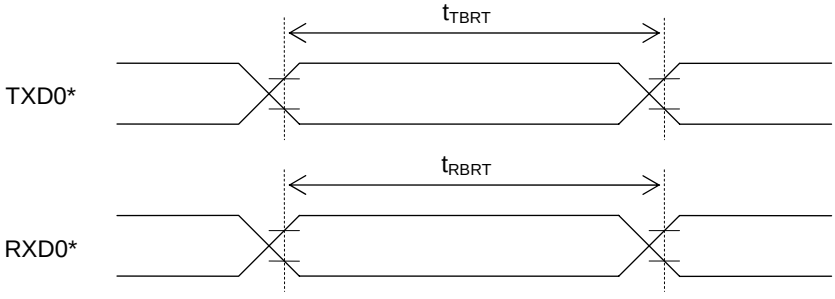


AC CHARACTERISTICS (Serial Port)

(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*[1]	—	s
Receive baud rate	t_{RBRT}	—	BRT*[1] –3%	BRT*[1]	BRT*[1] +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



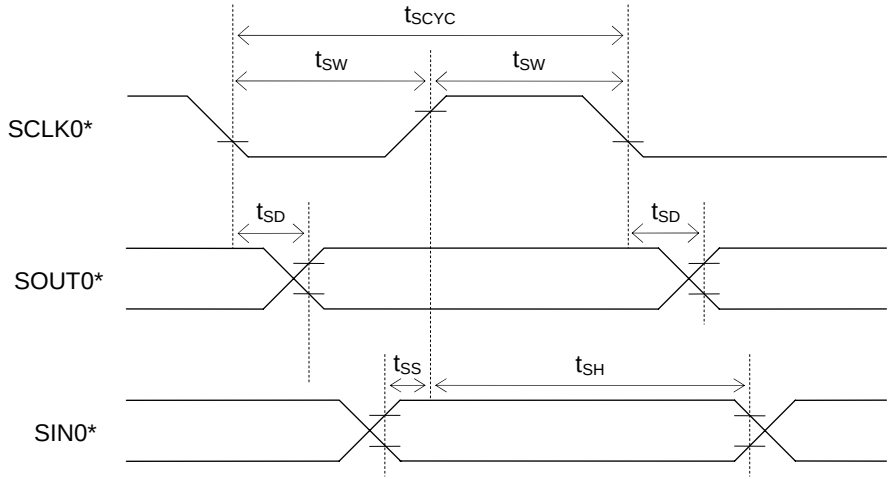
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	µs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*[1]	—	s
SCLK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	µs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*[1] ×0.4	SCLK*[1] ×0.5	SCLK*[1] ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	500	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	500	ns
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	—	500	—	—	ns
SIN input hold time	t_{SH}	—	300	—	—	ns

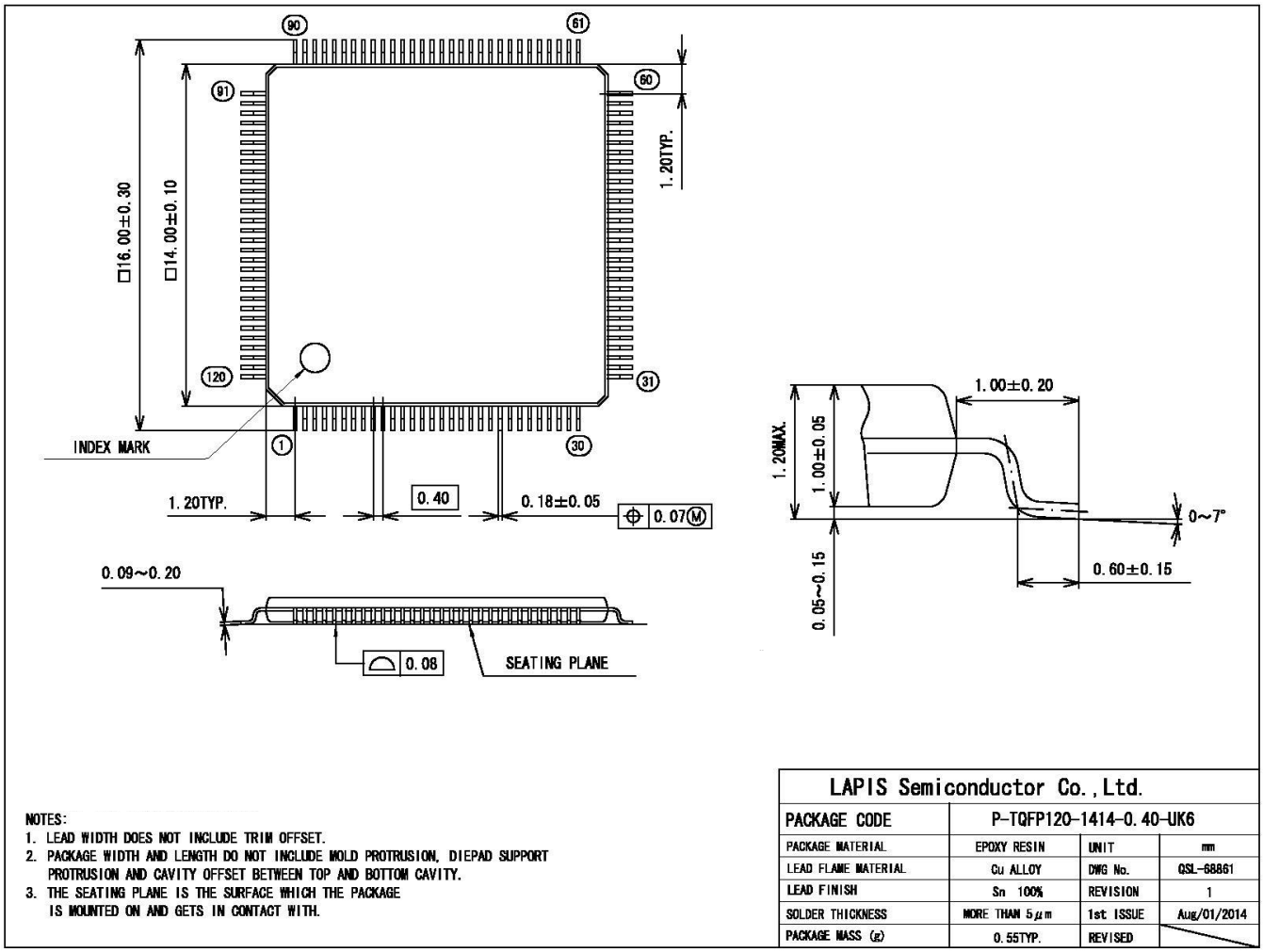
*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)



*: Indicates the secondary function of the port.

PACKAGE DIMENSIONS

(Unit: mm)



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP120-1414-0.40-UK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68861
LEAD FINISH	Sn 100%	REVISION	1
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Aug/01/2014
PACKAGE MASS (g)	0.55TYP.	REVISED	

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q411-01	Jul.17,2010	–	–	Formally edition 1
FEDL610Q411-02	Mar.23,2011	3, 4, 21	3, 4, 21	Add the explanation of ML610Q411PC.
		34	34	Replace the package dimension (Only the format is changed. Package size and material are not changed.)
FEDL610Q411-03	Apr.15,2015	All	All	Change header and footer.
		1~3 5 7 9 11 13 15 16 18~20 21 23 24 25 27	1~3 5 7 9 11 13 15 16 18~20 22 24 25 26 27	Delete ML610Q415 and ML610Q411PC
		4	4	Change from "Shipment" to "Product name ― Supported Function"
		–	21	Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS
		21	22	Change "RESET" to "Reset pulse width (P_{RST}) " and "Power-on reset activation power rise time (T_{POR}) ".
		36	36	Change description in Note.
FEDL610Q411-04	July.13,2015	14	14	Corrected a typo. -PAD No,"37" is corrected to "36". -PAD No,"36" is corrected to "35".

Notes

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