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Details	
Product Status	Last Time Buy
Core Processor	SH-4A
Core Size	32-Bit Single-Core
Speed	324MHz
Connectivity	ATAPI, Ethernet, I²C, SCI, SSI, USB
Peripherals	DMA, LCD, POR, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.15V ~ 1.35V
Data Converters	-
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	404-FBGA
Supplier Device Package	404-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s77640n300bg

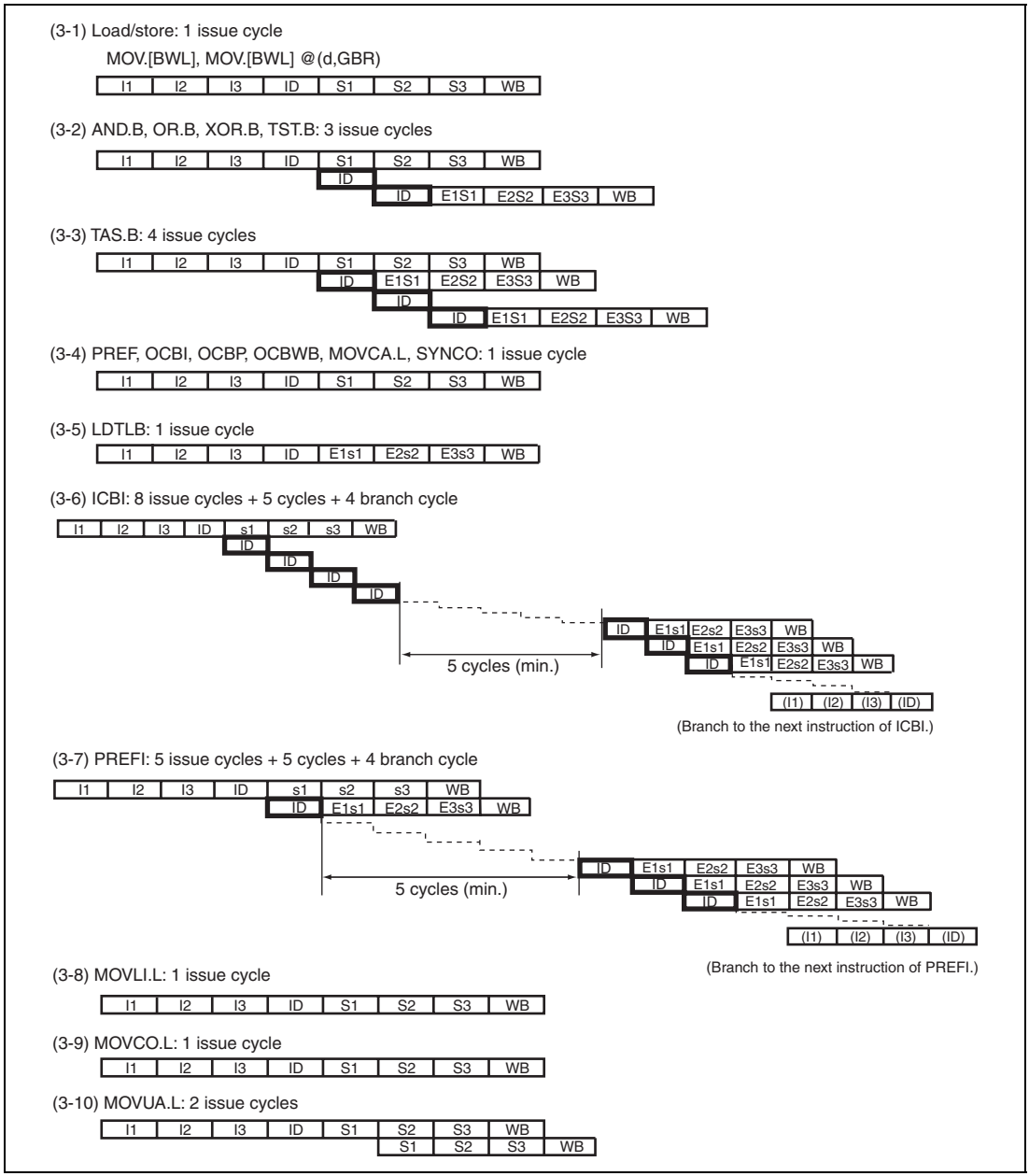

Figure 4.2 Instruction Execution Patterns (3)

5.4 Exception Types and Priorities

Table 5.3 shows the types of exceptions, with their relative priorities, vector addresses, and exception/interrupt codes.

Table 5.3 Exceptions

					Exception Transition Direction*3		
Exception Category	**Execution Mode**	**Exception**	**Priority Level*2**	**Priority Order*2**	**Vector Address**	**Offset**	**Exception Code*4**
Reset	Abort type	Power-on reset	1	1	H'A000 0000	—	H'000
		H-UDI reset	1	1	H'A000 0000	—	H'000
		Instruction TLB multiple-hit exception	1	2	H'A000 0000	—	H'140
		Data TLB multiple-hit exception	1	3	H'A000 0000	—	H'140
General exception	Re-execution type	User break before instruction execution*	2	0	(VBR/DBR)	H'100/—	H'1E0
		Instruction address error	2	1	(VBR)	H'100	H'0E0
		Instruction TLB miss exception	2	2	(VBR)	H'400	H'040
		Instruction TLB protection violation exception	2	3	(VBR)	H'100	H'0A0
		General illegal instruction exception	2	4	(VBR)	H'100	H'180
		Slot illegal instruction exception	2	4	(VBR)	H'100	H'1A0
		General FPU disable exception	2	4	(VBR)	H'100	H'800
		Slot FPU disable exception	2	4	(VBR)	H'100	H'820
		Data address error (read)	2	5	(VBR)	H'100	H'0E0
		Data address error (write)	2	5	(VBR)	H'100	H'100
		Data TLB miss exception (read)	2	6	(VBR)	H'400	H'040
		Data TLB miss exception (write)	2	6	(VBR)	H'400	H'060
		Data TLB protection violation exception (read)	2	7	(VBR)	H'100	H'0A0
		Data TLB protection violation exception (write)	2	7	(VBR)	H'100	H'0C0
		FPU exception	2	8	(VBR)	H'100	H'120
		Initial page write exception	2	9	(VBR)	H'100	H'080

5.6 Description of Exceptions

The various exception handling operations explained here are exception sources, transition address on the occurrence of exception, and processor operation when a transition is made.

5.6.1 Resets

(1) Power-On Reset

- Condition:
  Power-on reset request
- Operations:
  Exception code H'000 is set in EXPEVT, initialization of the CPU and on-chip peripheral module is carried out, and then a branch is made to the reset vector (H'A0000000). For details, see the register descriptions in the relevant sections. A power-on reset should be executed when power is supplied.

(2) H-UDI Reset

- Source: SDIR.TI[7:4] = B'0110 (negation) or B'0111 (assertion)
- Transition address: H'A0000000
- Transition operations:
  Exception code H'000 is set in EXPEVT, initialization of VBR and SR is performed, and a branch is made to PC = H'A0000000.
  CPU and on-chip peripheral module initialization is performed. For details, see the register descriptions in the relevant sections.

- FSCHG

This instruction changes the value of the SZ bit in FPSCR, enabling fast switching between use and non-use of pair single-precision data transfer.

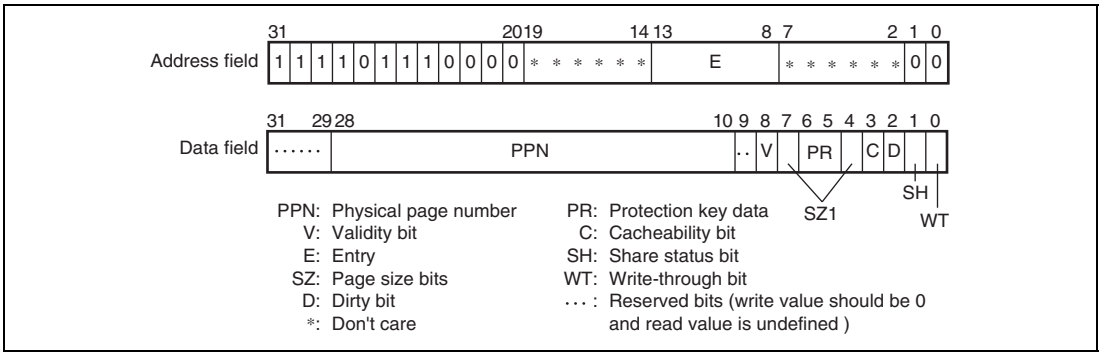

Figure 7.23 Memory-Mapped UTLB Data Array (TLB Compatible Mode)

7.7.6 UTLB Data Array (TLB Extended Mode)

In TLB extended mode, the names of the data arrays have been changed from UTLB data array to UTLB data array 1, UTLB data array 2 is added, and the EPR and ESZ bits are accessible. In TLB extended mode, the PR and SZ bits of UTLB data array 1 are reserved and 0 should be specified as the write value for these bits. In addition, when a write to UTLB data array 1 is performed, a write to UTLB data array 2 of the same entry should always be performed after that.

In TLB compatible mode (MMUCR.ME = 0), UTLB data array 2 cannot be accessed. Operation if they are accessed is not guaranteed.

(1) UTLB Data Array 1

In TLB extended mode, bits 7 to 4 in the data field, which correspond to the PR and SZ bits in compatible mode, are reserved. Specify 0 as the write value for these bits.

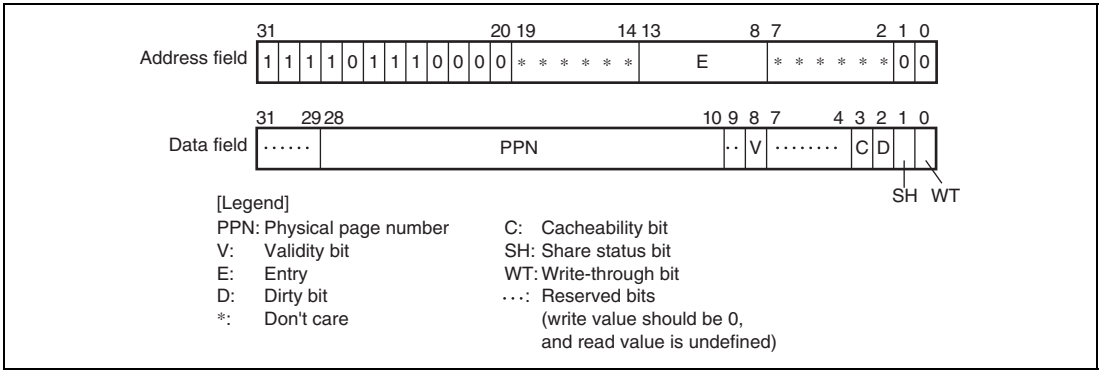

Figure 7.24 Memory-Mapped UTLB Data Array 1 (TLB Extended Mode)

11.4.15 CS3 Bus Control Register (CS3BCR)

Bit:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IWW[2:0]			—	IWRWD[2:0]			—	IWRWS[2:0]			—	IWRRD[2:0]		
Initial value:	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	IWRRS[2:0]			—	—	SZ[1:0]		RDSPL	—	—	—	—	—	—	—
Initial value:	0	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
63 to 31	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

11.9 Bus Arbitration

This module has two arbitration functions: one is arbitration of the accesses between the various internal modules, and the other is arbitration of the bus requests from the external devices.

11.9.1 Arbitration of Accesses between Internal Modules

This module arbitrates SDRAM or SRAM accesses between the CPU, various pixel bus modules, and LCDC. (SRAM cannot be accessed by the pixel bus modules or LCDC.) Since SDRAM accesses are often used for the applications requiring real-time operation such as reading out the image data for display, it is significant to assign the appropriate priority to the modules so that the requirements of the modules such as response time and bandwidth are satisfied. The policy of priority assignment is given below.

1. The highest priority (level 0) is given to SDRAM control such as refreshing and page management.
   Memory is refreshed according to the memory refresh interval specified separately.
2. A high priority (level 1) is given to the display controller (VDC2) and LCD controller (LCDC) to support transfer of the output data for display, which requires real-time operation.
3. A lower priority (level 2 or 3) is given to the other accesses.
   Either level can be selected for each module.

Figure 11.20 shows the arbitration of the access requests. In the figure, priority level 1 is given to the VDC2 and LCDC, and the round-robin method is used to arbitrate the accesses between them. Similarly, priority level 3 is given to the SuperHyway modules (CPU, DMAC, EtherC, and others), ATAPI, and G2D command/data; and the round-robin method is used to arbitrate the accesses between them. Access requests are arbitrated using the request signals that are being asserted at the arbitration timing. Figure 11.21 shows an arbitration example in which the priority levels of SuperHyway modules and G2D module are raised to level 2. Arbitration is carried out only between the modules indicated by the solid lines.

The request-masking function is provided to limit memory accesses during NMI interrupt processing. This function allows assigning relatively higher percentage of memory use *by* the CPU interrupt processing upon NMI interrupt generation. Requests from different modules can be masked separately through the request mask setting register (RQM) so that the optimum settings can be made according to the usage of NMI.

For the LCDC, any of priority levels 1, 2, and 3 can be selected through register setting.

The priority is determined hierarchically according to the priority level, round-robin scheduling for the modules with the same priority level, and sub-round-robin scheduling for the modules with the same priority level, in this order. The following describes each determination.

1. Determination according to the priority level

   The priority is fixed: level 0 > level 1 > level 2 > level 3.
2. Determination according to the level-1 round-robin scheduling

   The priority is determined according to the round-robin scheduling for the level-1 modules.

   After reset: LCDC > pixel bus module

   After the LCDC has been selected: Pixel bus > LCDC

   After the pixel bus has been selected: LCDC > pixel bus

   Note that the pixel bus refers to the modules selected according to the level-1 pixel bus sub-round-robin scheduling.
3. Determination according to the level-1 pixel bus sub-round-robin scheduling

   When this determination is selected, the priority is also determined according to the round-robin scheduling for the level-1 pixel bus modules.

   After reset: VDC2 (layer 1) > VDC2 (layer 2) > VDC2 (layer 3) > VDC2 (layer 4)

   After the VDC2 (layer 1) has been selected: VDC2 (layer 2) > VDC2 (layer 3) > VDC2 (layer 4) > VDC2 (layer 1)

   After the VDC2 (layer 2) has been selected: VDC2 (layer 3) > VDC2 (layer 4) > VDC2 (layer 1) > VDC2 (layer 2)

   After the VDC2 (layer 3) has been selected: VDC2 (layer 4) > VDC2 (layer 1) > VDC2 (layer 2) > VDC2 (layer 3)

   After the VDC2 (layer 4) has been selected: VDC2 (layer 1) > VDC2 (layer 2) > VDC2 (layer 3) > VDC2 (layer 4)
4. Determination according to the level-2 or level-3 round-robin scheduling

   The priority is determined according to the round-robin scheduling for the level-2 or level-3 modules. Either priority level 2 or 3 can be given to the devices separately through the arbitration mode register.

   When the same priority level is assigned to more than one device, the priority is determined according to the round-robin scheduling for each level.

   The priority of the devices with the same priority level is as follows:

   After reset: SuperHyway > pixel bus > LCDC

   Note that the pixel bus refers to the devices selected according to the level-2 or level-3 pixel bus sub-round-robin scheduling.

   After the pixel bus has been selected: LCDC > SuperHyway > pixel bus

   After the LCDC has been selected: SuperHyway > pixel bus > LCDC

18.3.9 Block Count Source Registers 0 to 5 (SSIBLCNTSR0 to SSIBLCNTSR5)

SSIBLCNTSR0 to SSIBLCNTSR5 is a 32-bit readable/writable register that set the transfer byte count as SSIBLCNT0 to SSIBLCNT5 increment timing other than the port function. This register value is initialized by a hardware reset or the software reset for the corresponding SSI_DMAC (DMRST bit in the corresponding SSIDMCOR0 to SSIDMCOR5). To be written to this register, DMEN bit in the corresponding SSIDMCOR0 to SSIDMCOR5 must be 0.

In addition, when the block transfer end interrupt or the n-times block transfer end interrupt is used, set a value other than the initial value in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BLCNTSR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BLCNTSR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BLCNTSR [31:0]	All 0	R/W	SSIBLCNT0 to SSIBLCNT5 Increment Timing These bits set the transfer byte count as SSIBLCNT0 to SSIBLCNT5 increment timing. The following transfer count should be selected according to the RDMA or WDMA maximum burst size. 1 burst: 8 × n [H'08 × n] (bytes) 2 bursts: 16 × n [H'10 × n] (bytes) 4 bursts: 32 × n [H'20 × n] (bytes)

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	RFFO[2:0]	111	R/W	Receive Frame Count Overflow BSY Output Threshold 000: When two receive frames have been stored in the receive FIFO. 001: When four receive frames have been stored in the receive FIFO. 010: When six receive frames have been stored in the receive FIFO. : 110: When 14 receive frames have been stored in the receive FIFO. 111: When 16 receive frames have been stored in the receive FIFO.
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	RFDO[2:0]	111	R/W	Receive FIFO Overflow BSY Output Threshold 000: When (256 – 32) bytes of data is stored in the receive FIFO. 001: When (512 – 32) bytes of data is stored in the receive FIFO. : 110: When (1792 – 32) bytes of data is stored in the receive FIFO. 111: When (2048 – 32) bytes of data is stored in the receive FIFO.

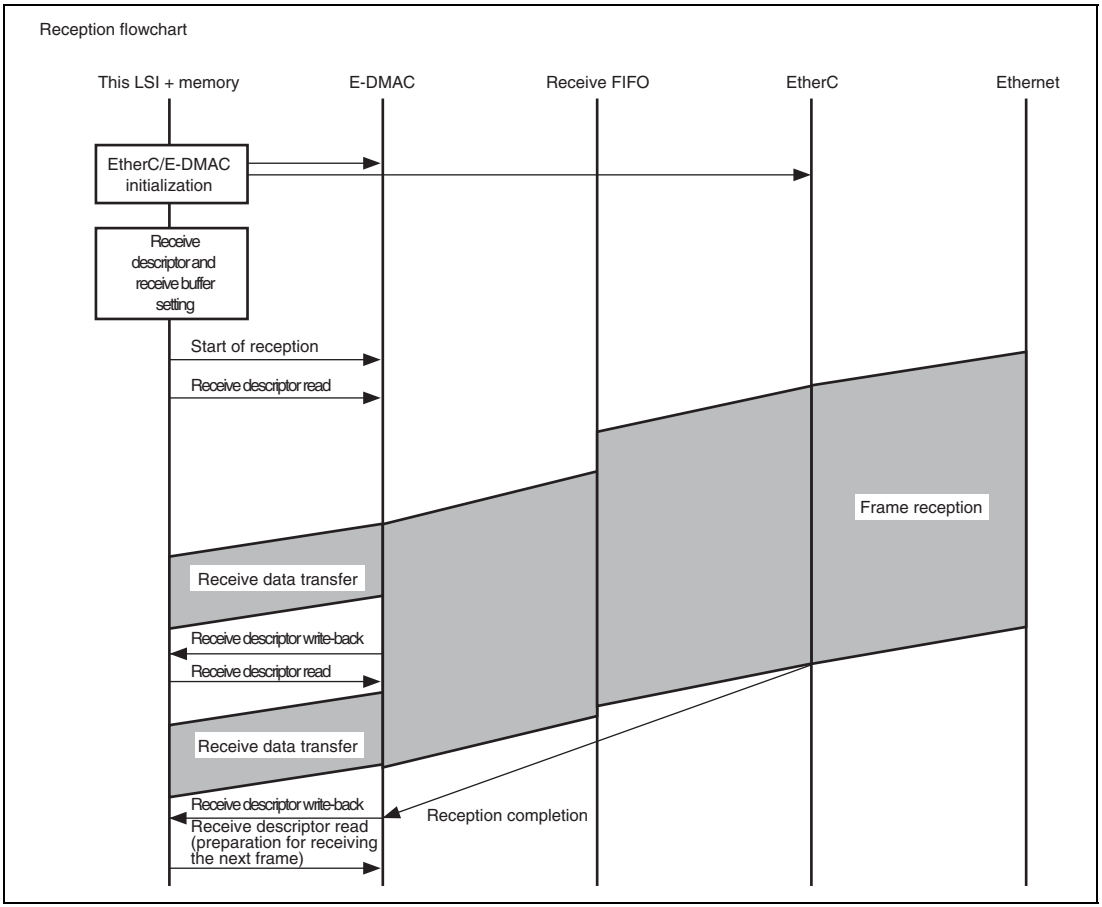

Figure 20.5 Sample Reception Flowchart (Single-Frame/Two-Descriptor)

Bit	Bit Name	Initial Value	R/W	Description
11, 10	MBW[1:0]	All 0	R/W	FIFO Port Access Bit Width Specifies the bit width for accessing the DnFIFO port. 00: 8-bit width 01: 16-bit width 10: 32-bit width 11: Setting prohibited When the selected pipe is in the receiving direction, once reading data is started after setting these bits, these bits should not be modified until all the data has been read. When the selected pipe is in the receiving direction, set the CURPIPE and MBW bits simultaneously. When the selected pipe is in the transmitting direction, the bit width cannot be changed from the 8-bit width to the 16-/32-bit width or from the 16-bit width to the 32-bit width while data is being written to the buffer memory. The odd number of bytes can be written through byte-access control even when 8- or 16-bit width is selected.
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
8	BIGEND	0	R/W	FIFO Port Endian Control Specifies the byte endian for the DnFIFO port. 0: Little endian 1: Big endian
7 to 4	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

Table 21.18 Pipe Setting Items

Register Name	Bit Name	Setting Contents	Remarks
DCPCFG PIPECFG	TYPE	Specifies the transfer type	PIPE1 to PIPE9: Can be set
	BFRE	Selects the BRDY interrupt mode	PIPE1 to PIPE5: Can be set
	DBLB	Selects a double buffer	PIPE1 to PIPE5: Can be set
	CNTMD	Selects continuous transfer or non-continuous transfer	PIPE1 and PIPE2: Can be set (only when bulk transfer has been selected). PIPE3 to PIPE5: Can be set
	DIR	Selects transfer direction	IN or OUT can be set
	EPNUM	Endpoint number	PIPE1 to PIPE9: Can be set A value other than 0000 should be set when the pipe is used.
	SHTNAK	Selects disabled state for pipe when transfer ends	PIPE1 and PIPE2: Can be set (only when bulk transfer has been selected) PIPE3 to PIPE5: Can be set
PIPEBUF	BUFSIZE	Buffer memory size	DCP: Cannot be set (fixed at 256 bytes) PIPE1 to PIPE5: Can be set (a maximum of 2 Kbytes can be specified) PIPE6 to PIPE9: Cannot be set (fixed at 64 bytes)
	BUFNMB	Buffer memory number	DCP: Cannot be set (areas fixed at H'0 to H'3) PIPE1 to PIPE5: Can be set (can be specified in areas H'8 to H'7F) PIPE6 to PIPE9: Cannot be set (areas fixed at H'4 to H'7)

(7) User Clipping Area MAX Register (UCLMAR)

Offset: H'0D8

Initial Value: Undefined

The user clipping area MAX register (UCLMAR) is a 32-bit read-only register which indicates the maximum values of the user clipping coordinates. The upper word indicates the maximum value of the user clipping X coordinate (UXMAX) and the lower word indicates the maximum value of the user clipping Y coordinate (UYMAX). The unused bits are always read as 0. When setting this register by the WPR command, set UXMAX and UYMAX in the following ranges: $0 \leq UXMIN \leq UXMAX \leq SXMAX \leq 4095$, $0 \leq UYMIN \leq UYMAX \leq SYMAX \leq 4095$.

UCLMAR retains its value at a reset.

(8) Relative User Clipping Area MIN Register (RUCLMIR)

Offset: H'0DC

Initial Value: Undefined

The relative user clipping area MIN register (RUCLMIR) is a 32-bit read-only register which indicates the minimum values of the relative user clipping coordinates (offset values added to the local offset). When setting this register by the WPR command, set the relative coordinates from the local offset. The upper word indicates the minimum value of the relative user clipping X coordinate (RUXMIN) and the lower word indicates the minimum value of the relative user clipping Y coordinate (RUYMIN). The unused bits are always read as 0. When setting this register by the WPR command, set RUXMIN and RUYMIN in the following ranges: $0 \leq RUXMIN \leq RUXMAX \leq SXMAX \leq 4095$, $0 \leq RUYMIN \leq RUYMAX \leq SYMAX \leq 4095$. For details on the setting ranges, see (5) Relative Clipping Specification (RCLIP), in section 23.1.5, Rendering Attributes.

RUCLMIR retains its value at a reset.

(9) Relative User Clipping Area MAX Register (RUCLMAR)

Offset: H'0E0

Initial Value: Undefined

The relative user clipping area MAX register (RUCLMAR) is a 32-bit read-only register which indicates the maximum values of the relative user clipping coordinates (offset values added to the local offset). When setting this register by the WPR command, set the relative coordinates from

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	DTFO[7:0]	H'00	R/W	Fourth Data Specify 4th data to be input or output via the FD7 to FD0 pins. In write: Specify write data In read: Store read data

25.3.12 Control Code FIFO Register (FLECFIFO)

FLECFIFO is used to read or write the control code FIFO area.

In DMA transfer, data in this register must be specified as the destination (source).

Note that the direction of read or write specified by the SELRW bit in FLCMDCR must match that specified in this register.

When transferring 16-byte DMA, access FLECFIFO from the address on the 16-byte address boundary.

Before accessing the FLECFIFO, clear the FIFO data by setting the AC1CLR bit in the FINTDMACR to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECFO[31:24]								ECFO[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ECFO[15:8]								ECFO[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ECFO [31:24]	H'00	R/W	First Data Specify 1st data to be input or output via the FD7 to FD0 pins. In write: Specify write data In read: Store read data

26.2.3 SRC Input Data Control Register (SRCIDCTRL)

SRCIDCTRL is a 16-bit readable/writable register that specifies the endian format of input data, enables/disables the interrupt requests, and specifies the triggering number of data units.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	IED	IEN	-	-	-	-	-	-	IFTRG[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	IED	0	R/W	Input Data Endian Specifies the endian format of the input data. 0: Big endian 1: Little endian
8	IEN	0	R/W	Input Data FIFO Empty Interrupt Enable Enables/disables the input data FIFO empty interrupt request to be issued when the number of data units in the input FIFO becomes equal to or smaller than the triggering number specified by the IFTRG1 and IFTRG0 bits, thus resulting in the IINT bit in the SRC status register (SRCSTAT) being set to 1. 0: Input data FIFO empty interrupt is disabled. 1: Input data FIFO empty interrupt is enabled.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

With the above settings, the user break occurs after executing the instruction at address H'00037226 where ASID is H'80 before executing the instruction at address H'0003722E where ASID is H'70.

- Example 1-3

  Register settings: CBR0 = H'00000013 / CRR0 = H'00002001 / CAR0 = H'00027128 / CAMR0 = H'00000000 / CBR1 = H'00000013 / CRR1 = H'00002001 / CAR1 = H'00031415 / CAMR1 = H'00000000 / CDR1 = H'00000000 / CDMR1 = H'00000000 / CETR1 = H'00000000 / CBCR = H'00000000

  Specified conditions: Independent for channels 0 and 1

  — Channel 0

    Address: H'00027128 / Address mask: H'00000000

    Bus cycle: Instruction fetch (before executing the instruction)

    ASID is not included in the conditions.

  — Channel 1

    Address: H'00031415 / Address mask: H'00000000

    Data: H'00000000 / Data mask: H'00000000 / Execution count: H'00000000

    Bus cycle: Instruction fetch (before executing the instruction)

    ASID, data values, and execution count are not included in the conditions.

  With the above settings, the user break occurs for channel 0 before executing the instruction at address H'00027128. No user break occurs for channel 1 since the instruction fetch is executed only at even addresses.

- Example 1-4

  Register settings: CBR0 = H'40800013 / CRR0 = H'00002000 / CAR0 = H'00037226 / CAMR0 = H'00000000 / CBR1 = H'C0700013 / CRR1 = H'00002001 / CAR1 = H'0003722E / CAMR1 = H'00000000 / CDR1 = H'00000000 / CDMR1 = H'00000000 / CETR1 = H′00000000 / CBCR = H'00000000

  Specified conditions: Channel 0 → Channel 1 sequential mode

  — Channel 0

    Address: H'00037226 / Address mask: H'00000000 / ASID: H'80

    Bus cycle: Instruction fetch (before executing the instruction)

  — Channel 1

    Address: H'0003722E / Address mask: H'00000000 / ASID: H'70

    Data: H'00000000 / Data mask: H'00000000 / Execution count: H'00000000

    Bus cycle: Instruction fetch (before executing the instruction)

    Data values and execution count are not included in the conditions.

Number	Pin Name	I/O*
289	D41/IODREQ	OUTPUT
288	D41/IODREQ	INPUT
287	D35/IDEA0	CONTROL
286	D35/IDEA0	OUTPUT
285	D35/IDEA0	INPUT
284	D37/IDEA1	CONTROL
283	D37/IDEA1	OUTPUT
282	D37/IDEA1	INPUT
281	D39/IDED14	CONTROL
280	D39/IDED14	OUTPUT
279	D39/IDED14	INPUT
278	D34/PF5	CONTROL
277	D34/PF5	OUTPUT
276	D34/PF5	INPUT
275	D36/IDEA2	CONTROL
274	D36/IDEA2	OUTPUT
273	D36/IDEA2	INPUT
272	D63/IDED1	CONTROL
271	D63/IDED1	OUTPUT
270	D63/IDED1	INPUT
269	D38/IDED15	CONTROL
268	D38/IDED15	OUTPUT
267	D38/IDED15	INPUT
266	D62/IDED0	CONTROL
265	D62/IDED0	OUTPUT
264	D62/IDED0	INPUT
263	$\overline{\text{WE2}}$/DQM64UL	CONTROL
262	$\overline{\text{WE2}}$/DQM64UL	OUTPUT
261	$\overline{\text{WE0}}$/DQM64LL	CONTROL
260	$\overline{\text{WE0}}$/DQM64LL	OUTPUT
259	D60/IDED2	CONTROL
258	D60/IDED2	OUTPUT

Number	Pin Name	I/O*
193	AUDIO_CLK2/PC5	INPUT
192	CRS/PD7/IDEA1_M	CONTROL
191	CRS/PD7/IDEA1_M	OUTPUT
190	CRS/PD7/IDEA1_M	INPUT
189	COL/PE7/IDEA2_M	CONTROL
188	COL/PE7/IDEA2_M	OUTPUT
187	COL/PE7/IDEA2_M	INPUT
186	TX_ER/PD6/$\overline{\text{IDEIOWR\_M}}$	CONTROL
185	TX_ER/PD6/$\overline{\text{IDEIOWR\_M}}$	OUTPUT
184	TX_ER/PD6/$\overline{\text{IDEIOWR\_M}}$	INPUT
183	MII_TXD3/SSIDATA5/$\overline{\text{IODACK\_M}}$/PD0	CONTROL
182	MII_TXD3/SSIDATA5/$\overline{\text{IODACK\_M}}$/PD0	OUTPUT
181	MII_TXD3/SSIDATA5/$\overline{\text{IODACK\_M}}$/PD0	INPUT
180	MII_TXD2/AUDIO_CLK5/IDEINT_M/PD1	CONTROL
179	MII_TXD2/AUDIO_CLK5/IDEINT_M/PD1	OUTPUT
178	MII_TXD2/AUDIO_CLK5/IDEINT_M/PD1	INPUT
177	RX_ER/PE6/IODREQ_M	CONTROL
176	RX_ER/PE6/IODREQ_M	OUTPUT
175	RX_ER/PE6/IODREQ_M	INPUT
174	MII_TXD1/SSIWS5/$\overline{\text{IDEIORD\_M}}$/PD2	CONTROL
173	MII_TXD1/SSIWS5/$\overline{\text{IDEIORD\_M}}$/PD2	OUTPUT
172	MII_TXD1/SSIWS5/$\overline{\text{IDEIORD\_M}}$/PD2	INPUT
171	SSIDATA3/PH4	CONTROL
170	SSIDATA3/PH4	OUTPUT
169	SSIDATA3/PH4	INPUT
168	MII_TXD0/SSISCK5/IDEIORDY_M/PD3	CONTROL
167	MII_TXD0/SSISCK5/IDEIORDY_M/PD3	OUTPUT
166	MII_TXD0/SSISCK5/IDEIORDY_M/PD3	INPUT
165	TX_EN/PD4/IDED0_M	CONTROL
164	TX_EN/PD4/IDED0_M	OUTPUT
163	TX_EN/PD4/IDED0_M	INPUT
162	SSIWS3/PH6	CONTROL

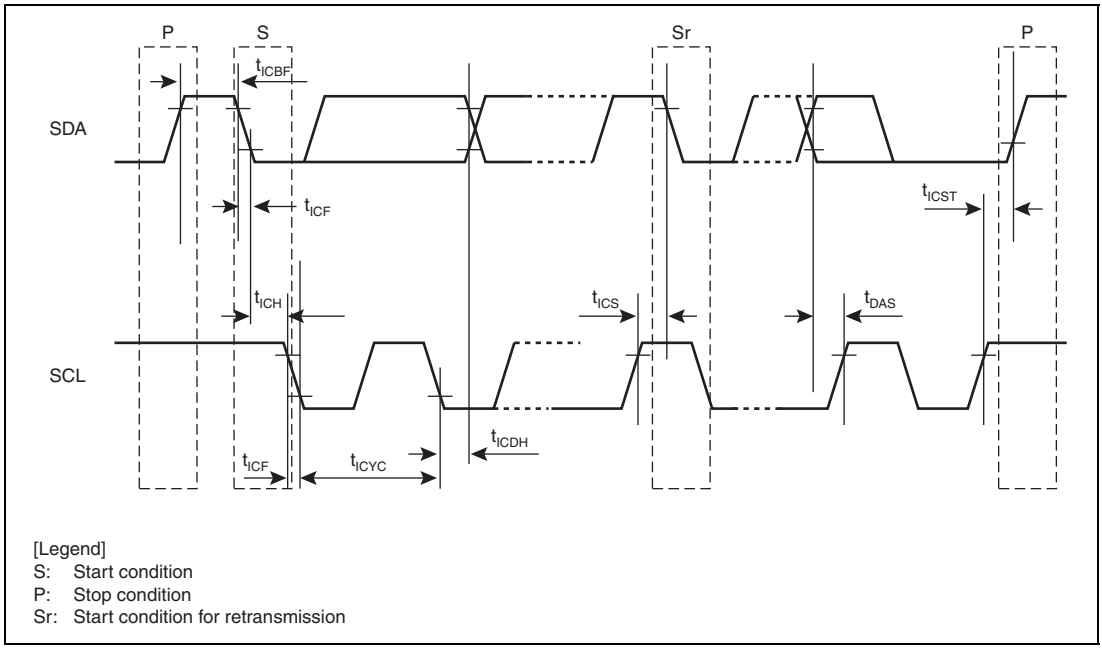

Figure 34.28 I²C Timing

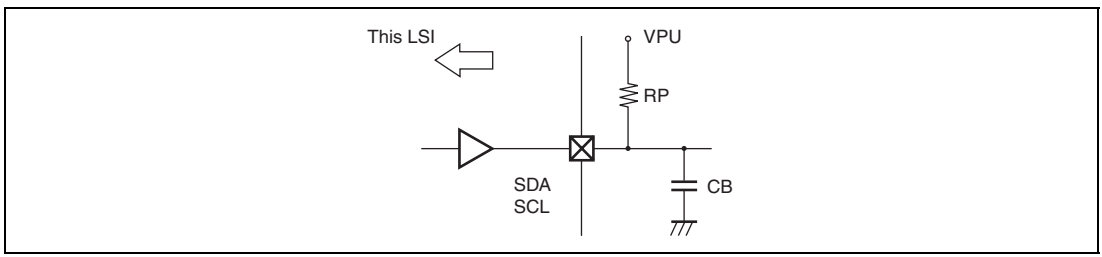

Figure 34.29 AC Characteristics Load Condition