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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	64MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	143
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	68K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-PBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f296

List of tables

Table 2. Ball description

Symbol	Ball no.	Type	Function (including port, pin and alternate function where applicable)			
P6.0 to P6.7	E4	O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 6 outputs can be configured as push-pull or open-drain drivers. The input threshold of Port 6 is selectable (TTL or CMOS).	P6.0	$\overline{CS0}$	Chip select 0 output
	D3	O		P6.1	$\overline{CS1}$	Chip select 1 output
	B1	O		P6.2	$\overline{CS2}$	Chip select 2 output
		I/O			SCLK1	SSC1: Master clock output/slave clock input
	C1	O		P6.3	$\overline{CS3}$	Chip select 3 output
		I/O			MTSR1	SSC1: Master-transmitter/slave-receiver O/I
	D2	O		P6.4	$\overline{CS4}$	Chip select 4 output
		I/O			MRST1	SSC1: Master-receiver/slave-transmitter I/O
	E3	I		P6.5	$\overline{HOLD}$	External master hold request input
	F4	O		P6.6	$\overline{HLDA}$	Hold acknowledge output
	D1	O		P6.7	$\overline{BREQ}$	Bus request output
P8.0 to P8.7	E2	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 8 outputs can be configured as push-pull or open-drain drivers. The input threshold of Port 8 is selectable (TTL or CMOS).	P8.0	CC16IO	CAPCOM2: CC16 capture input/compare output
	F3	I/O		P8.1	CC17IO	CAPCOM2: CC17 capture input/compare output
	F2	I/O		P8.2	CC18IO	CAPCOM2: CC18 capture input/compare output
	G3	I/O		P8.3	CC19IO	CAPCOM2: CC19 capture input/compare output
	G2	I/O		P8.4	CC20IO	CAPCOM2: CC20 capture input/compare output
	H4	I/O		P8.5	CC21IO	CAPCOM2: CC21 capture input/compare output
	H3	I/O		P8.6	CC22IO	CAPCOM2: CC22 capture input/compare output
					RxD1	ASC1: Data input (asynchronous) or I/O (synchronous)
	H2	I/O		P8.7	CC23IO	CAPCOM2: CC23 capture input/compare output
		O			TxD1	ASC1: Clock/data output (asynchronous/synchronous)

Table 2. Ball description (continued)

Symbol	Ball no.	Type	Function (including port, pin and alternate function where applicable)
V_{SS}	A1, A4 A8, A11, A13, A16 A17, B3, B5 B6, B8 B9, B17, D5, D6 F1, F17, G4, H1 K16, K17, L1, L4 N15, N17, R17, T15, T16, U7, U10, U13, U14, U16, U17	-	Digital ground

Flash address register low (FARL)

FARL (0x0E 0010)							FCR						Reset value: 0000h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
ADD 15	ADD 14	ADD 13	ADD 12	ADD 11	ADD 10	ADD 9	ADD 8	ADD 7	ADD 6	ADD 5	ADD 4	ADD 3	ADD 2	Reserved
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	-

Table 22. FARL register description

BIt	Bit name	Function
15-2	ADD[15:2]	Address 15:2 These bits must be written with the address of the Flash location to program in the following operations: Word program (32-bit) and double word program (64-bit). In double word program the ADD2 bit must be written to 0.
1-0	-	Reserved

Flash address register high (FARH)

FARH (0x0E 0012)											FCR			Reset value: 0000h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											ADD 20	ADD 19	ADD 18	ADD 17	ADD 16
-											RW	RW	RW	RW	RW

Table 23. FARH register description

BIt	Bit name	Function
15-5	-	Reserved
4-0	ADD[20:16]	Address 20:16 These bits must be written with the address of the Flash location to program in the following operations: Word program and double word program.

5.5.5 Erase suspend, program and resume

A sector erase operation can be suspended in order to program (word or double word) another sector.

Example: Sector erase of sector B3F1 of Bank 3 in XFlash module.

```
FCR0H|= 0x0800;     /*Set SER in FCR0H*/
FCR1H|= 0x0002;     /*Set B3F1*/
FCR0H|= 0x8000;     /*Operation start*/
```

Example: Sector erase suspend

```
FCR0H|= 0x4000;     /*Set SUSP in FCR0H*/
do                  /* Loop to wait for LOCK=0 and BSY bit(s)=0 */
{tmp = FCR0L ;
} while( (tmp && 0x00E6) );
```

Example: Word program of data 0x5555AAAA at address 0x0C5554 in XFlash module.

```
FCR0H&= 0xBFFF;     /*Rst SUSP in FCR0H*/
FCR0H|= 0x2000;     /*Set WPG in FCR0H*/
FARL = 0x5554;      /*Load Add in FARL*/
FARH = 0x000C;      /*Load Add in FARH*/
FDR0L = 0xAAAA;     /*Load Data in FDR0L*/
FDR0H = 0x5555;     /*Load Data in FDR0H*/
FCR0H|= 0x8000;     /*Operation start*/
```

Once the program operation is finished, the erase operation can be resumed in the following way:

```
FCR0H|= 0x0800;     /*Set SER in FCR0H*/
FCR0H|= 0x8000;     /*Operation resume*/
```

During the program operation in erase suspend, bits SER and SUSP are low. A word or double word program during erase suspend cannot be suspended.

To summarize:

- A sector erase can be suspended by setting SUSP bit
- To perform a word program operation during erase suspend, bits SUSP and SER must first be reset, then bits WPG and WMS can be set.
- To resume the sector erase operation bit SER must be set again
- It is forbidden to start any write operation when the SUSP bit is set

6.5.2 Hardware aspects

The new bootstrap loading method via UART and CAN is compatible with the old method via UART only. However, some additional hardware is required with the new method which is summarized in Table 41.

Table 41. Hardware topics summary

Actual bootstrap loader	New bootstrap loader	Comments
P4.5 can be used as output in BSL mode	P4.5 cannot be used as user output in BSL mode. It can only be used as CAN1_RxD, input, or address-segments.	
The level on CAN1_RxD can change during step 2 of the booting steps (see Section 6.2.3 on page 70)	The level on CAN1_RxD must be stable at 1 during step 2 of the booting steps (see Section 6.2.3 on page 70)	External pull-up on P4.5 needed

6.6 Alternate boot mode (ABM)

6.6.1 Activation

Alternate boot mode is activated with the combination 01 on Port 0L[5..4] at the rising edge of $\overline{\text{RSTIN}}$.

6.6.2 Memory mapping

ST10F296E has the same memory mapping for standard and alternate boot mode:

- Test-Flash: Mapped from 00’0000h. The standard bootstrap loader can be started by executing a jump to the address of this routine (JMPS 00’xxxx; address to be defined).
- User Flash: The user Flash is divided into two parts: The IFlash, visible only for memory reads and memory writes (no code fetch) and the XFlash, visible for any ST10 access (memory read, memory write, code fetch).
- All ST10F296E XRAM and XPeripheral modules can be accessed if enabled in the XPERCON register.

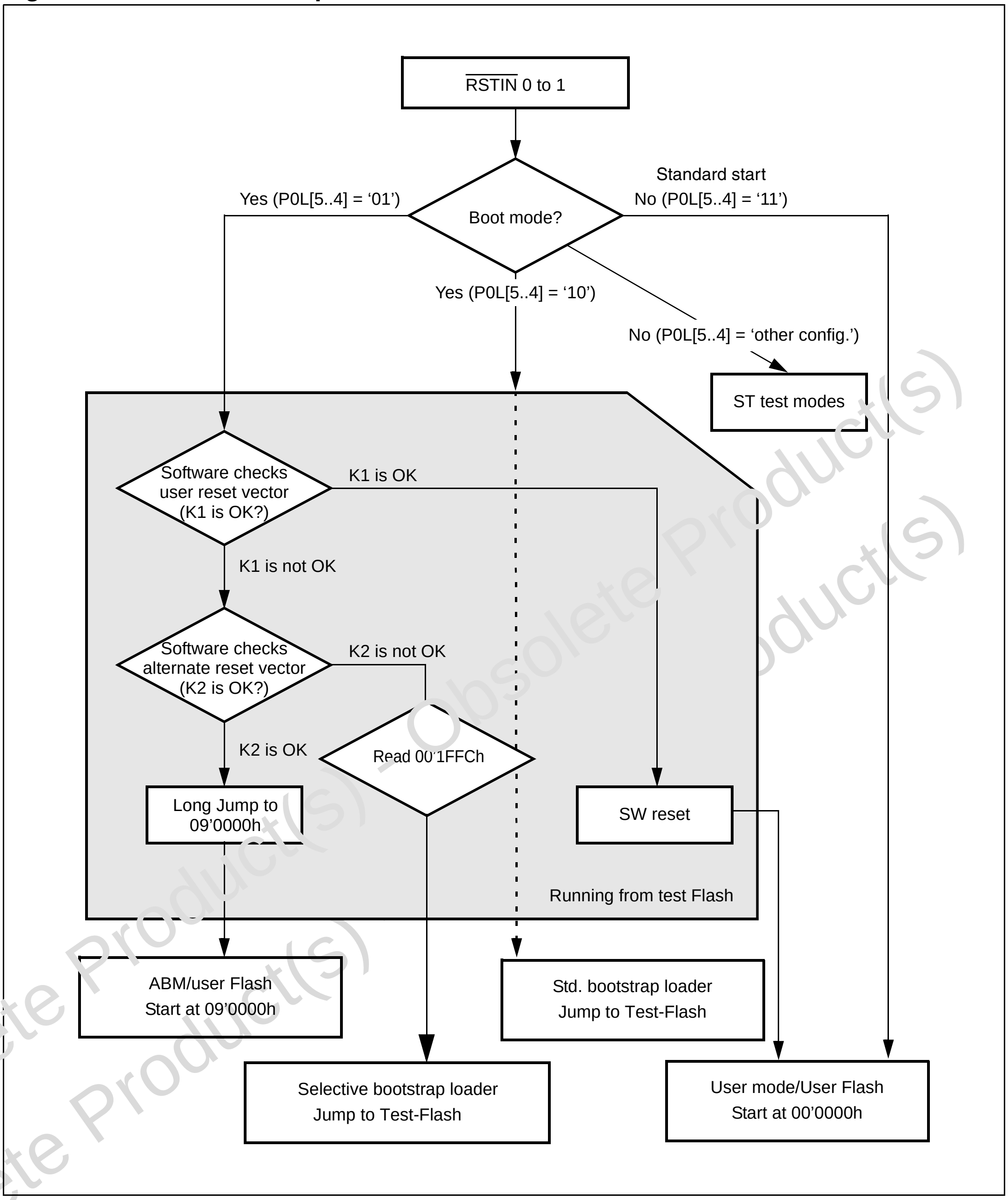
Note: *The alternate boot mode can be used to reprogram the whole content of ST10F296E user Flash (except Block 0 in Bank 2).*

6.6.3 Interrupts

The ST10 interrupt vector table is always mapped from address 00’0000h.

As a consequence, interrupts are not allowed in alternate boot mode. All maskable and non maskable interrupts must be disabled.

Figure 15. Reset boot sequence



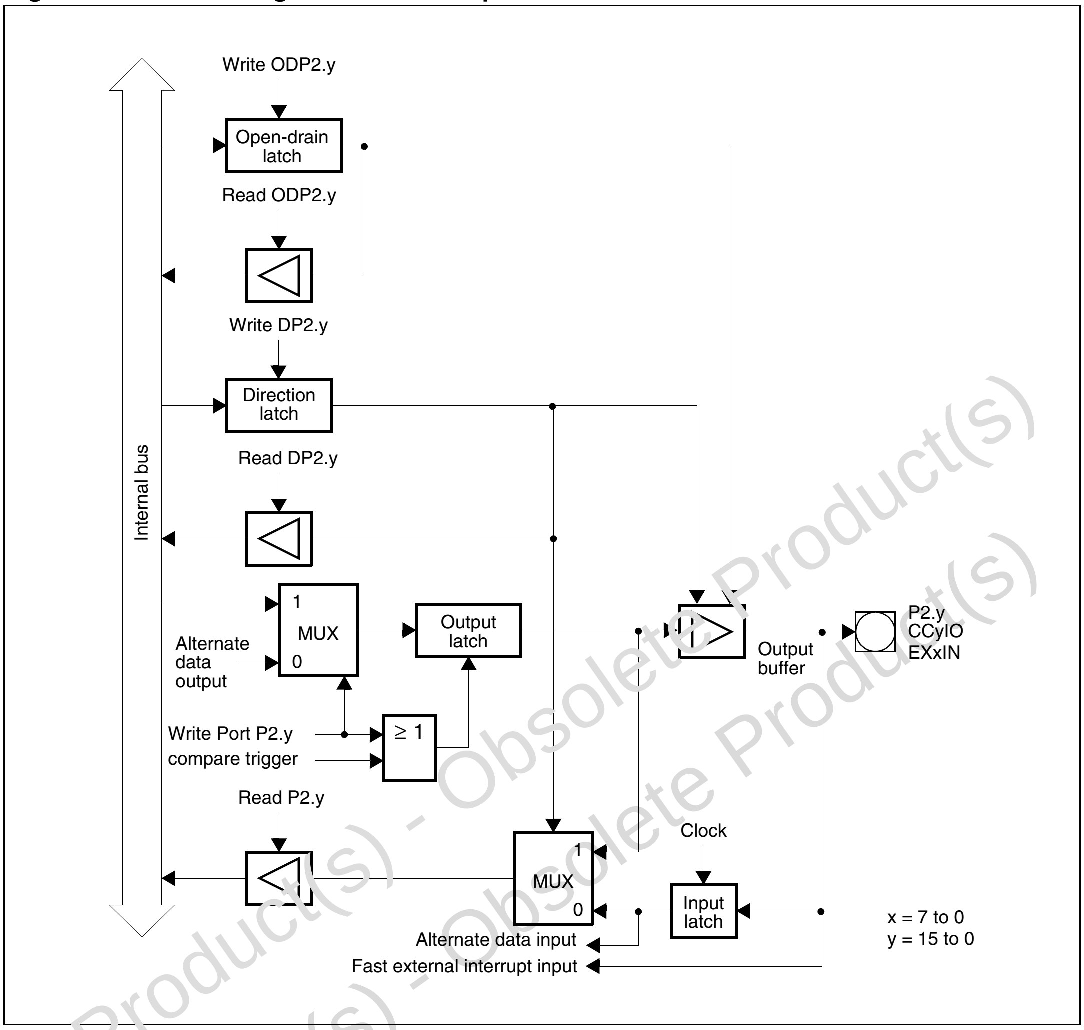
7.2 Instruction set summary

Table 45 lists the instructions of the ST10F296E. A detailed description of each instruction can be found in the ST10 family programming manual (PM0036).

Table 45. Instruction set summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2/4
ADDC(B)	Add word (byte) operands with carry	2/4
SUB(B)	Subtract word (byte) operands	2/4
SUBC(B)	Subtract word (byte) operands with carry	2/4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bit-wise AND, (word/byte operands)	2/4
OR(B)	Bit-wise OR, (word/byte operands)	2/4
XOR(B)	Bit-wise XOR, (word/byte operands)	2/4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bit-wise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2/4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2/4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2/4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2/4
MOVBS	Move byte operand to word operand with sign extension	2/4
MOVBZ	Move byte operand to word operand with zero extension	2/4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4

Figure 37. Block diagram of a Port 2 pin



XODP9CLR register

XODP9CLR (EB90h) XBus Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XODP9CLR.15	XODP9CLR.14	XODP9CLR.13	XODP9CLR.12	XODP9CLR.11	XODP9CLR.10	XODP9CLR.9	XODP9CLR.8	XODP9CLR.7	XODP9CLR.6	XODP9CLR.5	XODP9CLR.4	XODP9CLR.3	XODP9CLR.2	XODP9CLR.1	XODP9CLR.0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Table 110. XODP9CLR register description

Bit	Bit name	Function
15-0	XODP9CLR.y	Writing a 1 clears the corresponding bit of the XODP9.y register. Writing a 0 has no effect.

13.12 XPort 10

XPort 10 is enabled by setting the XPEN and XPORT10EN/XPORT9EN bits of the SYSCON and XPERCON registers respectively. On the XBus interface, the register are not bit-addressable. This 16-bit input port can only read data. There is no output latch and no direction register. Data written to XP10 are lost.

13.12.1 XPort 10 registers

XP10 register

XP10 (EBC0h) XBus Reset value: XXXXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XP10.15	XP10.14	XP10.13	XP10.12	XP10.11	XP10.10	XP10.9	XP10.8	XP10.7	XP10.6	XP10.5	XP10.4	XP10.3	XP10.2	XP10.1	XP10.0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 111. XP10 register description

Bit	Bit name	Function
15-0	XP10.y	Port data register XP10 bit y

Timer output

The trigger output, XADCINJ, is generated when the current value of the timer (XTCVR) matches the end value stored in the XTEVR register and when the output enable bit is set (XTCR.TOE = 1). If the output enable bit is reset, no event is generated regardless of the timer status (the XADINJ pin is kept at high impedance state).

The XADCINJ output trigger event is a positive pulse of 12 CPU clock cycles width (187 ns @64 MHz). To generate an ADC channel injection it has to be externally connected to the input P7.7/CC31 (CAPCOM2 capture/compare).

The ADC exclusively converts Port 5 or XPort 10 inputs. If one ‘y’ channel has to be used continuously in injection mode, it must be externally connected by hardware to Port5.y and XPort10.y inputs.

20.2 Asynchronous reset

An asynchronous reset is triggered when the RSTIN pin is pulled low while the RPD pin is at low level. The ST10F296E device is immediately (after the input filter delay) forced into a reset default state. It pulls the RSTOUT pin low, it cancels pending internal hold states (if any), it aborts all internal/external bus cycles, it switches buses (data, address and control signals) and I/O pin drivers to high-impedance, and it pulls the Port 0 pins high.

Note: If an asynchronous reset occurs in the internal memories during a read or write phase, the content of the memory itself could be corrupted. To avoid this, synchronous reset usage is strongly recommended.

20.2.1 Power-on reset

The asynchronous reset must be used during the power-on of the device. Depending on the crystal or resonator frequency, the on-chip oscillator needs about 1 ms to 10 ms to stabilize (refer to *Section 24: Electrical characteristics*), with an already stable V_{DD}. The logic of the ST10F296E does not need a stabilized clock signal to detect an asynchronous reset, so it is suitable for power-on conditions. To ensure a proper reset sequence, the RSTIN pin and the RPD pin must be held low until the device clock signal is stabilized and the system configuration value on Port 0 has settled.

At power-on, it is important to respect some additional constraints introduced by the start-up phase of the different embedded modules.

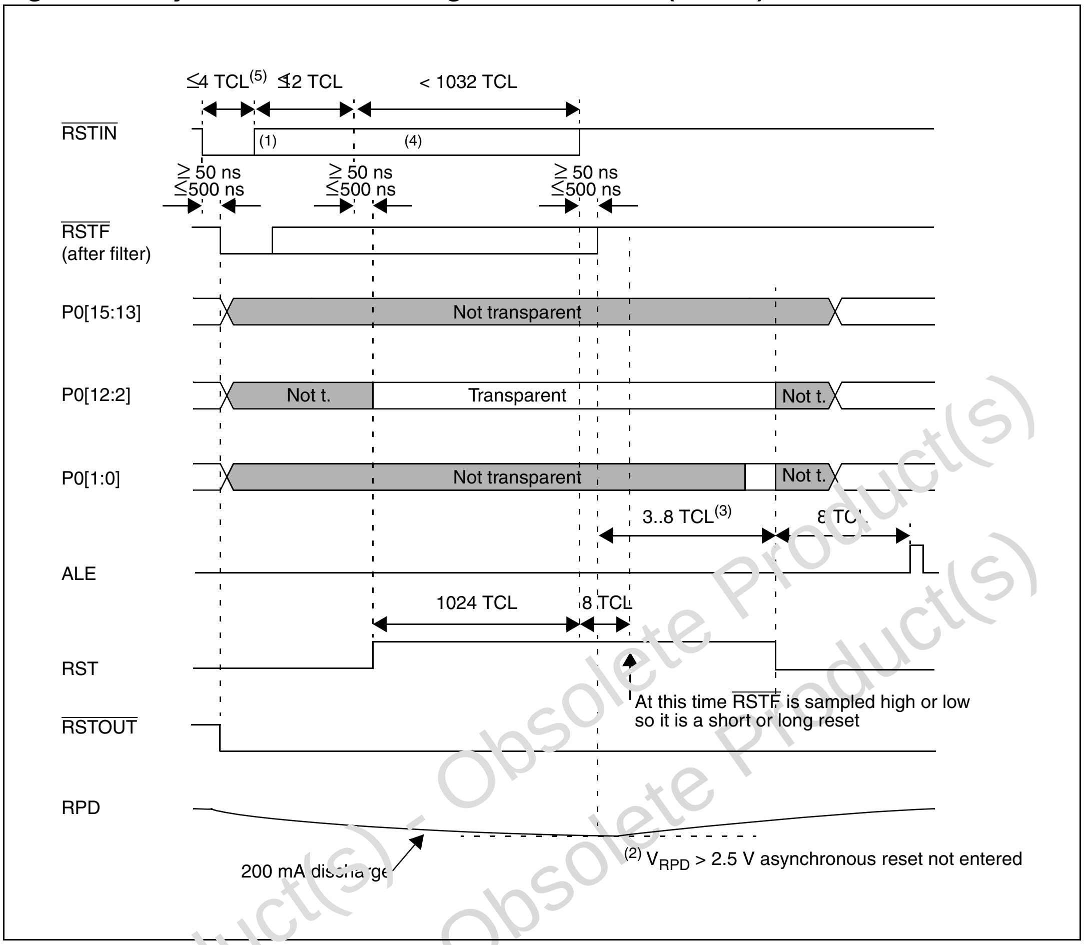
In particular, the on-chip voltage regulator needs at least 1 ms to stabilize the internal 1.8 V for the core logic. This time is computed from when the external reference (V_{DD}) becomes stable inside the specification range (that is at least 4.5 V). This is a constraint for the application hardware (external voltage regulator). The RSTIN pin assertion must be extended to guarantee the voltage regulator stabilization.

A second constraint is imposed by the embedded Flash. When booting from the internal memory, starting from the RSTIN pin being released, the Flash needs a maximum of 1 ms for its initialization. Before this, the internal reset (RST signal) is not released, so the CPU does not start code execution in internal memory.

Note: The above is not true if the external memory is used (pin EA held low during reset phase). In this case, once the RSTIN pin is released, and after a few CPU clock (filter delay plus 3...8 TCL), the internal reset signal RST is released, afterwhich code execution can start immediately. Eventual access to the data in the internal Flash is forbidden before its initialization phase is complete. An eventual access during the starting phase returns FFFFh at the beginning and 009Bh later on (an illegal opcode trap can be generated).

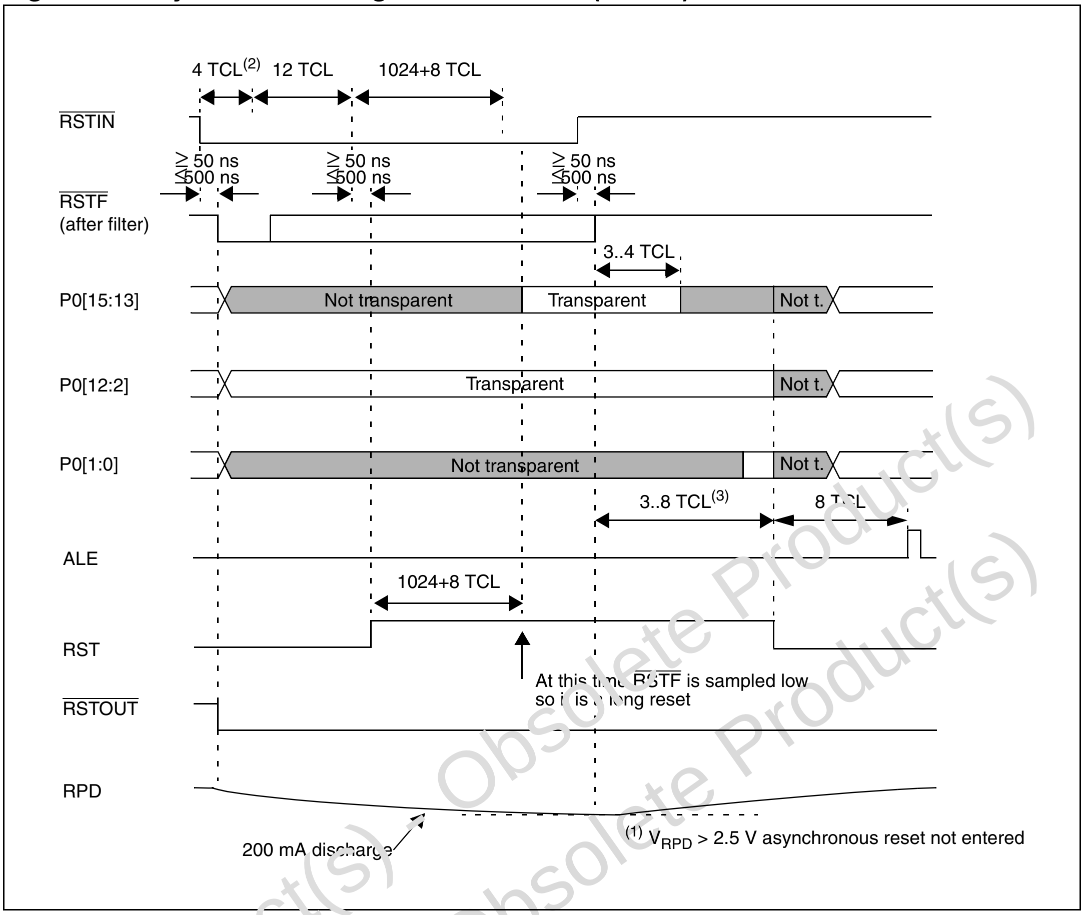
At power-on, the RSTIN pin must be tied low for a minimum period of time that includes the start-up time of the main oscillator (t_{STUP} = 1 ms for the resonator, 10 ms for the crystal) and the PLL synchronization time (t_{PSUP} = 200 µs). Consequently, if the internal Flash is used, the RSTIN pin could be released to recover some time in the start-up phase (Flash initialization needs a stable V_{18}, but, does not need a stable system clock since an internal dedicated oscillator is used) before the main oscillator and PLL are stable.

Figure 80. Synchronous short/long hardware reset (EA = 0)



1. RSTIN assertion can be released here. See *Section 21.1: Idle mode on page 240* for details on minimum pulse duration.
2. If RPD voltage drops below the threshold voltage (about 2.5 V for 5 V operation) during the reset condition (RSTIN low), an asynchronous reset is entered immediately.
3. Three to eight TCL depending on clock source selection.
4. The RSTIN pin is pulled low if the BDRSTEN bit (of the SYSCON register) was previously set by software. The BDRSTEN bit is cleared after reset.
5. The minimum RSTIN low pulse duration must be longer than 500 ns, to guarantee the pulse is not masked by the internal filter (see *Section 21.1: Idle mode on page 240*).

Figure 82. Synchronous long hardware reset ($\overline{EA}$ = 0)



1. If RPD voltage drops below the threshold voltage (about 2.5 V for 5 V operation) during the reset condition ($\overline{RSTIN}$ low), an asynchronous reset is entered immediately.
2. The minimum $\overline{RSTIN}$ low pulse duration must be longer than 500 ns, to guarantee the pulse is not masked by the internal filter (see *Section 21.1: Idle mode on page 240*).
3. Three to eight TCL depending on clock source selection.

20.4 Software reset

A software reset sequence can be triggered at any time by the protected SRST (software reset) instruction. This instruction can be executed within a program, for example: On a hardware trap that reveals system failure or to leave bootstrap loader mode.

On execution of the SRST instruction, the internal reset sequence is started. The microcontroller behavior is the same as for a synchronous short reset, except that only bits P0.12...P0.8 are latched at the end of the reset sequence, while previously latched, bits P0.7...P0.2 are cleared (written at 1).

A software reset is always taken as synchronous. There is no influence on software reset behavior with RPD status. If a bidirectional reset is selected, a software reset event pulls the $\overline{RSTIN}$ pin low. This occurs only if RPD is high. If RPD is low, the $\overline{RSTIN}$ pin is not pulled low even though a bidirectional reset is selected.

See *Figure 83* and *Figure 84* which shows unidirectional software reset timing. See *Figure 85*, *Figure 86*, and *Figure 87* for bidirectional software reset timing.

21.2.1 Protected power-down mode

This mode is selected when the PWDCFG bit of the SYSCON register is cleared. Protected power-down mode is only activated if the $\overline{NMI}$ pin is pulled low when executing the PWRDN instruction. This mode is only deactivated with an external hardware reset on the $\overline{RSTIN}$ pin.

21.2.2 Interruptible power-down mode

This mode is selected when the PWDCFG bit of the SYSCON register is set (see *Section 23: Register set on page 248*).

Interruptible power-down mode is only activated if all the enabled fast external interrupt pins are at their inactive level (see *Table 134: EXICON register description*).

This mode is deactivated with an external reset applied to the $\overline{RSTIN}$ pin, with an interrupt request applied to one of the fast external interrupt pins, with an interrupt generated by the RTC, or with an interrupt generated by activity on the interfaces of the CAN and I²C modules. To allow the internal PLL and clock to stabilize, the $\overline{RSTIN}$ pin must be held low according the recommendations described in *Section 20: System reset*.

EXICON register

EXICON (F1C0h/E0h) ESFR Reset value: 0000h

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
EXI7ES	EXI6ES	EXI5ES	EXI4ES	EXI3ES	EXI2ES	EXI1ES	EXI0ES
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 134. EXICON register description

Bit	Bit name	Function
15:0	EXIxES	External interrupt x edge selection field (x = 7...0) 00: Fast external interrupts disabled (referred to as standard mode). The EXxIN pin is not taken into account for entering/exiting power-down mode. 01: Interrupt on positive edge (rising). Power-down mode is entered if EXiIN = 0 and exited if EXxIN = 1 (referred to as 'high' active level). 10: Interrupt on negative edge (falling). Power-down mode is entered if EXiIN = 1 and exited if EXxIN = 0 (referred to as 'low' active level). 11: Interrupt on any edge (rising or falling). Power-down mode is always entered and is exited if EXxIN level changes.

EXxIN inputs are normally sampled interrupt inputs. However, the power-down mode circuitry uses them as level-sensitive inputs.

An EXxIN (x = 3...0) interrupt enable bit (bit CCxIE in the CCxIC register) does not need to be set to bring the device out of power-down mode. An external RC circuit must be connected to the RPD pin, as shown in *Figure 93*.

Table 140. SFRs ordered by name (continued)

Name	Physical address	8-bit address	Description	Reset value
CC23IC **(b)**	F16Eh **(E)**	B7h	CAPCOM register 23 interrupt control register	--00h
CC24	FE70h	38h	CAPCOM register 24	0000h
CC24IC **(b)**	F170h **(E)**	B8h	CAPCOM register 24 interrupt control register	--00h
CC25	FE72h	39h	CAPCOM register 25	0000h
CC25IC **(b)**	F172h **(E)**	B9h	CAPCOM register 25 interrupt control register	--00h
CC26	FE74h	3Ah	CAPCOM register 26	0000h
CC26IC **(b)**	F174h **(E)**	BAh	CAPCOM register 26 interrupt control register	--00h
CC27	FE76h	3Bh	CAPCOM register 27	0000h
CC27IC **(b)**	F176h **(E)**	BBh	CAPCOM register 27 interrupt control register	--00h
CC28	FE78h	3Ch	CAPCOM register 28	0000h
CC28IC **(b)**	F178h **(E)**	BCh	CAPCOM register 28 interrupt control register	--00h
CC29	FE7Ah	3Dh	CAPCOM register 29	0000h
CC29IC **(b)**	F184h **(E)**	C2h	CAPCOM register 29 interrupt control register	--00h
CC30	FE7Ch	3Eh	CAPCOM register 30	0000h
CC30IC **(b)**	F18Ch **(E)**	C6h	CAPCOM register 30 interrupt control register	--00h
CC31	FE7Eh	3Fh	CAPCOM register 31	0000h
CC31IC **(b)**	F194h **(E)**	CAh	CAPCOM register 31 interrupt control register	--00h
CCM0 **(b)**	FF52h	A9h	CAPCOM mode control register 0	0000h
CCM1 **(b)**	FF54h	AAh	CAPCOM mode control register 1	0000h
CCM2 **(b)**	FF56h	ABh	CAPCOM mode control register 2	0000h
CCM3 **(b)**	FF58h	ACh	CAPCOM mode control register 3	0000h
CCM4 **(b)**	FF22h	91h	CAPCOM mode control register 4	0000h
CCM5 **(b)**	FF24h	92h	CAPCOM mode control register 5	0000h
CCM6 **(b)**	FF26h	93h	CAPCOM mode control register 6	0000h
CCM7 **(b)**	FF28h	94h	CAPCOM mode control register 7	0000h
CP	FE10h	08h	CPU context pointer register	FC00h
CRIC **(b)**	FF6Ah	B5h	GPT2 CAPREL interrupt control register	--00h
CSP	FE08h	04h	CPU code segment pointer register (read-only)	0000h
DP0L **(b)**	F100h **(E)**	80h	P0L direction control register	--00h
DP0H **(b)**	F102h **(E)**	81h	P0h direction control register	--00h
DP1L **(b)**	F104h **(E)**	82h	P1L direction control register	--00h
DP1H **(b)**	F106h **(E)**	83h	P1h direction control register	--00h
DP2 **(b)**	FFC2h	E1h	Port 2 direction control register	0000h
DP3 **(b)**	FFC6h	E3h	Port 3 direction control register	0000h

IDMEM register

IDMEM (F07Ah/3Dh) ESFR Reset value: 30D0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEMTYP				MEMSIZE											
R				R											

Table 148. IDMEM register description

Bit	Bit name	Function
15-12	MEMTYP	Internal memory type 0h: ROM-less 1h: (M) ROM memory 2h: (S) Standard Flash memory 3h: (H) High performance Flash memory (ST10F296E) 4h...Fh: Reserved
11 - 0	MEMSIZE	Internal memory size Internal memory size is 4 x (MEMSIZE) (in Kbyte). The 0D0h for the ST10F296E is 832 Kbytes

IDPROG register

IDPROG (F078h/3Ch) ESFR Reset value: 0040h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGVPP								PROGVDD							
R								R							

Table 149. IDPROG register description

Bit	Bit name	Function
15-8	PROGVPP	Programming V_{PP} voltage (no need of external V_{PP}) - 00h No need for external V_{PP} (00h)
7-0	PROGVDD	Programming V_{DD} voltage When programming EPROM or Flash devices, V_{DD} voltage is calculated using the following formula for 5 V ST10F296E devices: V_{DD} = 20 x [PROGVDD] / 256 (volts) - 40h

Note: All identification registers are read-only registers.

The values written inside different identification register bits are valid only after the Flash initialization phase has been completed. When code execution starts from the internal memory (pin $\overline{EA}$ held high during reset), the Flash has completed initialization and the identification register bits can be read. When code execution starts from the external memory (pin $\overline{EA}$ held low during reset), Flash initialization has not been completed and the identification register bits cannot be read. The user can poll bits 15 and 14 of the IDMEM register. When both these bits are read low, Flash initialization can be completed and all identification register bits can be read.

EXICON register

EXICON (F1C0h/E0h) ESFR Reset value: 0000h

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
EXI7ES	EXI6ES	EXI5ES	EXI4ES	EXI3ES(1)(2)	EXI2ES(1)(3)	EXI1ES	EXI0ES
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. EXI2ES and EXI3ES must be configured as 01b because RTC interrupt request lines are rising edge active.
2. Alarm interrupt request line (RTCAI) is linked with EXI3ES
3. Timed interrupt request line (RTCSI) is linked with EXI2ES

Table 153. EXICON register description

Bit	Bit name	Function
15-0	EXIxES (x = 7 to 0)	External interrupt x edge selection field (x = 7...0) 00: Fast external interrupts disabled (standard mode). EXxIN pin not taken into account for entering/exiting power-down mode. 01: Interrupt on positive rising edge. Power-down mode is entered if EXiIN = 0 and exited if EXxIN = 1 (referred as 'high' active level). 10: Interrupt on negative falling edge. Power-down mode is entered if EXiIN = 1 and exited if EXxIN = 0 (referred as 'low' active level). 11: Interrupt on any edge (rising or falling). Power-down mode is always entered, it is exited if the EXxIN level changes.

Table 181. PBGA 208 (23 x 23 x 1.96 mm) mechanical data

Dimensions	Millimeters			Inches (approx)(1)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A		1.960			0.0772	
A1	0.500	0.600	0.700	0.0197	0.0236	0.0276
A2		1.360			0.0535	
A3		0.560			0.0220	
ϕ b	0.600	0.760	0.900	0.0236	0.0299	0.0354
D	22.900	23.000	23.100	0.9016	0.9055	0.9094
D1		20.320			0.8000	
E	22.900	23.000	23.100	0.9016	0.9055	0.9094
E1		20.320			0.8000	
e		1.270			0.0500	
f	1.240	1.340	1.440	0.0488	0.0528	0.0567

1. Values in inches are converted from mm and rounded to four decimal digits.

27 Revision history

Table 183. Document revision history

Date	Revision	Changes
24-Jan-2005	1	Initial release.
20-Oct-2008	2	Initial public release. Document reformatted; content of *Features* reworked to fit into one page (no technical changes); content of remaining document reworked to improve readability (no technical changes). Updated *Table 1: Device summary*. *Section 7: Central processing unit (CPU)*: Removed sections on the SYSCON register and MAC features; amended *Section 7.3*; removed table entitled *MAC coprocessor specific instructions* and replaced with *Table 46*; removed tables entitled *Pointer postmodification combinations for Rwn and IDXi* and *MAC registers referenced as 'CoReg'*. *Section 9: Interrupt system*: Updated introductory text; removed sections on *Extrenal interrupts* and *Interrupt control register*; removed some text from *Section 9.1: XPeripheral interrupt*. *Section 24: Electrical characteristics*: Updated *Table 164*, *Table 172*, *Table 176*, *Figure 99*, and *Figure 120*. *Section 25: Package mechanical data*: Added ECOPACK text. *Table 181: PBGA 208 (23 x 23 x 1.96 mm) mechanical data*: Converted values in inches to four decimal places.