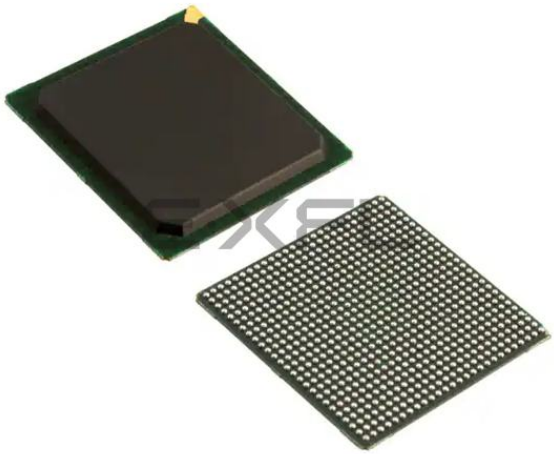

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4160
Number of Logic Elements/Cells	37440
Total RAM Bits	1548288
Number of I/O	519
Number of Gates	1800000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3sd1800a-4fgg676i

Table 1: **Summary of XA Spartan-3A DSP FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM Bits (1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XA3SD1800A	1800K	37,440	88	48	4,160	16,640	260K	1512K	84	8	519	227
XA3SD3400A	3400K	53,712	104	58	5,968	23,872	373K	2268K	126	8	469	213

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

Refer to DS610, *Spartan-3A DSP FPGA Family Data Sheet* for a full product description, AC and DC specifications, and package pinout descriptions. Any values shown specifically in this XA Spartan-3A DSP Automotive FPGA Family data sheet override those shown in DS610.

For information regarding reliability qualification, refer to RPT103, *Xilinx Spartan-3A Family Automotive Qualification Report* and RPT070, *Spartan-3A Commercial Qualification Report*. Contact your local Xilinx representative for more details on these reports.

Key Feature Differences from Commercial XC Devices

- AEC-Q100 device qualification and full production part approval process (PPAP) documentation support available in both extended temperature I- and Q-Grades
- Guaranteed to meet full electrical specifications over the T_J = –40°C to +125°C temperature range (Q-Grade)
- XA Spartan-3A DSP devices are available in the -4 speed grade only
- PCI-66 and PCI-X are not supported in the XA Spartan-3A DSP FPGA product line
- Platform Flash is not supported within the XA family
- XA Spartan-3A DSP devices are available in Pb-free packaging only
- MultiBoot is not supported in XA versions of this product.
- The XA Spartan-3A DSP device must be power cycled prior to reconfiguration.

Architectural Overview

The XA Spartan-3A DSP family architecture consists of five fundamental programmable functional elements:

- **XtremeDSP DSP48A Slice** provides an 18-bit x 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications.
- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kb dual-port blocks.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. The XA3SD1800A has four columns of DSP48A slices, and the XA3SD3400A has five columns of DSP48A slices. Each DSP48A has an associated block RAM. The DCMs are positioned in the center with two at the top and two at the bottom of the device and in the two outer columns of the four or five columns of block RAM and DSP48As.

The XA Spartan-3A DSP family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

DC Electrical Characteristics

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the published parameter values apply to all XA Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both I-Grade and Q-Grade.

Absolute Maximum Ratings

Stresses beyond those listed under Table 4, *Absolute Maximum Ratings* might cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Table 13: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}[2]		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25[3]	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33[3]	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25[4]	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25[3]	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33[3]	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25[5]	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33[5]	Inputs Only			100	800	1000	0.3	1.2	2.8[6]
RSDS_25[3]	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33[3]	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33[3,4,7]	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25[3]	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33[3]	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18[8]	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68		0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II[8]	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II[8]	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See External Termination Requirements for Differential I/O, page 16.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX} = 3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} - (V_{ID}/2)$.
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. $(V_{CCAUX} - 300\ mV) \le V_{ICM} \le (V_{CCAUX} - 37\ mV)$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. V_{REF} inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The V_{REF} settings are the same as for the single-ended versions in Table 11. Other differential standards do not use V_{REF}.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 18: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Max	
Clock-to-Output Times					
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	XA3SD1800A	3.51	ns
			XA3SD3400A	3.82	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	XA3SD1800A	5.58	ns
			XA3SD3400A	6.13	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 23. If the latter is true, *add* the appropriate Output adjustment from Table 26.
3. DCM output jitter is included in all measurements.

Pin-to-Pin Setup and Hold Times

Table 19: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Min	
Setup Times					
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XA3SD1800A	3.11	ns
			XA3SD3400A	2.49	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 6, without DCM	XA3SD1800A	3.39	ns
			XA3SD3400A	3.08	ns
Hold Times					
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XA3SD1800A	–0.38	ns
			XA3SD3400A	–0.26	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 6, without DCM	XA3SD1800A	–0.71	ns
			XA3SD3400A	–0.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 23. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 23. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Output Timing Adjustments

Table 26: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below	Units
			Speed Grade: -4	
Single-Ended Standards				
LVTTL	Slow	2 mA	5.58	ns
		4 mA	3.44	ns
		6 mA	3.44	ns
		8 mA	2.26	ns
		12 mA	1.66	ns
		16 mA	1.29	ns
		24 mA	2.97	ns
	Fast	2 mA	3.37	ns
		4 mA	2.26	ns
		6 mA	2.26	ns
		8 mA	0.62	ns
		12 mA	0.61	ns
		16 mA	0.59	ns
		24 mA	0.60	ns
	QuietIO	2 mA	27.67	ns
		4 mA	27.67	ns
		6 mA	27.67	ns
		8 mA	16.71	ns
		12 mA	16.67	ns
		16 mA	16.22	ns
		24 mA	12.11	ns

Table 26: **Output Timing Adjustments for IOB *(Cont'd)***

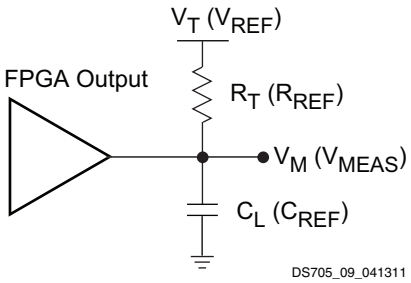
Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below	Units
			Speed Grade: -4	
LVCMOS33	Slow	2 mA	5.58	ns
		4 mA	3.30	ns
		6 mA	3.30	ns
		8 mA	2.26	ns
		12 mA	1.29	ns
		16 mA	1.21	ns
		24 mA	2.79	ns
	Fast	2 mA	3.72	ns
		4 mA	2.04	ns
		6 mA	2.08	ns
		8 mA	0.53	ns
		12 mA	0.59	ns
		16 mA	0.59	ns
		24 mA	0.51	ns
	QuietIO	2 mA	27.67	ns
		4 mA	27.67	ns
		6 mA	27.67	ns
		8 mA	16.71	ns
		12 mA	16.29	ns
		16 mA	16.18	ns
		24 mA	12.11	ns

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 27 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 9. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1 MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 9: **Output Test Setup**

Table 27: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		–	0	3.3	1M	0	1.4
LVCMOS33		–	0	3.3	1M	0	1.65
LVCMOS25		–	0	2.5	1M	0	1.25
LVCMOS18		–	0	1.8	1M	0	0.9
LVCMOS15		–	0	1.5	1M	0	0.75
LVCMOS12		–	0	1.2	1M	0	0.6
PCI33_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 27 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 9. Use parameter values V_T, R_T, and V_M from Table 27. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 26) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 28 and Table 29 provide the essential SSO guidelines. For each device/package combination, Table 28 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and may not match the physical number of pairs. For each output signal standard and drive strength, Table 29 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 29 are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from Table 28 and Table 29 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 28 x Table 29

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics.

Table 28: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	Package Style *(Pb-free)*	
	CSG484	FGG676
XA3SD1800A	6	9
XA3SD3400A	6	10

Table 29: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX}=3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type: CSG484 and FGG676	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
LVCMOS33	Slow	2	76	76
		4	46	46
		6	27	27
		8	20	20
		12	13	13
		16	10	10
		24	–	9
	Fast	2	10	10
		4	8	8
		6	5	5
		8	4	4
		12	4	4
		16	2	2
		24	–	2
	QuietIO	2	76	76
		4	46	46
		6	32	32
		8	26	26
		12	18	18
		16	14	14
		24	–	10

DSP48A Timing

To reference the DSP48A block diagram, see the *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide* (UG431).

Table 35: **Setup Times for the DSP48A**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade: -4	Units
					Min	
Setup Times of Data/Control Pins to the Input Register Clock						
T_{DSPDCK_AA}	A input to A register CLK	–	–	–	0.04	ns
T_{DSPDCK_DB}	D input to B register CLK	Yes(1)	–	–	1.88	ns
T_{DSPDCK_CC}	C input to C register CLK	–	–	–	0.05	ns
T_{DSPDCK_DD}	D input to D register CLK	–	–	–	0.04	ns
T_{DSPDCK_OPB}	OPMODE input to B register CLK	Yes	–	–	0.42	ns
T_{DSPDCK_OPOP}	OPMODE input to OPMODE register CLK	–	–	–	0.06	ns
Setup Times of Data Pins to the Pipeline Register Clock						
T_{DSPDCK_AM}	A input to M register CLK	–	Yes	–	3.79	ns
T_{DSPDCK_BM}	B input to M register CLK	Yes	Yes	–	4.97	ns
		No	Yes	–	3.79	ns
T_{DSPDCK_DM}	D input to M register CLK	Yes	Yes	–	5.06	ns
T_{DSPDCK_OPM}	OPMODE to M register CLK	Yes	Yes	–	5.42	ns
Setup Times of Data/Control Pins to the Output Register Clock						
T_{DSPDCK_AP}	A input to P register CLK	–	Yes	Yes	5.49	ns
T_{DSPDCK_BP}	B input to P register CLK	Yes	Yes	Yes	6.74	ns
		No	Yes	Yes	5.48	ns
T_{DSPDCK_DP}	D input to P register CLK	Yes	Yes	Yes	6.83	ns
T_{DSPDCK_CP}	C input to P register CLK	–	–	Yes	2.18	ns
T_{DSPDCK_OPP}	OPMODE input to P register CLK	Yes	Yes	Yes	7.18	ns

Notes:

1. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
2. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 36: **Clock to Out, Propagation Delays, and Maximum Frequency for the DSP48A**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade: -4	Units
					Min	
Clock to Out from Output Register Clock to Output Pin						
T_{DSPCKO_PP}	CLK (PREG) to P output	–	–	–	1.44	ns
Clock to Out from Pipeline Register Clock to Output Pins						
T_{DSPCKO_PM}	CLK (MREG) to P output	–	Yes(1)	Yes	3.63	ns
		–	Yes	No	2.23	ns
Clock to Out from Input Register Clock to Output Pins						
T_{DSPCKO_PA}	CLK (AREG) to P output	–	Yes	Yes	7.27	ns
T_{DSPCKO_PB}	CLK (BREG) to P output	Yes	Yes	Yes	8.56	ns
T_{DSPCKO_PC}	CLK (CREG) to P output	–	–	Yes	3.87	ns
T_{DSPCKO_PD}	CLK (DREG) to P output	Yes	Yes	Yes	8.42	ns
Combinatorial Delays from Input Pins to Output Pins						
T_{DSPDO_AP} T_{DSPDO_BP}	A or B input to P output	–	No	Yes	3.19	ns
		–	Yes	No	5.28	ns
		–	Yes	Yes	6.49	ns
T_{DSPDO_BP}	B input to P output	Yes	No	No	4.01	ns
		Yes	Yes	No	6.65	ns
		Yes	Yes	Yes	7.74	ns
T_{DSPDO_CP}	C input to P output	–	–	Yes	3.17	ns
T_{DSPDO_DP}	D input to P output	Yes	Yes	Yes	7.82	ns
T_{DSPDO_OPP}	OPMODE input to P output	Yes	Yes	Yes	8.18	ns
Maximum Frequency						
F_{MAX}	All registers used	Yes	Yes	Yes	250	MHz

Notes:

1. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
2. To reference the DSP48A block diagram, see UG431, *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide*.
3. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 38: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade: -4		Units
				Min	Max	
Output Frequency Ranges						
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs		All	5	250	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs			5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs			10	334	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output			0.3125	166	MHz
Output Clock Jitter(2,3,4)						
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±[0.5% of CLKIN period + 100]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±[0.5% of CLKIN period + 100]	ps
Duty Cycle(4)						
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKIN period + 350]	ps
Phase Alignment(4)						
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		–	±[1% of CLKIN period + 100]	ps
		All others		–	±[1% of CLKIN period + 150]	ps
Lock Time						
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	–	5	ms
		F_{CLKIN} > 15 MHz		–	600	µs
Delay Lines						
DCM_DELAY_STEP(5)	Finest delay resolution, averaged over all steps		All	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 37.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps, averaged over all steps.
5. The typical delay step size is 23 ps.

Miscellaneous DCM Timing

Table 43: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

DNA Port Timing

Table 44: **DNA_PORT Interface Timing**

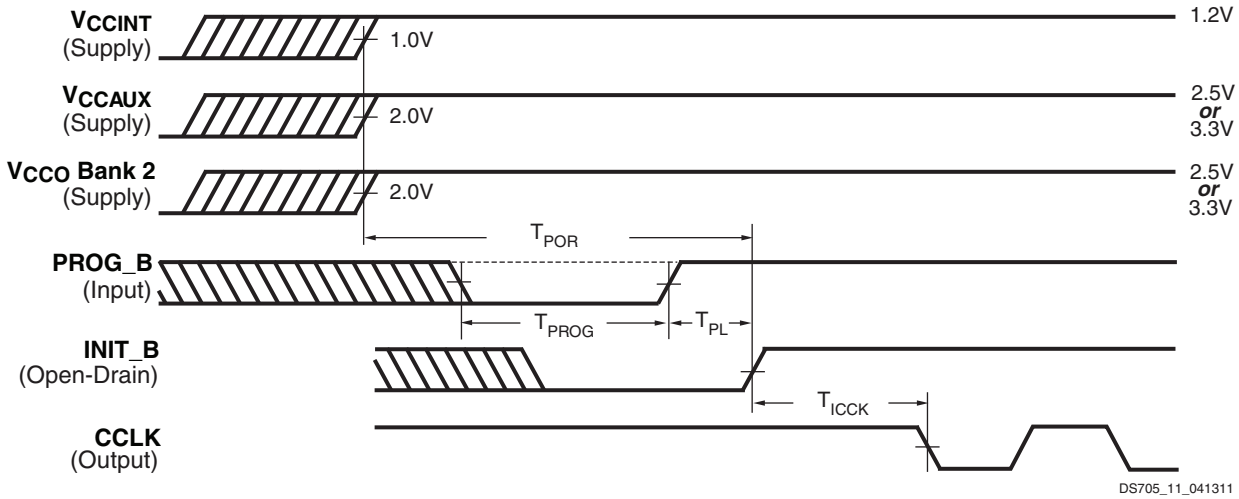
Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0.0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0.0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, and the maximum READ pulse width is 10 µs.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 – M2).

Figure 11: **Waveforms for Power-On and the Beginning of Configuration**

Table 46: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	Min	Max	Units
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	All	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	300	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the SPI and BPI modes.
4. For details on configuration, see UG332, *Spartan-3 Generation Configuration User Guide*.

Configuration Clock (CCLK) Characteristics

Table 47: **CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by *ConfigRate* setting	1 *(power-on value)*	I-Grade/ Q-Grade	1,180	2,500	ns
T_{CCLK3}		3	I-Grade/ Q-Grade	390	833	ns
T_{CCLK6}		6	I-Grade/ Q-Grade	195	417	ns
T_{CCLK7}		7	I-Grade/ Q-Grade	168	357	ns
T_{CCLK8}		8	I-Grade/ Q-Grade	147	313	ns
T_{CCLK10}		10	I-Grade/ Q-Grade	116	250	ns
T_{CCLK12}		12	I-Grade/ Q-Grade	97	208	ns
T_{CCLK13}		13	I-Grade/ Q-Grade	88	192	ns
T_{CCLK17}		17	I-Grade/ Q-Grade	68	147	ns
T_{CCLK22}		22	I-Grade/ Q-Grade	51	114	ns
T_{CCLK25}		25	I-Grade/ Q-Grade	45	100	ns
T_{CCLK27}		27	I-Grade/ Q-Grade	42	93	ns
T_{CCLK33}		33	I-Grade/ Q-Grade	34	76	ns
T_{CCLK44}		44	I-Grade/ Q-Grade	25	57	ns
T_{CCLK50}		50	I-Grade/ Q-Grade	21	50	ns
$T_{CCLK100}$		100	I-Grade/ Q-Grade	10.6	25	ns

Notes:

1. Set the *ConfigRate* option value when generating a configuration bitstream.

Slave Serial Mode Timing

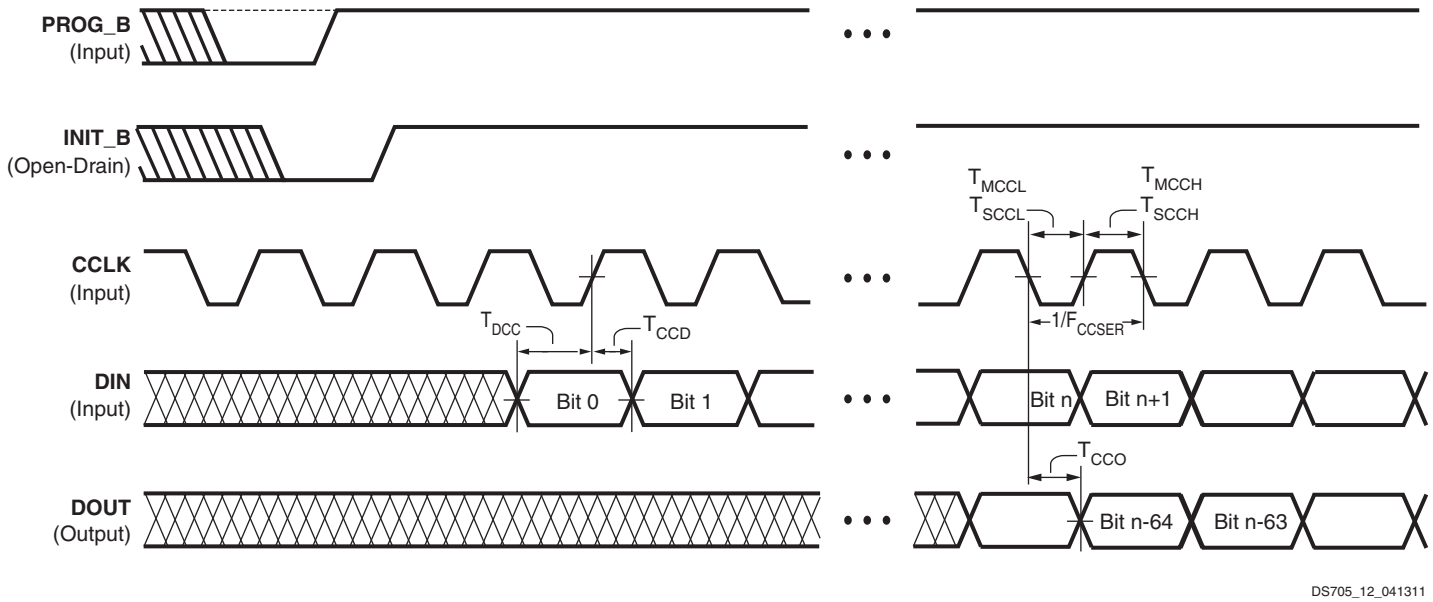


Figure 12: **Waveforms for Slave Serial Configuration**

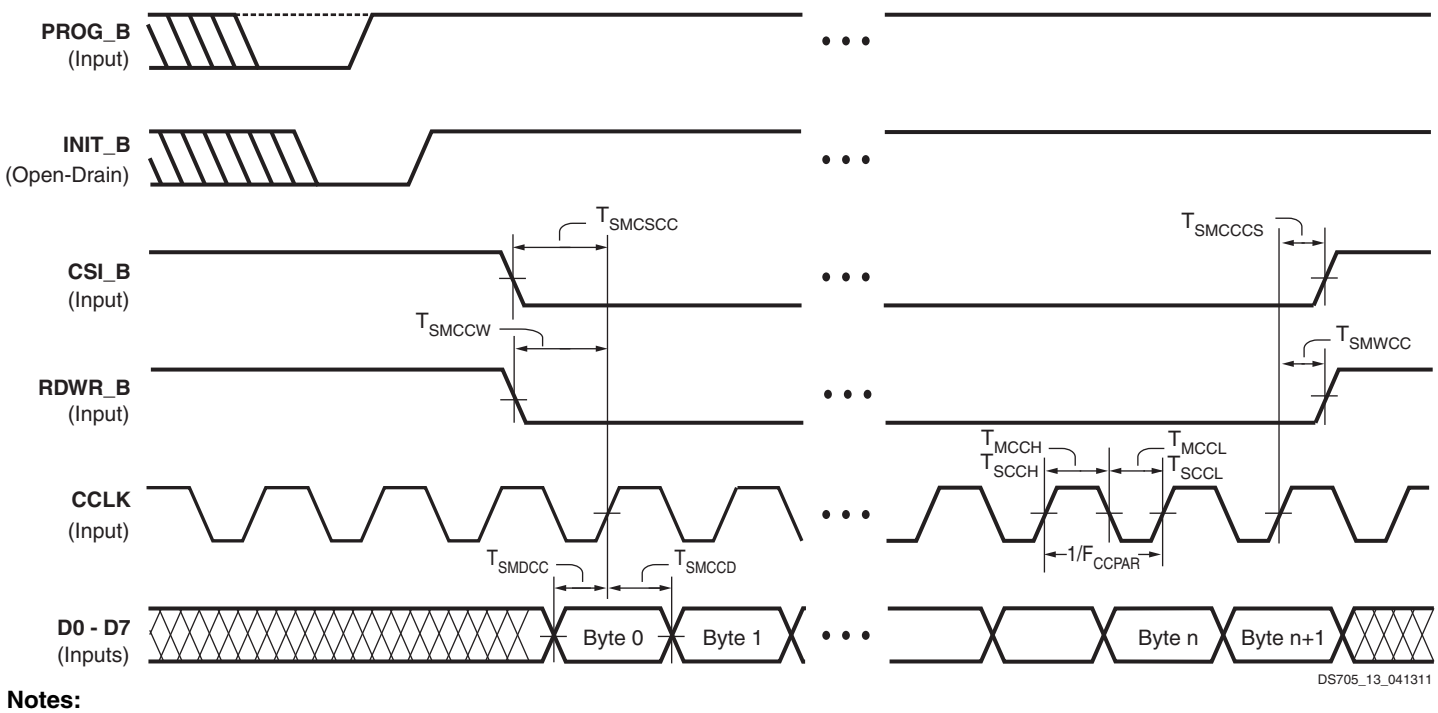
Table 51: **Timing for the Slave Serial Configuration Modes**

Symbol	Description		Min	Max	Units
Clock-to-Output Times					
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		1.5	10	ns
Setup Times					
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		7	–	ns
Hold Times					
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		1.0	–	ns
Clock Timing					
T_{CCH}	High pulse width at the CCLK input pin		See Table 50		
T_{CCL}	Low pulse width at the CCLK input pin		See Table 50		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	100	MHz
		With bitstream compression	0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0 - D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0 - D7 bus.
2. To pause configuration, pause CCLK instead of deasserting CSI_B. See the section in Chapter 7 called “Non-Continuous SelectMAP Data Loading” in UG332 for more details.

Figure 13: **Waveforms for Slave Parallel Configuration**

Table 52: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		Min	Max	Units
Setup Times					
T_{SMDCC} (2)	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		17	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Serial Peripheral Interface Configuration Timing

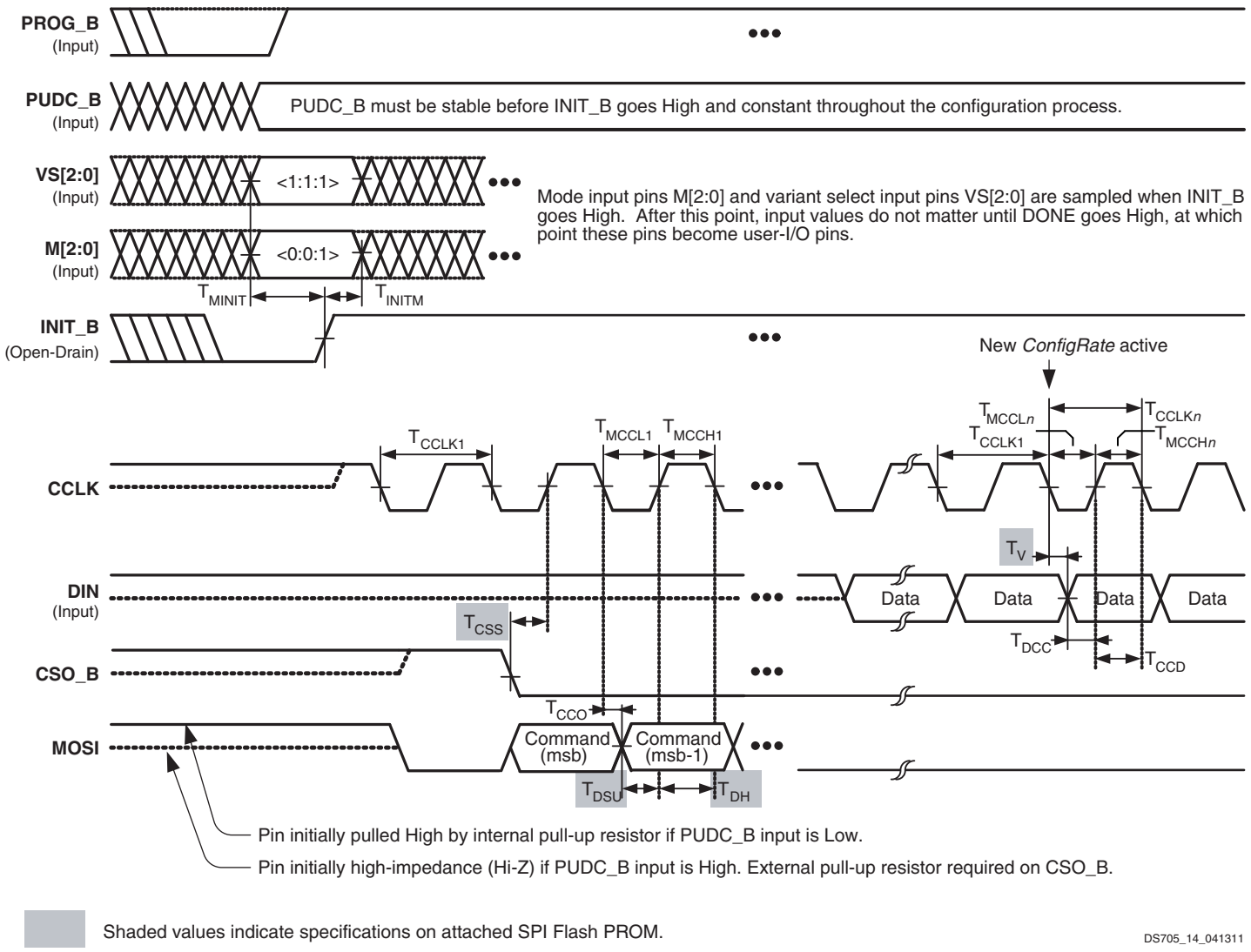


Figure 14: **Waveforms for Serial Peripheral Interface Configuration**

Table 53: **Timing for Serial Peripheral Interface Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 47		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 47		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling edge	See Table 51		
T_{DCC}	Setup time on DIN data input before CCLK rising edge	See Table 51		
T_{CCD}	Hold time on DIN data input after CCLK rising edge	0	–	ns

Table 54: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Byte Peripheral Interface Configuration Timing

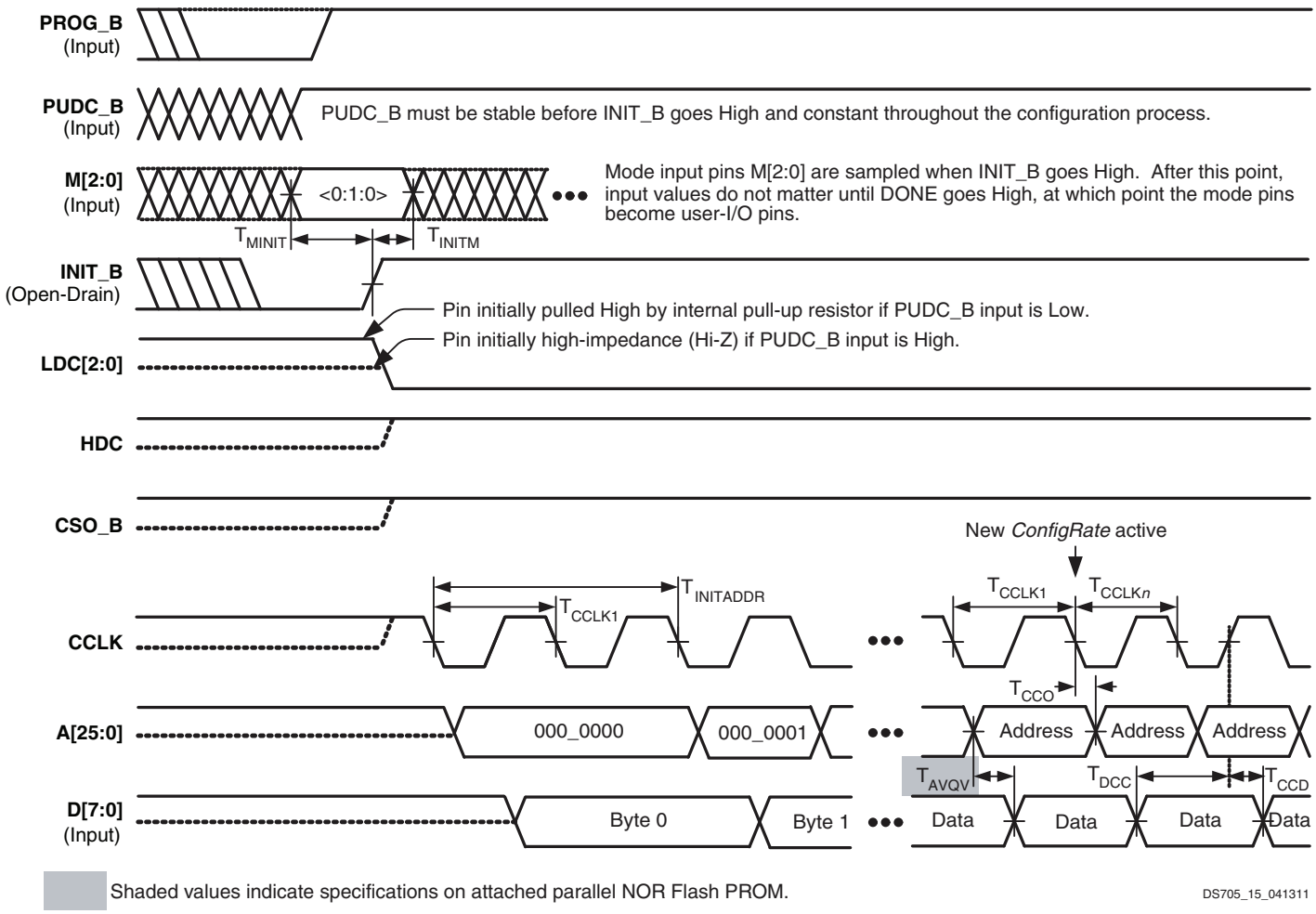


Figure 15: **Waveforms for Byte-wide Peripheral Interface Configuration**

Table 55: **Timing for Byte-wide Peripheral Interface Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 47		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 47		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 51		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 52		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	–	ns