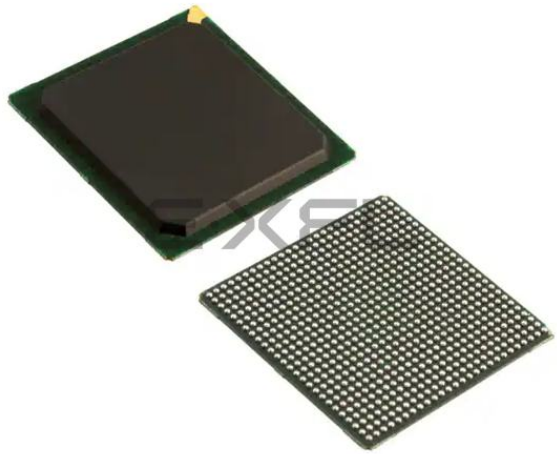

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4160
Number of Logic Elements/Cells	37440
Total RAM Bits	1548288
Number of I/O	519
Number of Gates	1800000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3sd1800a-4fgg676q

Table 1: **Summary of XA Spartan-3A DSP FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM Bits (1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XA3SD1800A	1800K	37,440	88	48	4,160	16,640	260K	1512K	84	8	519	227
XA3SD3400A	3400K	53,712	104	58	5,968	23,872	373K	2268K	126	8	469	213

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

Refer to DS610, *Spartan-3A DSP FPGA Family Data Sheet* for a full product description, AC and DC specifications, and package pinout descriptions. Any values shown specifically in this XA Spartan-3A DSP Automotive FPGA Family data sheet override those shown in DS610.

For information regarding reliability qualification, refer to RPT103, *Xilinx Spartan-3A Family Automotive Qualification Report* and RPT070, *Spartan-3A Commercial Qualification Report*. Contact your local Xilinx representative for more details on these reports.

Key Feature Differences from Commercial XC Devices

- AEC-Q100 device qualification and full production part approval process (PPAP) documentation support available in both extended temperature I- and Q-Grades
- Guaranteed to meet full electrical specifications over the T_J = –40°C to +125°C temperature range (Q-Grade)
- XA Spartan-3A DSP devices are available in the -4 speed grade only
- PCI-66 and PCI-X are not supported in the XA Spartan-3A DSP FPGA product line
- Platform Flash is not supported within the XA family
- XA Spartan-3A DSP devices are available in Pb-free packaging only
- MultiBoot is not supported in XA versions of this product.
- The XA Spartan-3A DSP device must be power cycled prior to reconfiguration.

Architectural Overview

The XA Spartan-3A DSP family architecture consists of five fundamental programmable functional elements:

- **XtremeDSP DSP48A Slice** provides an 18-bit x 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications.
- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kb dual-port blocks.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. The XA3SD1800A has four columns of DSP48A slices, and the XA3SD3400A has five columns of DSP48A slices. Each DSP48A has an associated block RAM. The DCMs are positioned in the center with two at the top and two at the bottom of the device and in the two outer columns of the four or five columns of block RAM and DSP48As.

The XA Spartan-3A DSP family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

I/O Capabilities

The XA Spartan-3A DSP FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

XA Spartan-3A DSP FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

XA Spartan-3A DSP FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os and Differential I/O Pairs**

Device	CSG484		FGG676	
	User	Differential	User	Differential
XA3SD1800A	**309** *(60)*	**140** *(78)*	**519** *(110)*	**227** *(131)*
XA3SD3400A	**309** *(60)*	**140** *(78)*	**469** *(60)*	**213** *(117)*

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

Production Status

Table 3 indicates the production status of each XA Spartan-3A DSP FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating a production configuration bitstream. Later versions are also supported.

Table 3: **XA Spartan-3A DSP FPGA Family Production Status (Production Speed File)**

Temperature Range		I-Grade	Q-Grade
Speed Grade		Standard (-4)	Standard (-4)
Part Number	XA3SD1800A	Production (v1.32)	Production (v1.32)
	XA3SD3400A	Production (v1.32)	–

DC Electrical Characteristics

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the published parameter values apply to all XA Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both I-Grade and Q-Grade.

Absolute Maximum Ratings

Stresses beyond those listed under Table 4, *Absolute Maximum Ratings* might cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Power Supply Specifications

Table 5: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.8	2.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 7: **Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

Quiescent Current Requirements

Table 10: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(2)	I-Grade Maximum(2)	Q-Grade Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XA3SD1800A	41	500	900	mA
		XA3SD3400A	64	725	–	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XA3SD1800A	0.4	5	5	mA
		XA3SD3400A	0.4	5	–	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XA3SD1800A	25	110	145	mA
		XA3SD3400A	39	160	–	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A DSP FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480, *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Single-Ended I/O Standards

Table 11: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[2]			V_{REF}			V_{IL}	V_{IH}[3]
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33[4]	3.0	3.3	3.6				0.8	2.0
LVCMOS25[4,5]	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3[6]	3.0	3.3	3.6				$0.3 \bullet V_{CCO}$	$0.5 \bullet V_{CCO}$
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III	1.4	1.5	1.6	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL2_II	2.3	2.5	2.7	1.15	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVCMOS25 inputs when V_{CCAUX} = 3.3V range and for PCI I/O standards.
3. For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 4.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVCMOS25 or LVCMOS33 standard depending on V_{CCAUX}. The Dual-Purpose configuration pins use the LVCMOS25 standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci. The PCI IOSTANDARD is not supported on input-only pins.

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

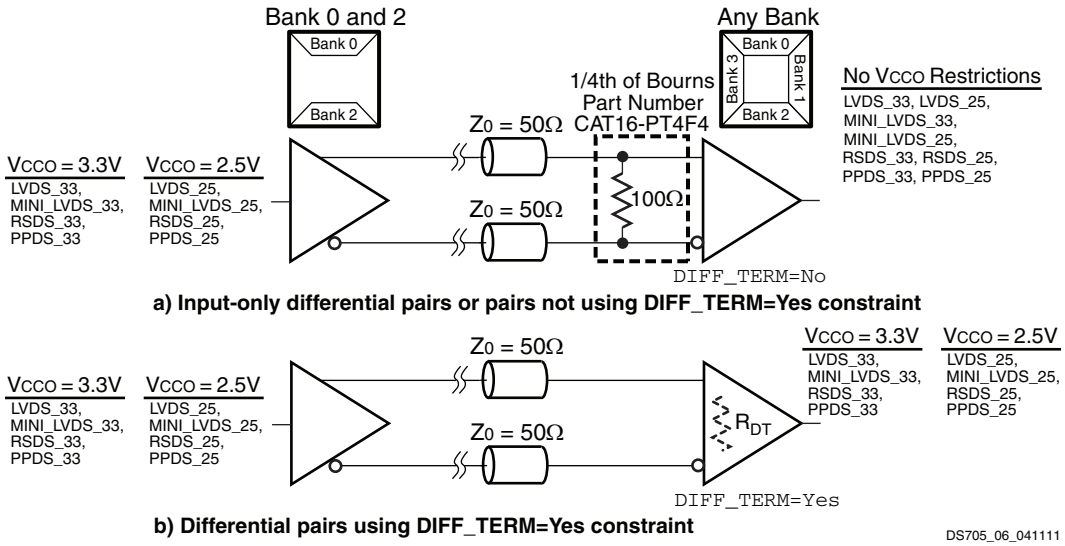


Figure 6: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

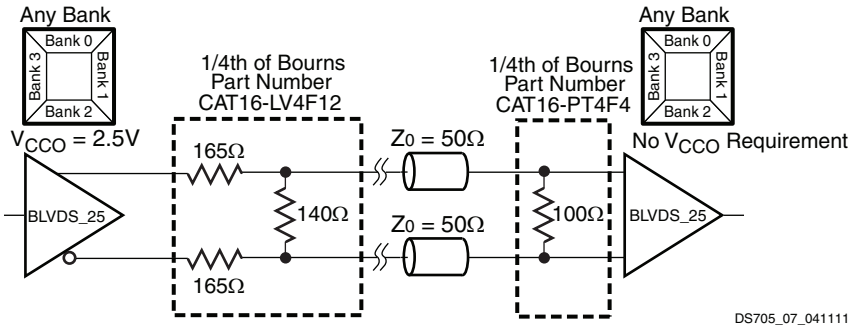


Figure 7: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

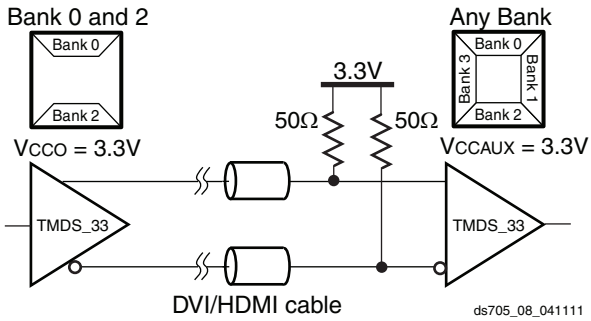


Figure 8: **External Input Resistors Required for TMDS_33 I/O Standard**

Input Setup and Hold Times

Table 20: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade: -4	Units
					Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2)	0	XA3SD1800A	1.81	ns
				XA3SD3400A	1.88	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25(2)	1	XA3SD1800A	2.24	ns
			2		2.83	ns
			3		3.64	ns
			4		4.20	ns
			5		4.16	ns
			6		5.09	ns
			7		6.02	ns
			8		6.63	ns
			1	XA3SD3400A	2.44	ns
			2		3.02	ns
			3		3.81	ns
			4		4.39	ns
			5		4.26	ns
			6		5.08	ns
			7		5.95	ns
			8		6.55	ns

Table 20: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade: -4 Min	Units
Hold Times						
T_{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3)	0	XA3SD1800A	–0.52	ns
				XA3SD3400A	–0.56	ns
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3)	1	XA3SD1800A	–1.40	ns
			2		–2.11	ns
			3		–2.48	ns
			4		–2.77	ns
			5		–2.62	ns
			6		–3.06	ns
			7		–3.42	ns
			8		–3.65	ns
			1	XA3SD3400A	–1.31	ns
			2		–1.88	ns
			3		–2.44	ns
			4		–2.89	ns
			5		–2.83	ns
			6		–3.33	ns
			7		–3.63	ns
			8		–3.96	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB	–	–	All	1.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 23.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 23. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 21: **Sample Window (Source Synchronous)**

Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB flip-flop	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. • Answer Record 30879	ps

Table 23: **Input Timing Adjustments by IOSTANDARD *(Cont'd)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	Speed Grade: -4	
HSTL_I	0.72	ns
HSTL_III	0.85	ns
HSTL_I_18	0.69	ns
HSTL_II_18	0.83	ns
HSTL_III_18	0.79	ns
SSTL18_I	0.71	ns
SSTL18_II	0.71	ns
SSTL2_I	0.71	ns
SSTL2_II	0.71	ns
SSTL3_I	0.78	ns
SSTL3_II	0.78	ns
Differential Standards		
LVDS_25	0.79	ns
LVDS_33	0.79	ns
BLVDS_25	0.79	ns
MINI_LVDS_25	0.84	ns
MINI_LVDS_33	0.84	ns
LVPECL_25	0.80	ns
LVPECL_33	0.80	ns
RSDS_25	0.83	ns
RSDS_33	0.83	ns
TMDS_33	0.80	ns
PPDS_25	0.81	ns
PPDS_33	0.81	ns
DIFF_HSTL_I_18	0.80	ns
DIFF_HSTL_II_18	0.98	ns
DIFF_HSTL_III_18	1.05	ns
DIFF_HSTL_I	0.77	ns
DIFF_HSTL_III	1.05	ns
DIFF_SSTL18_I	0.76	ns
DIFF_SSTL18_II	0.76	ns
DIFF_SSTL2_I	0.77	ns
DIFF_SSTL2_II	0.77	ns
DIFF_SSTL3_I	1.06	ns
DIFF_SSTL3_II	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Output Propagation Times

Table 24: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Max	
Clock-to-Output Times					
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	All	3.13	ns
Propagation Times					
T_{IOOP}	The time it takes for data to travel from the JOB's O input to the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	All	2.91	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		All	2.85	ns
Set/Reset Times					
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	All	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin		All	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Three-State Output Propagation Times

Table 25: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Max	
Synchronous Output Enable/Disable Times					
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.39	ns
T_{IOCKON}[2]	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	3.35	ns
Asynchronous Output Enable/Disable Times					
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	10.36	ns
Set/Reset Times					
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.86	ns
T_{IOSRON}[2]	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.82	ns

Notes:

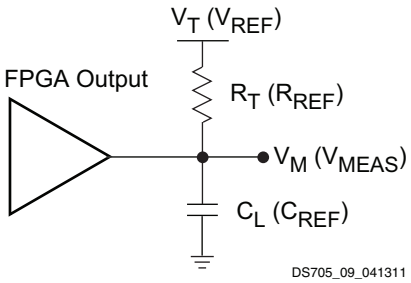
1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 27 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 9. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1 MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 9: **Output Test Setup**

Table 27: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		–	0	3.3	1M	0	1.4
LVCMOS33		–	0	3.3	1M	0	1.65
LVCMOS25		–	0	2.5	1M	0	1.25
LVCMOS18		–	0	1.8	1M	0	0.9
LVCMOS15		–	0	1.5	1M	0	0.75
LVCMOS12		–	0	1.2	1M	0	0.6
PCI33_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}

Table 29: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX}=3.3V)**

Signal Standard (IOSTANDARD)			Package Type: CSG484 and FGG676	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Single-Ended Standards				
LVTTL	Slow	2	60	60
		4	41	41
		6	29	29
		8	22	22
		12	13	13
		16	11	11
		24	9	9
	Fast	2	10	10
		4	6	6
		6	5	5
		8	3	3
		12	3	3
		16	3	3
		24	2	2
	QuietIO	2	80	80
		4	48	48
		6	36	36
		8	27	27
		12	16	16
		16	13	13
		24	12	12

Table 29: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX}=3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type: CSG484 and FGG676	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
LVCMOS25	Slow	2	76	76
		4	46	46
		6	33	33
		8	24	24
		12	18	18
		16	–	11
		24	–	7
	Fast	2	18	18
		4	14	14
		6	6	6
		8	6	6
		12	3	3
		16	–	3
		24	–	2
	QuietIO	2	76	76
		4	60	60
		6	48	48
		8	36	36
		12	36	36
		16	–	36
		24	–	8
LVCMOS18	Slow	2	64	64
		4	34	34
		6	22	22
		8	18	18
		12	–	13
		16	–	10
	Fast	2	18	18
		4	9	9
		6	7	7
		8	4	4
		12	–	4
		16	–	3
	QuietIO	2	64	64
		4	64	64
		6	48	48
		8	36	36
		12	–	36
		16	–	24

DSP48A Timing

To reference the DSP48A block diagram, see the *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide* (UG431).

Table 35: **Setup Times for the DSP48A**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade: -4	Units
					Min	
Setup Times of Data/Control Pins to the Input Register Clock						
T_{DSPDCK_AA}	A input to A register CLK	–	–	–	0.04	ns
T_{DSPDCK_DB}	D input to B register CLK	Yes(1)	–	–	1.88	ns
T_{DSPDCK_CC}	C input to C register CLK	–	–	–	0.05	ns
T_{DSPDCK_DD}	D input to D register CLK	–	–	–	0.04	ns
T_{DSPDCK_OPB}	OPMODE input to B register CLK	Yes	–	–	0.42	ns
T_{DSPDCK_OPOP}	OPMODE input to OPMODE register CLK	–	–	–	0.06	ns
Setup Times of Data Pins to the Pipeline Register Clock						
T_{DSPDCK_AM}	A input to M register CLK	–	Yes	–	3.79	ns
T_{DSPDCK_BM}	B input to M register CLK	Yes	Yes	–	4.97	ns
		No	Yes	–	3.79	ns
T_{DSPDCK_DM}	D input to M register CLK	Yes	Yes	–	5.06	ns
T_{DSPDCK_OPM}	OPMODE to M register CLK	Yes	Yes	–	5.42	ns
Setup Times of Data/Control Pins to the Output Register Clock						
T_{DSPDCK_AP}	A input to P register CLK	–	Yes	Yes	5.49	ns
T_{DSPDCK_BP}	B input to P register CLK	Yes	Yes	Yes	6.74	ns
		No	Yes	Yes	5.48	ns
T_{DSPDCK_DP}	D input to P register CLK	Yes	Yes	Yes	6.83	ns
T_{DSPDCK_CP}	C input to P register CLK	–	–	Yes	2.18	ns
T_{DSPDCK_OPP}	OPMODE input to P register CLK	Yes	Yes	Yes	7.18	ns

Notes:

1. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
2. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 40: **Switching Characteristics for the DFS *(Cont'd)***

Symbol	Description		Device	Speed Grade: -4		Units
				Min	Max	
Lock Time						
LOCK_FX[2,3]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	–	5	ms
		F_{CLKIN} > 15 MHz		–	450	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 39.
2. DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Maximum output jitter is characterized within a reasonable noise environment (40 SSOs and 25% CLB switching) on an FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of "±[1% of CLKFX period + 200]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Phase Shifter

Table 41: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Operating Frequency Ranges				
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	MHz
Input Pulse Requirements				
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	–

Table 42: **Switching Characteristics for the PS in Variable Phase Mode**

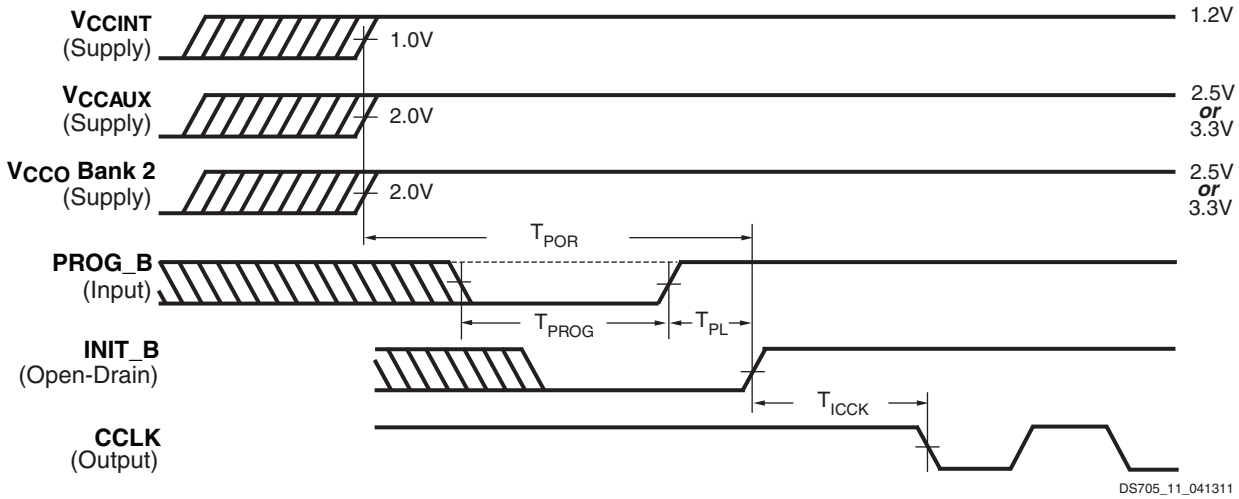
Symbol	Description		Phase Shift Amount	Units
Phase Shifting Range				
MAX_STEPS[2]	Maximum allowed number of DCM_DELAY_STEP[3] steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MIN]	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MAX]	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 41.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 38.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 – M2).

Figure 11: **Waveforms for Power-On and the Beginning of Configuration**

Table 46: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	Min	Max	Units
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	All	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	300	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the SPI and BPI modes.
4. For details on configuration, see UG332, *Spartan-3 Generation Configuration User Guide*.

Slave Serial Mode Timing

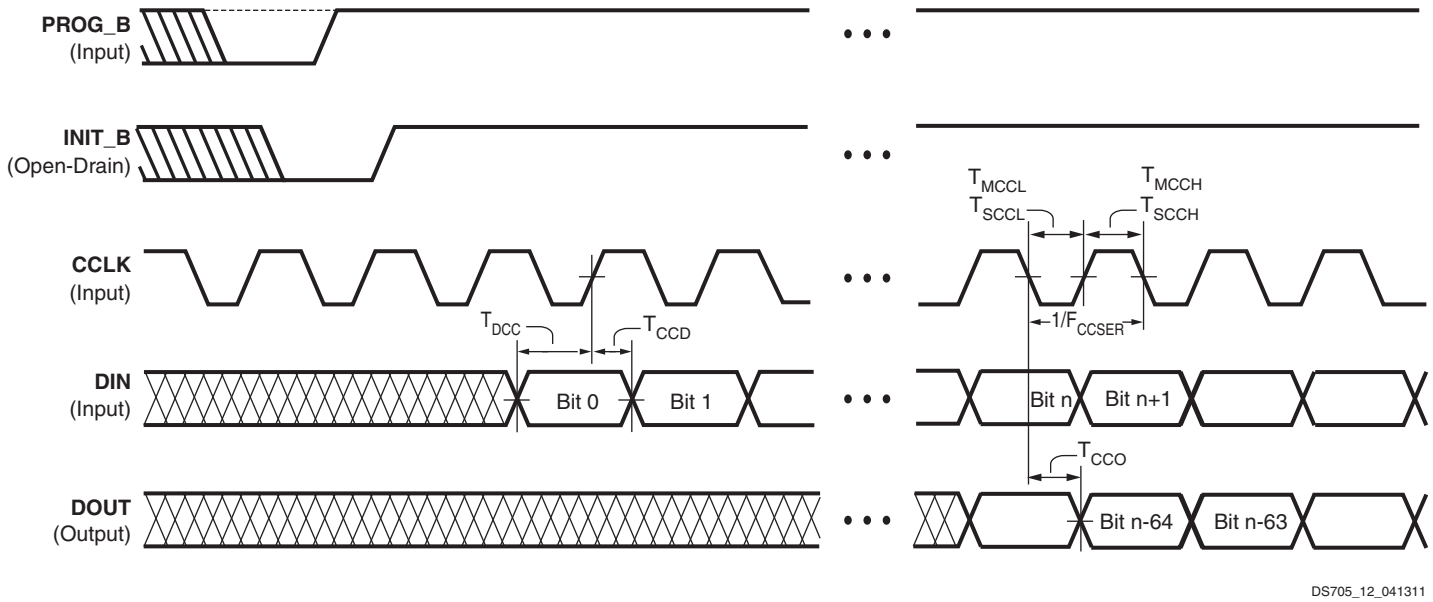


Figure 12: **Waveforms for Slave Serial Configuration**

Table 51: **Timing for the Slave Serial Configuration Modes**

Symbol	Description		Min	Max	Units
Clock-to-Output Times					
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		1.5	10	ns
Setup Times					
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		7	–	ns
Hold Times					
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		1.0	–	ns
Clock Timing					
T_{CCH}	High pulse width at the CCLK input pin		See Table 50		
T_{CCL}	Low pulse width at the CCLK input pin		See Table 50		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	100	MHz
		With bitstream compression	0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Serial Peripheral Interface Configuration Timing

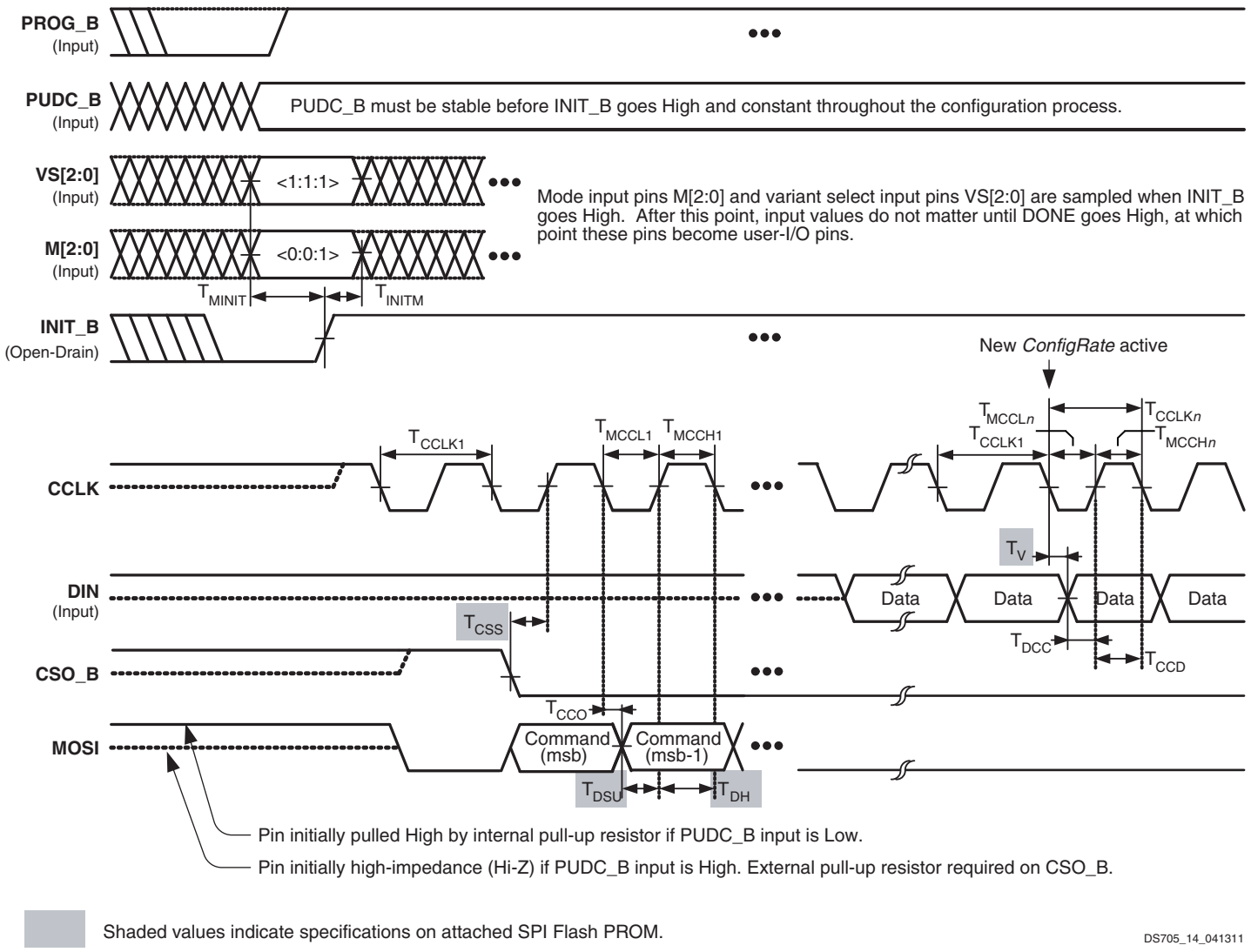


Figure 14: **Waveforms for Serial Peripheral Interface Configuration**

Table 53: **Timing for Serial Peripheral Interface Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 47		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 47		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling edge	See Table 51		
T_{DCC}	Setup time on DIN data input before CCLK rising edge	See Table 51		
T_{CCD}	Hold time on DIN data input after CCLK rising edge	0	–	ns

Revision History

The following table shows the revision history for this document.

Date	Version	Description
07/10/08	1.0	Initial Xilinx release.
01/20/09	1.1	Updated Features and Key Feature Differences from Commercial XC Devices. Removed MultiBoot description from Configuration. Updated Note 2 in Figure 11. Updated T_{ACC} requirement in Table 56.
04/18/11	2.0	This revision goes along with XCN11019: *Data Sheet Revisions for Xilinx Automotive (XA) Spartan-3A/-3A DSP FPGA Devices*. Added I_{IK} to Table 4. Updated description for V_{IN} in Table 8 including adding Note 4. Also, added Note 2 to I_L in Table 9 to note potential leakage between pins of a differential pair. Updated Notes 5 and 6 in Table 13. Table 20: Updated tags to Note 3. In Table 44, corrected symbols for $T_{DNACLKH}$ and $T_{DNACLKL}$. Corrected symbols for $T_{SUSPEND\_GTS}$ and $T_{SUSPEND\_GWE}$ in Table 45. Revised standard title to: IEEE 1149.1/1532 JTAG Test Access Port Timing. Updated Notice of Disclaimer.

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