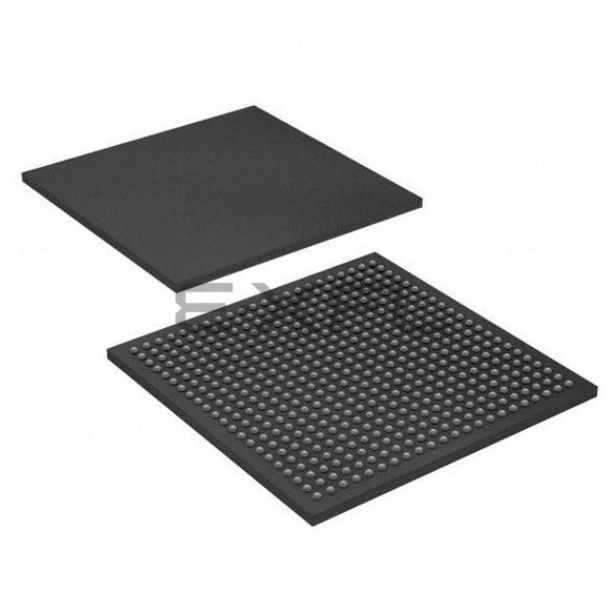

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5968
Number of Logic Elements/Cells	53712
Total RAM Bits	2322432
Number of I/O	309
Number of Gates	3400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3sd3400a-4csg484i

Package Marking

Figure 2 shows the top marking for XA Spartan-3A DSP FPGAs in BGA packages.

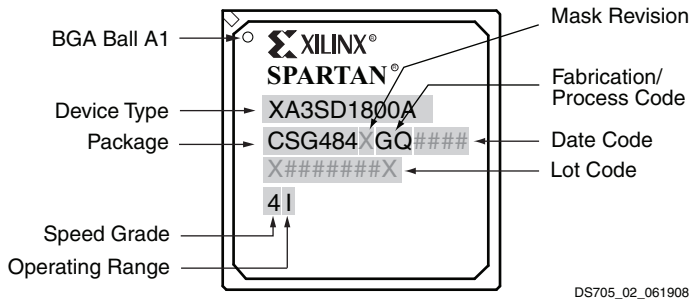


Figure 2: **XA Spartan-3A DSP FPGA Package Marking Example**

Ordering Information

XA Spartan-3A DSP FPGAs are available in Pb-free packaging only for all device/package combinations.

Pb-Free Packaging

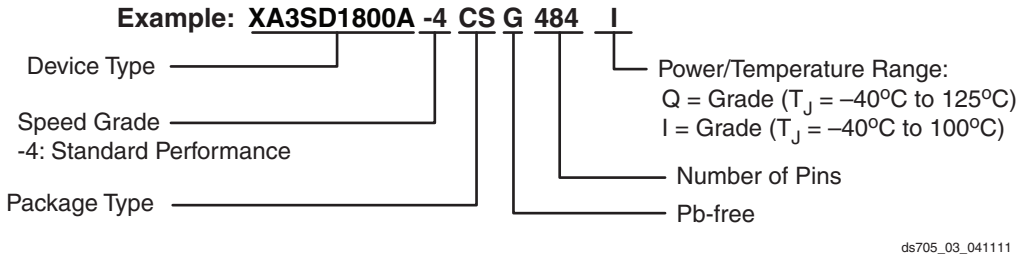


Figure 3: **Ordering Information**

Device	Speed Grade		Package Type / Number of Pins		Temperature Range (T_J)	
XA3SD1800A	-4	Standard Performance	CSG484	484-ball Chip-Scale Ball Grid Array (CSBGA)	I	I-Grade (–40°C to 100°C)
XA3SD3400A			FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)	Q	Q-Grade (–40°C to 125°C)

Notes:

1. The XA Spartan-3A DSP FPGA product line is available in -4 speed grade only.
2. The XA3SD3400A is available in I-Grade only.

Power Supply Specifications

Table 5: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.8	2.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 7: **Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

Quiescent Current Requirements

Table 10: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(2)	I-Grade Maximum(2)	Q-Grade Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XA3SD1800A	41	500	900	mA
		XA3SD3400A	64	725	–	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XA3SD1800A	0.4	5	5	mA
		XA3SD3400A	0.4	5	–	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XA3SD1800A	25	110	145	mA
		XA3SD3400A	39	160	–	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A DSP FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480, *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL[3]	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24[6]	–24		
LVCMOS33[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16[6]		
	24[4]	24	–24[6]		
LVCMOS25[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16[4]	16	–16[6]		
	24[4]	24[6]	–24[6]		
LVCMOS18[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6[6]		
	8	8	–8		
	12[4]	12	–12[6]		
	16[4]	16	–16		
LVCMOS15[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8[4]	8	–8		
	12[4]	12	–12		
LVCMOS12[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4[4]	4	–4		
	6[4]	6	–6		
PCI33_3[5]		1.5	–0.5	10% V_{CCO}	90% V_{CCO}

Table 13: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}[2]		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25[3]	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33[3]	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25[4]	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25[3]	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33[3]	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25[5]	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33[5]	Inputs Only			100	800	1000	0.3	1.2	2.8[6]
RSDS_25[3]	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33[3]	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33[3,4,7]	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25[3]	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33[3]	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18[8]	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68		0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II[8]	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II[8]	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See External Termination Requirements for Differential I/O, page 16.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX} = 3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} - (V_{ID}/2)$.
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. $(V_{CCAUX} - 300\ mV) \le V_{ICM} \le (V_{CCAUX} - 37\ mV)$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. V_{REF} inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The V_{REF} settings are the same as for the single-ended versions in Table 11. Other differential standards do not use V_{REF}.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 18: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Max	
Clock-to-Output Times					
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	XA3SD1800A	3.51	ns
			XA3SD3400A	3.82	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	XA3SD1800A	5.58	ns
			XA3SD3400A	6.13	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 23. If the latter is true, *add* the appropriate Output adjustment from Table 26.
3. DCM output jitter is included in all measurements.

Pin-to-Pin Setup and Hold Times

Table 19: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Min	
Setup Times					
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XA3SD1800A	3.11	ns
			XA3SD3400A	2.49	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 6, without DCM	XA3SD1800A	3.39	ns
			XA3SD3400A	3.08	ns
Hold Times					
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XA3SD1800A	–0.38	ns
			XA3SD3400A	–0.26	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 6, without DCM	XA3SD1800A	–0.71	ns
			XA3SD3400A	–0.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 23. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 23. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Setup and Hold Times

Table 20: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade: -4	Units
					Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2)	0	XA3SD1800A	1.81	ns
				XA3SD3400A	1.88	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25(2)	1	XA3SD1800A	2.24	ns
			2		2.83	ns
			3		3.64	ns
			4		4.20	ns
			5		4.16	ns
			6		5.09	ns
			7		6.02	ns
			8		6.63	ns
			1	XA3SD3400A	2.44	ns
			2		3.02	ns
			3		3.81	ns
			4		4.39	ns
			5		4.26	ns
			6		5.08	ns
			7		5.95	ns
			8		6.55	ns

Table 26: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below	Units
			Speed Grade: -4	
LVCMOS33	Slow	2 mA	5.58	ns
		4 mA	3.30	ns
		6 mA	3.30	ns
		8 mA	2.26	ns
		12 mA	1.29	ns
		16 mA	1.21	ns
		24 mA	2.79	ns
	Fast	2 mA	3.72	ns
		4 mA	2.04	ns
		6 mA	2.08	ns
		8 mA	0.53	ns
		12 mA	0.59	ns
		16 mA	0.59	ns
		24 mA	0.51	ns
	QuietIO	2 mA	27.67	ns
		4 mA	27.67	ns
		6 mA	27.67	ns
		8 mA	16.71	ns
		12 mA	16.29	ns
		16 mA	16.18	ns
		24 mA	12.11	ns

Table 26: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below	Units
			Speed Grade: -4	
LVCMOS15	Slow	2 mA	6.41	ns
		4 mA	3.97	ns
		6 mA	3.21	ns
		8 mA	2.53	ns
		12 mA	2.06	ns
	Fast	2 mA	5.83	ns
		4 mA	3.05	ns
		6 mA	1.95	ns
		8 mA	1.60	ns
		12 mA	1.30	ns
	QuietIO	2 mA	34.11	ns
		4 mA	25.66	ns
		6 mA	24.64	ns
		8 mA	22.06	ns
		12 mA	20.64	ns
LVCMOS12	Slow	2 mA	7.14	ns
		4 mA	4.87	ns
		6 mA	5.67	ns
	Fast	2 mA	6.77	ns
		4 mA	5.02	ns
		6 mA	4.09	ns
	QuietIO	2 mA	50.76	ns
		4 mA	43.17	ns
		6 mA	37.31	ns
PCI33_3			0.34	ns
HSTL_I			0.85	ns
HSTL_III			1.16	ns
HSTL_I_18			0.35	ns
HSTL_II_18			0.30	ns
HSTL_III_18			0.47	ns
SSTL18_I			0.40	ns
SSTL18_II			0.30	ns
SSTL2_I			0.00	ns
SSTL2_II			–0.05	ns
SSTL3_I			0.00	ns
SSTL3_II			0.17	ns

Table 26: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	Speed Grade: -4	
Differential Standards		
LVDS_25	1.49	ns
LVDS_33	0.46	ns
BLVDS_25	0.11	ns
MINI_LVDS_25	1.11	ns
MINI_LVDS_33	0.41	ns
LVPECL_25	Input Only	
LVPECL_33		
RSDS_25	1.72	ns
RSDS_33	0.64	ns
TMDS_33	0.46	ns
PPDS_25	1.28	ns
PPDS_33	0.88	ns
DIFF_HSTL_I_18	0.43	ns
DIFF_HSTL_II_18	0.41	ns
DIFF_HSTL_III_18	0.36	ns
DIFF_HSTL_I	1.01	ns
DIFF_HSTL_III	1.16	ns
DIFF_SSTL18_I	0.49	ns
DIFF_SSTL18_II	0.41	ns
DIFF_SSTL2_I	0.91	ns
DIFF_SSTL2_II	0.10	ns
DIFF_SSTL3_I	1.18	ns
DIFF_SSTL3_II	0.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Table 27: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
SSTL2_II	1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I	1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II	1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}
Differential						
LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
MINI_LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
LVPECL_33	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
RSDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
RSDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
TMDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	3.3	V_{ICM}
PPDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
PPDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
DIFF_HSTL_I	0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_HSTL_III	0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_HSTL_I_18	0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_HSTL_II_18	0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_HSTL_III_18	1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
DIFF_SSTL18_I	0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_SSTL18_II	0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_SSTL2_I	1.25	V_{REF} – 0.5	V_{REF} + 0.5	50	1.25	V_{REF}
DIFF_SSTL2_II	1.25	V_{REF} – 0.5	V_{REF} + 0.5	50	1.25	V_{REF}
DIFF_SSTL3_I	1.5	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
DIFF_SSTL3_II	1.5	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1 MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Table 29: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX}=3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type: CSG484 and FGG676	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
LVCMOS33	Slow	2	76	76
		4	46	46
		6	27	27
		8	20	20
		12	13	13
		16	10	10
		24	–	9
	Fast	2	10	10
		4	8	8
		6	5	5
		8	4	4
		12	4	4
		16	2	2
		24	–	2
	QuietIO	2	76	76
		4	46	46
		6	32	32
		8	26	26
		12	18	18
		16	14	14
		24	–	10

Configurable Logic Block Timing

Table 30: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Clock-to-Output Times				
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.68	ns
Setup Times				
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.88	–	ns
Hold Times				
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0.00	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0.00	–	ns
Clock Timing				
T_{CH}	The High pulse width of the CLB's CLK signal	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	667	MHz
Propagation Times				
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.71	ns
Set/Reset Pulse Width				
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 31: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Clock-to-Output Times				
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.72	ns
Setup Times				
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.59	–	ns
Hold Times				
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	–	ns

Table 32: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Clock-to-Output Times				
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.82	ns
Setup Times				
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.18	–	ns
Hold Times				
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	–	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 33: **Clock Distribution Switching Characteristics**

Description	Symbol	Minimum	Maximum	Units
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	–	0.23	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	–	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	0	334	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Block RAM Timing

Table 34: **Block RAM Timing**

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Clock-to-Output Times				
$T_{RCKO\_DOA\_NC}$	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.80	ns
T_{RCKO_DOA}	Clock CLK to DOUT output (with output register)	–	1.45	ns
Setup Times				
T_{RCCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.46	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.33	–	ns
T_{RCCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.60	–	ns
T_{RCCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	0.75	–	ns
T_{RCCK_REGCE}	Setup time for the CE input before the active transition at the CLK input of the block RAM	0.40	–	ns
T_{RCCK_RST}	Setup time for the RST input before the active transition at the CLK input of the block RAM	0.25	–	ns
Hold Times				
T_{RCKC_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0.10	–	ns
T_{RDCK_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0.10	–	ns
T_{RCKC_ENB}	Hold time on the EN input after the active transition at the CLK input	0.10	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0.10	–	ns
T_{RCKC_REGCE}	Hold time on the CE input after the active transition at the CLK input	0.10	–	ns
T_{RCKC_RST}	Hold time on the RST input after the active transition at the CLK input	0.10	–	ns
Clock Timing				
T_{BPWH}	High pulse width of the CLK signal	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.79	–	ns
Clock Frequency				
F_{BRAM}	Block RAM clock frequency	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Digital Frequency Synthesizer

Table 39: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade: -4		Units
				Min	Max	
Input Frequency Ranges[2]						
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333	MHz
Input Clock Jitter Tolerance[3]						
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 37.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. The DCM specifications are guaranteed when both adjacent DCMs are locked.

Table 40: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade: -4		Units
				Min	Max	
Output Frequency Ranges						
CLKOUT_FREQ_FX[2]	Frequency for the CLKFX and CLKFX180 outputs		All	5	311	MHz
Output Clock Jitter[3,4]						
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.			**Typ**	**Max**	
		CLKIN ≤ 20 MHz	All	Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip		ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle[5,6]						
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	ps
Phase Alignment[6]						
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	ps

Slave Serial Mode Timing

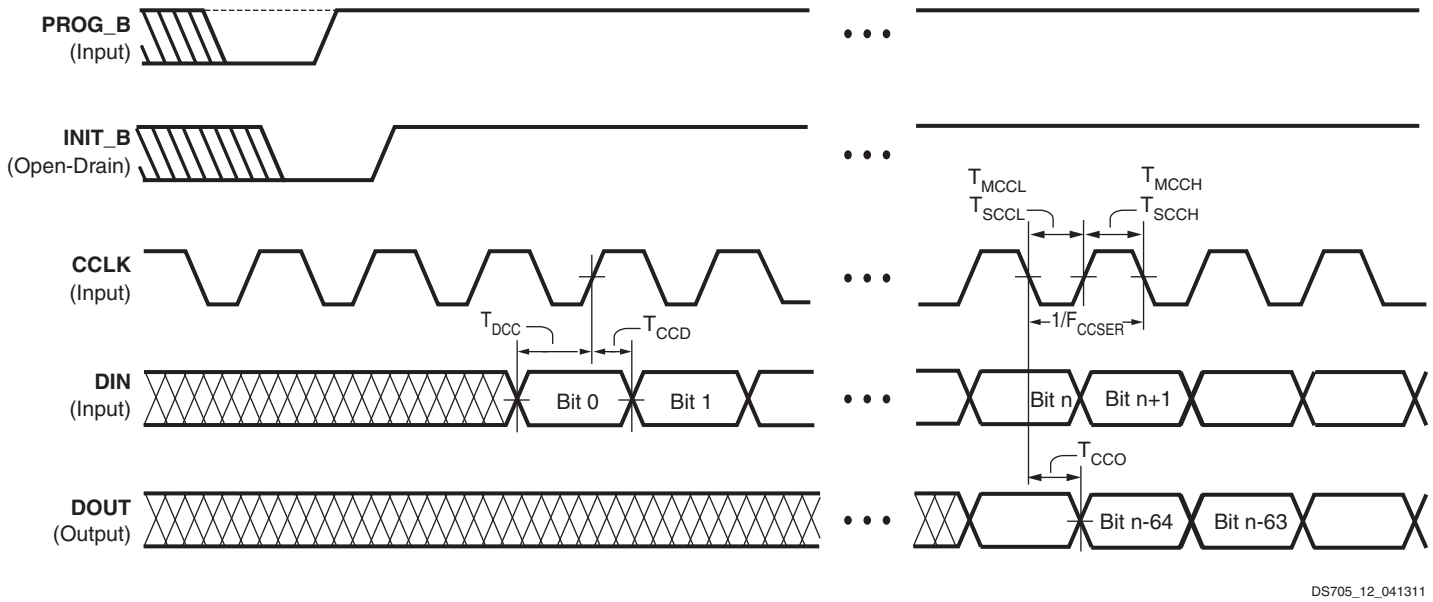


Figure 12: **Waveforms for Slave Serial Configuration**

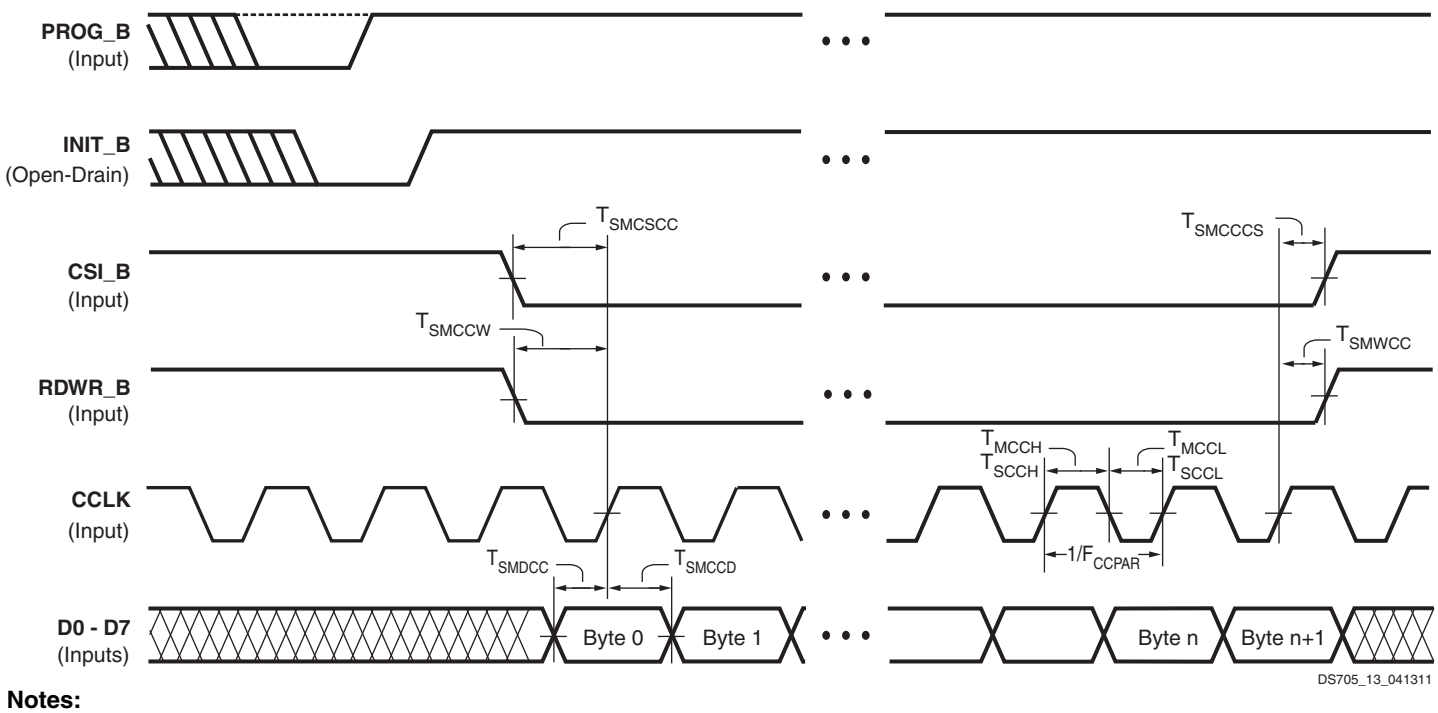
Table 51: **Timing for the Slave Serial Configuration Modes**

Symbol	Description		Min	Max	Units
Clock-to-Output Times					
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		1.5	10	ns
Setup Times					
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		7	–	ns
Hold Times					
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		1.0	–	ns
Clock Timing					
T_{CCH}	High pulse width at the CCLK input pin		See Table 50		
T_{CCL}	Low pulse width at the CCLK input pin		See Table 50		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	100	MHz
		With bitstream compression	0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0 - D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0 - D7 bus.
2. To pause configuration, pause CCLK instead of deasserting CSI_B. See the section in Chapter 7 called “Non-Continuous SelectMAP Data Loading” in UG332 for more details.

Figure 13: **Waveforms for Slave Parallel Configuration**

Table 52: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		Min	Max	Units
Setup Times					
T_{SMDCC} (2)	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		17	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Table 54: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Revision History

The following table shows the revision history for this document.

Date	Version	Description
07/10/08	1.0	Initial Xilinx release.
01/20/09	1.1	Updated Features and Key Feature Differences from Commercial XC Devices. Removed MultiBoot description from Configuration. Updated Note 2 in Figure 11. Updated T_{ACC} requirement in Table 56.
04/18/11	2.0	This revision goes along with XCN11019: *Data Sheet Revisions for Xilinx Automotive (XA) Spartan-3A/-3A DSP FPGA Devices*. Added I_{IK} to Table 4. Updated description for V_{IN} in Table 8 including adding Note 4. Also, added Note 2 to I_L in Table 9 to note potential leakage between pins of a differential pair. Updated Notes 5 and 6 in Table 13. Table 20: Updated tags to Note 3. In Table 44, corrected symbols for $T_{DNACLKH}$ and $T_{DNACLKL}$. Corrected symbols for $T_{SUSPEND\_GTS}$ and $T_{SUSPEND\_GWE}$ in Table 45. Revised standard title to: IEEE 1149.1/1532 JTAG Test Access Port Timing. Updated Notice of Disclaimer.

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