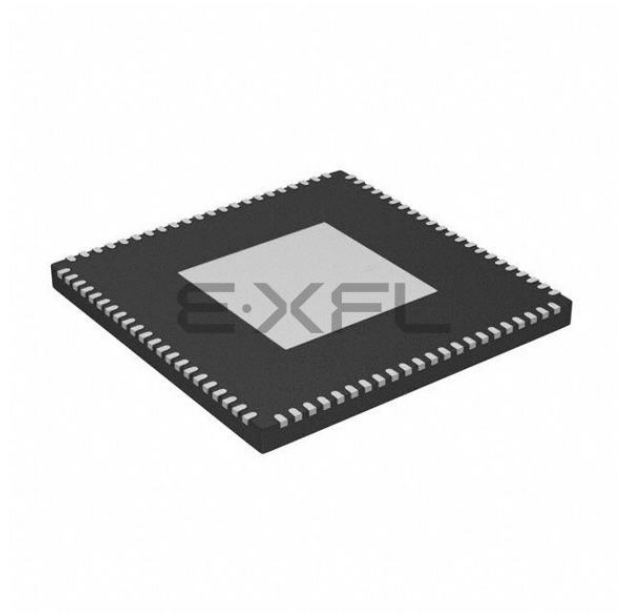

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | Fixed Point |
| Interface | CAN, EBI/EMI, I²C, IrDA, PPI, SPI, SPORT, UART/USART |
| Clock Rate | 300MHz |
| Non-Volatile Memory | FLASH (16MB) |
| On-Chip RAM | 68kB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.29V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 88-VFQFN Exposed Pad, CSP |
| Supplier Device Package | 88-LFCSP-VQ (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-bf504bcpz-3f |

# GENERAL DESCRIPTION

The ADSP-BF50x processors are members of the Blackfin® family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF50x processors are completely code compatible with other Blackfin processors. ADSP-BF50x processors offer performance up to 400 MHz and reduced static power consumption. Differences with respect to peripheral combinations are shown in Table 1.

**Table 1. Processor Comparison**

| Feature | | ADSP-BF504 | ADSP-BF504F | ADSP-BF506F |
|---|---|---|---|---|
| Up/Down/Rotary Counters | | 2 | 2 | 2 |
| Timer/Counters with PWM | | 8 | 8 | 8 |
| 3-Phase PWM Units | | 2 | 2 | 2 |
| SPORTs | | 2 | 2 | 2 |
| SPIs | | 2 | 2 | 2 |
| UARTs | | 2 | 2 | 2 |
| Parallel Peripheral Interface | | 1 | 1 | 1 |
| Removable Storage Interface | | 1 | 1 | 1 |
| CAN | | 1 | 1 | 1 |
| TWI | | 1 | 1 | 1 |
| Internal 32M Bit Flash | | – | 1 | 1 |
| ADC Control Module (ACM) | | 1 | 1 | 1 |
| Internal ADC | | – | – | 1 |
| GPIOs | | 35 | 35 | 35 |
| Memory (bytes) | L1 Instruction SRAM | 16K | 16K | 16K |
| | L1 Instruction SRAM/Cache | 16K | 16K | 16K |
| | L1 Data SRAM | 16K | 16K | 16K |
| | L1 Data SRAM/Cache | 16K | 16K | 16K |
| | L1 Scratchpad | 4K | 4K | 4K |
| | L3 Boot ROM | 4K | 4K | 4K |
| Maximum Speed Grade[1] | | 400 MHz | | |
| Maximum System Clock Speed | | 100 MHz | | |
| Package Options | | 88-Lead LFCSP | 88-Lead LFCSP | 120-Lead LQFP |

[1] For valid clock combinations, see Table 14, Table 15, Table 16, and Table 24.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

## PORTABLE LOW-POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which provides the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

## SYSTEM INTEGRATION

The ADSP-BF50x processors are highly integrated system-on-a-chip solutions for the next generation of embedded industrial, instrumentation, and power/motion control applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include a watchdog timer; two 32-bit up/down counters with rotary support; eight 32-bit timers/counters with PWM support; six pairs of 3-phase 16-bit center-based PWM units; two dual-channel, full-duplex synchronous serial ports (SPORTs); two serial peripheral interface (SPI) compatible ports; two UARTs with IrDA® support; a parallel peripheral interface (PPI); a removable storage interface (RSI) controller; an internal ADC with 12 channels, 12 bits, up to 2 MSPS, and ACM controller; a controller area network (CAN) controller; a 2-wire interface (TWI) controller; and an internal 32M bit flash.

## PROCESSOR PERIPHERALS

The ADSP-BF50x processors contain a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). These Blackfin processors contain high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The SPORT, SPI, UART, PPI, and RSI peripherals are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including boot ROM and internal 32M bit synchronous burst flash. Multiple on-chip buses running at up to 100 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF50x processors include an interface to an off-chip voltage regulator in support of the processor's dynamic power management capability.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

## UP/DOWN COUNTERS AND THUMBWHEEL INTERFACES

Two 32-bit up/down counters are provided that can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. The counters can also operate in general-purpose up/down count modes. Then, count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three pins have a programmable debouncing circuit.

Internal signals forwarded to each timer unit enable these timers to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

## 3-PHASE PWM UNITS

The two/dual 3-phase PWM generation units each feature:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single/double update modes
- Programmable dead time and switching frequency
- Twos-complement implementation which permits smooth transition to full ON and full OFF states
- Possibility to synchronize the PWM generation to either externally-generated or internally-generated synchronization pulses
- Special provisions for BDCM operation (crossover and output enable functions)
- Wide variety of special switched reluctance (SR) operating modes
- Output polarity and clock gating control
- Dedicated asynchronous PWM shutdown signal

Each PWM block integrates a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction motor (ACIM) or permanent magnet synchronous motor (PMSM) control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM) or brushless dc motor (BDCM). Software can enable a special mode for switched reluctance motors (SRM).

The six PWM output signals (per PWM unit) consist of three high-side drive signals (PWMx_AH, PWMx_BH, and PWMx_CH) and three low-side drive signals (PWMx_AL, PWMx_BL, and PWMx_CL). The polarity of the generated PWM signal can be set with software, so that either active HI or active LO PWM patterns can be produced.

The switching frequency of the generated PWM pattern is programmable using the 16-bit PWM_TM register. The PWM generator can operate in single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period, so that the resultant PWM patterns are symmetrical about the midpoint of the PWM period. In the double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

Pulses synchronous to the switching frequency can be generated internally and output on the PWMx_SYNC pin. The PWM unit can also accept externally generated synchronization pulses through PWMx_SYNC.

Each PWM unit features a dedicated asynchronous shutdown pin, $\overline{\text{PWMx\_TRIP}}$, which (when brought low) instantaneously places all six PWM outputs in the OFF state.

## SERIAL PORTS

The processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- $I^2S$ capable operation.
- Bidirectional operation—Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of $I^2S$ stereo audio.
- Buffered (8-deep) transmit and receive ports—Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking—Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from ($f_{SCLK}$/131,070) Hz to ($f_{SCLK}$/2) Hz.
- Word length—Each SPORT supports serial data words from 3 to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing—Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware—Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.

- DMA operations with single-cycle overhead—Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts—Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability—Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

## SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF50x processors have two SPI-compatible ports that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins MOSI (Master Output-Slave Input) and MISO (Master Input-Slave Output) and a clock pin, serial clock (SCK). An SPI chip select input pin ($\overline{\text{SPIx\_SS}}$) lets other SPI devices select the processor, and three SPI chip select output pins ($\overline{\text{SPIx\_SEL3–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

## UART PORTS (UARTS)

The ADSP-BF50x Blackfin processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports. Each UART port provides a simplified UART interface to other peripherals or hosts, enabling full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits; one or two stop bits; and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O). The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access). The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates. Flexible interrupt timing options are available on the transmit side.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from ($f_{SCLK}$/1,048,576) to ($f_{SCLK}$) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16^{(1-EDBO)} \times UART\_Divisor}$$

Where the 16-bit UART divisor comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant eight bits), and the EDBO is a bit in the UARTx_GCTL register.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The UARTs feature a pair of $\overline{\text{UAx\_RTS}}$ (request to send) and $\overline{\text{UAx\_CTS}}$ (clear to send) signals for hardware flow purposes. The transmitter hardware is automatically prevented from sending further data when the $\overline{\text{UAx\_CTS}}$ input is de-asserted. The receiver can automatically de-assert its $\overline{\text{UAx\_RTS}}$ output when the enhanced receive FIFO exceeds a certain high-water level. The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

## PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

In the active mode, it is possible to disable the control input to the PLL by setting the PLL_OFF bit in the PLL control register. This register can be accessed with a user-callable routine in the on-chip ROM called bfrom_SysControl(). If disabled, the PLL control input must be re-enabled before transitioning to the full-on or sleep modes.

**Table 4. Power Settings**

| Mode/State | PLL | PLL Bypassed | Core Clock (CCLK) | System Clock (SCLK) | Core Power |
|---|---|---|---|---|---|
| Full On | Enabled | No | Enabled | Enabled | On |
| Active | Enabled/ Disabled | Yes | Enabled | Enabled | On |
| Sleep | Enabled | — | Disabled | Enabled | On |
| Deep Sleep | Disabled | — | Disabled | Disabled | On |
| Hibernate | Disabled | — | Disabled | Disabled | Off |

For more information about PLL controls, see the "Dynamic Power Management" chapter in the *ADSP-BF50x Blackfin Processor Hardware Reference*.

### Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically, an external event wakes up the processor. When in the sleep mode, asserting a wakeup enabled in the SIC_IWRx registers causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

DMA accesses to L1 memory are not supported in sleep mode.

### Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset pin ($\overline{\text{RESET}}$). Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full on mode.

### Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all of the peripherals (SCLK). This setting sets the internal power supply voltage ($V_{DDINT}$) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved.

Writing 0 to the HIBERNATE bit causes EXT_WAKE to transition low, which can be used to signal an external voltage regulator to shut down.

Since $V_{DDEXT}$ can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

The processor can be woken up by asserting the $\overline{\text{RESET}}$ pin. All hibernate wakeup events initiate the hardware reset sequence. Individual sources are enabled by the VR_CTL register. The EXT_WAKE signal indicates the occurrence of a wakeup event.

As long as $V_{DDEXT}$ is applied, the VR_CTL register maintains its state during hibernation. All other internal registers and memories, however, lose their content in the hibernate state.

### Power Savings

As shown in Table 5, the processor supports three different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from other I/O, the processor can take advantage of dynamic power management without affecting the other I/O devices. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

**Table 5. Power Domains**

| Power Domain | Power Supply |
|---|---|
| All internal logic, except Memory | $V_{DDINT}$ |
| Flash Memory | $V_{DDFLASH}$ |
| All other I/O | $V_{DDEXT}$ |
| ADC digital supply[1] (Logic, I/O) | $DV_{DD}$, $V_{DRIVE}$ |
| ADC analog supply[1] | $AV_{DD}$ |

[1] On ADSP-BF506F processor only.

The dynamic power management feature of the processor allows both the processor's input voltage ($V_{DDINT}$) and clock frequency ($f_{CCLK}$) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

*Power Savings Factor*

$$= \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

$$\%\ Power\ Savings\ =\ (1 - Power\ Savings\ Factor) \times 100\%$$

**NOTE:** The SPORT must be enabled with the following settings: external clock, external frame sync, and active low frame sync.

**Table 10. The SPORTx Receive Configuration 2 Register (SPORTx_RCR2)**

| Setting | Description |
|---|---|
| RXSE = 1 | Secondary side enabled |
| SLEN = 1111 | 16-bit data-word (or may be set to 1101 for 14-bit data-word) |

To implement the power-down modes, SLEN should be set to 1001 to issue an 8-bit SCLK burst. A Blackfin driver for the ADC is available to download at www.analog.com.

## INTERNAL ADC

An ADC is integrated into the ADSP-BF506F product. All ADC signals are connected out to package pins to enable maximum interconnect flexibility in mixed signal applications.

The internal ADC is a dual, 12-bit, high speed, low power, successive approximation ADC that operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 2 MSPS. The device contains two ADCs, each preceded by a 3-channel multiplexer, and a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 30 MHz.

Figure 8 shows the functional block diagram of the internal ADC. The ADC features include:

- Dual 12-bit, 3-channel ADC
- Throughput rate: up to 2 MSPS
- Specified for $DV_{DD}$ and $AV_{DD}$ of 2.7 V to 5.25 V
- Pin-configurable analog inputs
  - 12-channel single-ended inputs

    or
  - 6-channel fully differential inputs

    or
  - 6-channel pseudo differential inputs
- Accurate on-chip voltage reference: 2.5 V
- Dual conversion with read 437.5 ns, 32 MHz ADSCLK
- High speed serial interface
  - SPI-/QSPI™-/MICROWIRE™-/DSP-compatible
- Low power shutdown mode

The conversion process and data acquisition use standard control inputs allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$; conversion is also initiated at this point. The conversion time is determined by the ADSCLK frequency. There are no pipelined delays associated with the part.

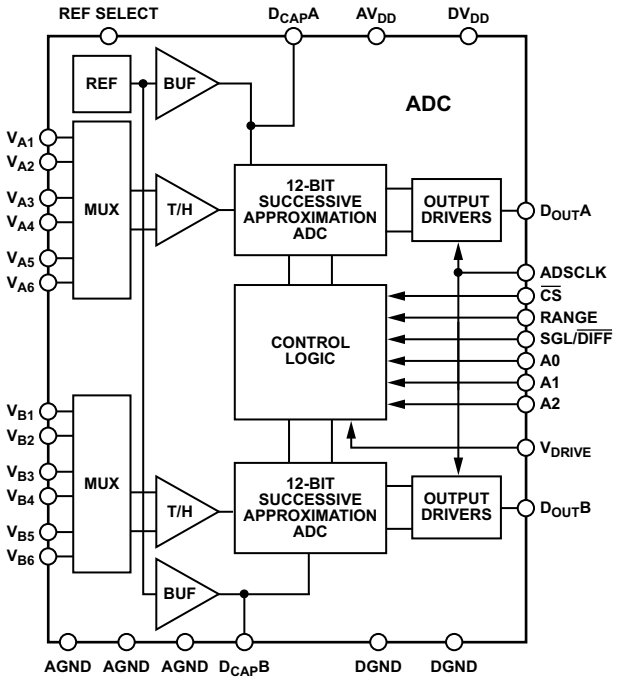



*Figure 8. ADC (Internal) Functional Block Diagram*

The internal ADC uses advanced design techniques to achieve very low power dissipation at high throughput rates. The part also offers flexible power/throughput rate management when operating in normal mode as the quiescent current consumption is so low.

The analog input range for the part can be selected to be a 0 V to $V_{REF}$ (or 2 × $V_{REF}$) range, with either straight binary or twos complement output coding. The internal ADC has an on-chip 2.5 V reference that can be overdriven when an external reference is preferred.

Additional highlights of the internal ADC include:

- Two complete ADC functions allow simultaneous sampling and conversion of two channels—Each ADC has three fully/pseudo differential pairs, or six single-ended channels, as programmed. The conversion result of both channels is simultaneously available on separate data lines, or in succession on one data line if only one serial connection is available.
- High throughput with low power consumption
- The internal ADC offers both a standard 0 V to $V_{REF}$ input range and a 2 × $V_{REF}$ input range.
- No pipeline delay—The part features two standard successive approximation ADCs with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

## ADC APPLICATION HINTS

The following sections provide application hints for using the ADC.

### *Grounding and Layout Considerations*

The analog and digital supplies to the ADC are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the ADC should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All AGND pins should be sunk in the AGND plane. Digital and analog ground planes should be joined in only one place. If the ADC is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the ground pins on the ADC.

Avoid running digital lines under the device as this couples noise onto the die. Avoid running digital lines in the area of the AGND pad as this couples noise onto the ADC die and into the AGND plane. The power supply lines to the ADC should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feed through within the board, traces on opposite sides of the board should run at right angles to each other.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

## ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF50x processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF50x Blackfin Processor Hardware Reference* (volumes 1 and 2)
- *Blackfin Processor Programming Reference*
- *ADSP-BF50x Blackfin Processor Anomaly List*

## RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http:\\www.analog.com\signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

**Table 12. ADC—Signal Descriptions (ADSP-BF506F Processor Only) (Continued)**

| Signal Name | Type | Function |
|---|---|---|
| $D_{OUT}A$, $D_{OUT}B$ | O | Serial Data Outputs. The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the ADSCLK input and 14 ADSCLKs are required to access the data. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data stream consists of two leading zeros followed by the 12 bits of conversion data. The data is provided MSB first. If $\overline{CS}$ is held low for 16 ADSCLK cycles rather than 14, then two trailing zeros will appear after the 12 bits of data. If $\overline{CS}$ is held low for a further 16 ADSCLK cycles on either $D_{OUT}A$ or $D_{OUT}B$, the data from the other ADC follows on the $D_{OUT}$ pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either $D_{OUT}A$ or $D_{OUT}B$ using only one serial port. For more information, see the ADC—Serial Interface section. |
| $V_{DRIVE}$ | P | Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the digital I/O interface operates. This pin should be decoupled to DGND. The voltage at this pin may be different than that at $AV_{DD}$ and $DV_{DD}$ but should never exceed either by more than 0.3 V. |
| $DV_{DD}$ | P | Digital Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for all digital circuitry on the internal ADC. The $DV_{DD}$ and $AV_{DD}$ voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND. |

| Parameter | | Test Conditions | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DDFLASH2}$ | Flash Memory Supply Current 2 — Reset/Powerdown | | | 15 | 50 | µA |
| $I_{DDFLASH3}$ | Flash Memory Supply Current 3 — Standby | | | 15 | 50 | µA |
| $I_{DDFLASH4}$ | Flash Memory Supply Current 4 — Automatic Standby | | | 15 | 50 | µA |
| $I_{DDFLASH5}$ | Flash Memory Supply Current 5 — Program | | | 15 | 40 | mA |
| | Flash Memory Supply Current 5 — Erase | | | 15 | 40 | mA |
| $I_{DDFLASH6}$ | Flash Memory Supply Current 6 — Dual Operations | Program/Erase in one bank, asynchronous read in another bank | | 25 | 60 | mA |
| | | Program/Erase in one bank, synchronous read in another bank | | 43 | 70 | mA |
| $I_{DDFLASH7}$ | Flash Memory Supply Current 7 — Program/Erase Suspended (Standby) | | | 15 | 50 | µA |

[1] Applies to input pins.
[2] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[3] Applies to three-statable pins.
[4] Applies to bidirectional pins SCL and SDA.
[5] Applies to all signal pins, except SCL and SDA.
[6] Guaranteed, but not tested.
[7] See the *ADSP-BF50x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[8] Applies to $V_{DDEXT}$ supply only. Clock inputs are tied high or low.
[9] Guaranteed maximum specifications.
[10] Unit for $V_{DDINT}$ is V (Volts). Unit for $f_{SCLK}$ is MHz. Example: 1.4 V, 75 MHz would be $0.16 \times 1.4 \times 75 = 16.8$ mA adder.
[11] See the *ADSP-BF50x Blackfin Processor Hardware Reference Manual* for definition of NORCLK.

## ESD SENSITIVITY

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PACKAGE INFORMATION

The information presented in Figure 9 and Table 23 provides details about the package branding for the ADSP-BF50x processors.


*Figure 9. Product Information on Package*

**Table 23. Package Brand Information[1]**

| Brand Key | Field Description |
|---|---|
| ADSP-BF50x | Product Name[2] |
| t | Temperature Range |
| pp | Package Type |
| Z | RoHS Compliant Designation |
| ccc | See Ordering Guide |
| vvvvvv.x | Assembly Lot Code |
| n.n | Silicon Revision |
| # | RoHS Compliance Designator |
| yyww | Date Code |

[1] Nonautomotive only. For branding information specific to Automotive products, contact Analog Devices Inc.
[2] See product names in the Ordering Guide on Page 81.

### *Parallel Peripheral Interface Timing*

Table 27 and Figure 14 on Page 35, Figure 20 on Page 40, and Figure 22 on Page 41 describe parallel peripheral interface operations.

**Table 27. Parallel Peripheral Interface Timing**

| Parameter | | $V_{DDEXT}$ = 1.8 V Min | $V_{DDEXT}$ = 1.8 V Max | $V_{DDEXT}$ = 2.5 V/3.3 V Min | $V_{DDEXT}$ = 2.5 V/3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{PCLKW}$ | PPI_CLK Width[1] | $t_{SCLK}$ – 1.5 | | $t_{SCLK}$ – 1.5 | | ns |
| $t_{PCLK}$ | PPI_CLK Period[1] | 2 × $t_{SCLK}$ – 1.5 | | 2 × $t_{SCLK}$ – 1.5 | | ns |
| *Timing Requirements—GP Input and Frame Capture Modes* | | | | | | |
| $t_{PSUD}$ | External Frame Sync Startup Delay[2] | 4 × $t_{PCLK}$ | | 4 × $t_{PCLK}$ | | ns |
| $t_{SFSPE}$ | External Frame Sync Setup Before PPI_CLK (Nonsampling Edge for Rx, Sampling Edge for Tx) | 6.7 | | 6.7 | | ns |
| $t_{HFSPE}$ | External Frame Sync Hold After PPI_CLK | 1.5 | | 1.5 | | ns |
| $t_{SDRPE}$ | Receive Data Setup Before PPI_CLK | 4.1 | | 3.5 | | ns |
| $t_{HDRPE}$ | Receive Data Hold After PPI_CLK | 2 | | 1.6 | | ns |
| *Switching Characteristics—GP Output and Frame Capture Modes* | | | | | | |
| $t_{DFSPE}$ | Internal Frame Sync Delay After PPI_CLK | | 8.7 | | 8.0 | ns |
| $t_{HOFSPE}$ | Internal Frame Sync Hold After PPI_CLK | 1.7 | | 1.7 | | ns |
| $t_{DDTPE}$ | Transmit Data Delay After PPI_CLK | | 8.7 | | 8.0 | ns |
| $t_{HDTPE}$ | Transmit Data Hold After PPI_CLK | 2.3 | | 1.9 | | ns |

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$

[2] The PPI port is fully enabled 4 PPI clock cycles after the PAB write to the PPI port enable bit. Only after the PPI port is fully enabled are external frame syncs and data words guaranteed to be received correctly by the PPI peripheral.

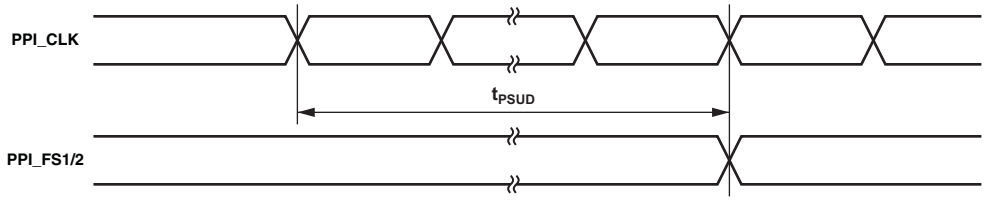



*Figure 13. PPI with External Frame Sync Timing*

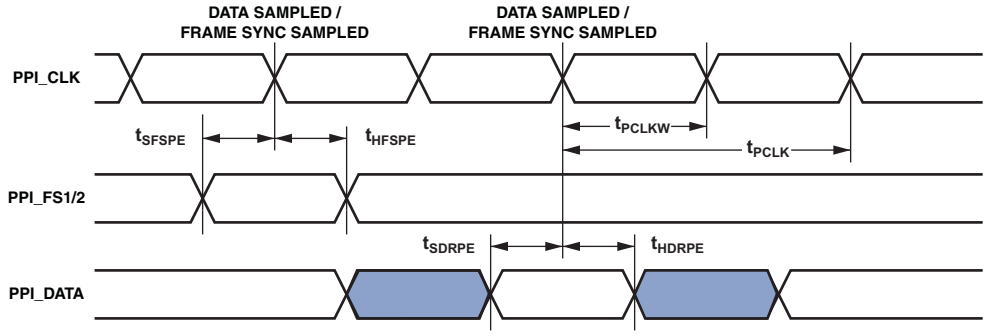



*Figure 14. PPI GP Rx Mode with External Frame Sync Timing*

**Table 33. Serial Ports — External Late Frame Sync**

| Parameter | | $V_{DDEXT}$ = 1.8 V Min | $V_{DDEXT}$ = 1.8 V Max | $V_{DDEXT}$ = 2.5 V/3.3 V Min | $V_{DDEXT}$ = 2.5 V/3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Switching Characteristics* | | | | | | |
| $t_{DDTLFSE}$ | Data Delay from Late External TFSx or External RFSx in Multi-channel Mode With MFD = 0[1, 2] | | 12.0 | | 10.0 | ns |
| $t_{DTENLFSE}$ | Data Enable from External RFSx in Multi-channel Mode With MFD = 0[1, 2] | 0.0 | | 0.0 | | ns |

[1] When in multi-channel mode, TFSx enable and TFSx valid follow $t_{DTENLFSE}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$ then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFSE}$ apply.

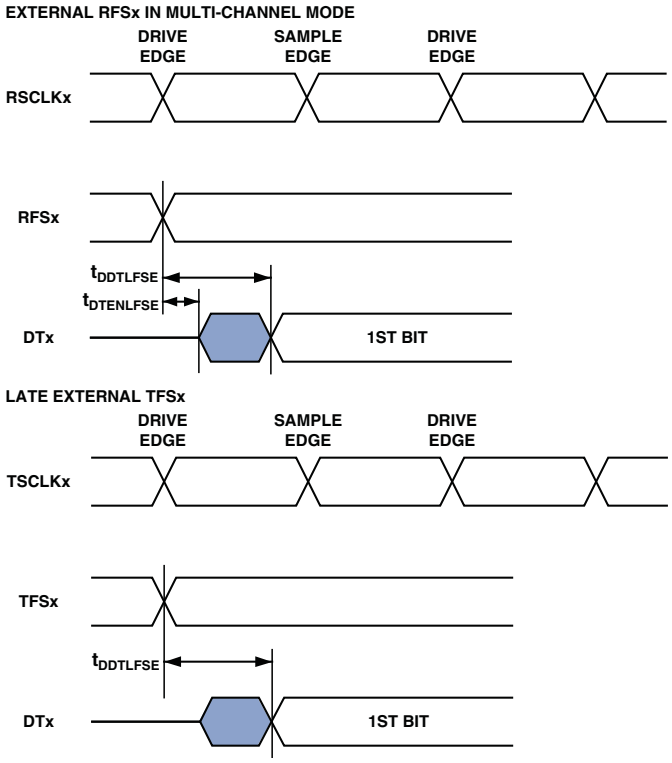



*Figure 22. Serial Ports — External Late Frame Sync*

### *Serial Peripheral Interface (SPI) Port—Master Timing*

Table 34 and Figure 23 describe SPI port master operations.

**Table 34. Serial Peripheral Interface (SPI) Port—Master Timing**

| Parameter | | $V_{DDEXT}$ = 1.8 V Min | $V_{DDEXT}$ = 1.8 V Max | $V_{DDEXT}$ = 2.5 V/3.3 V Min | $V_{DDEXT}$ = 2.5 V/3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SSPIDM}$ | Data Input Valid to SCK Edge (Data Input Setup) | 11.6 | | 9.6 | | ns |
| $t_{HSPIDM}$ | SCK Sampling Edge to Data Input Invalid | –1.5 | | –1.5 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{SDSCIM}$ | $\overline{SPISELx}$ low to First SCK Edge | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICHM}$ | Serial Clock High Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLM}$ | Serial Clock Low Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLK}$ | Serial Clock Period | $4 \times t_{SCLK} - 1.5$ | | $4 \times t_{SCLK} - 1.5$ | | ns |
| $t_{HDSM}$ | Last SCK Edge to $\overline{SPISELx}$ High | $2 \times t_{SCLK} - 2.0$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPITDM}$ | Sequential Transfer Delay | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{DDSPIDM}$ | SCK Edge to Data Out Valid (Data Out Delay) | 0 | 6 | 0 | 6 | ns |
| $t_{HDSPIDM}$ | SCK Edge to Data Out Invalid (Data Out Hold) | –1.0 | | –1.0 | | ns |

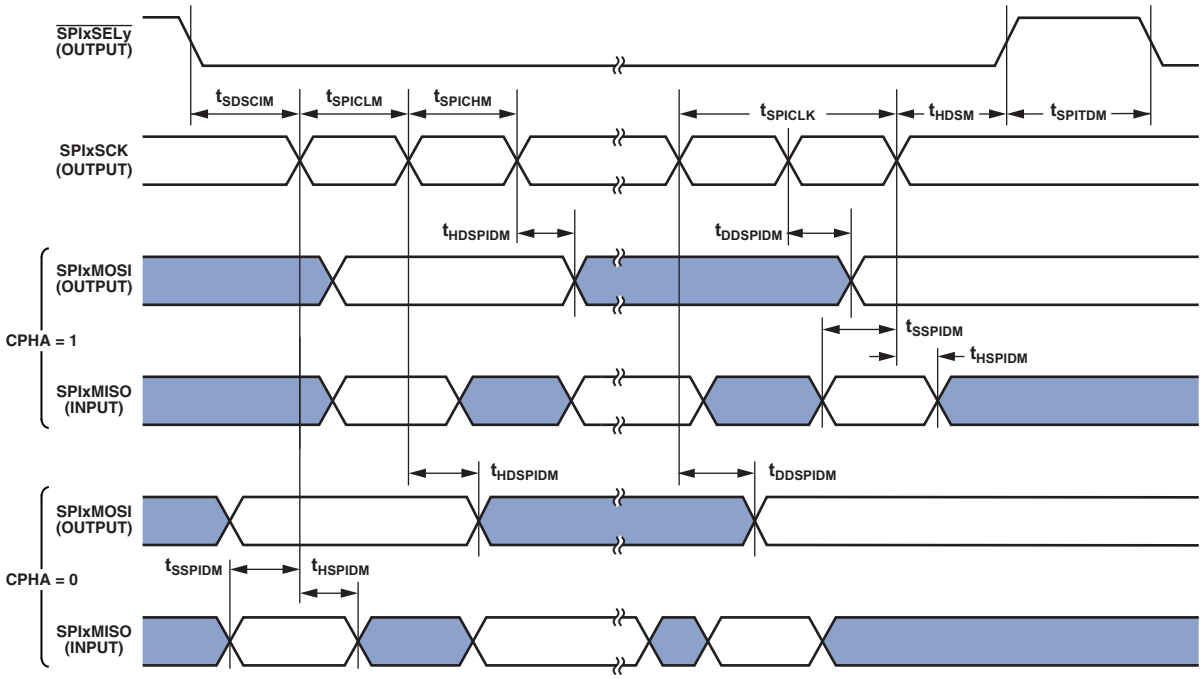



*Figure 23. Serial Peripheral Interface (SPI) Port—Master Timing*

### *Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing*

The UART ports receive and transmit operations are described in the *ADSP-BF50x Hardware Reference Manual*.

### *General-Purpose Port Timing*

Table 36 and Figure 25 describe general-purpose port operations.

**Table 36. General-Purpose Port Timing**

| Parameter | | $V_{DDEXT}$ = 1.8 V Min | $V_{DDEXT}$ = 1.8 V Max | $V_{DDEXT}$ = 2.5 V/3.3 V Min | $V_{DDEXT}$ = 2.5 V/3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirement* | | | | | | |
| $t_{WFI}$ | General-Purpose Port Pin Input Pulse Width | $t_{SCLK}$ + 1 | | $t_{SCLK}$ + 1 | | ns |
| *Switching Characteristic* | | | | | | |
| $t_{GPOD}$ | General-Purpose Port Pin Output Delay from CLKOUT High | 0 | 11.0 | 0 | 8.9 | ns |

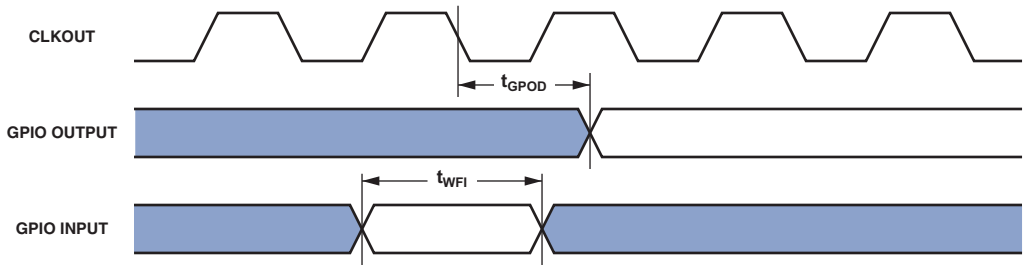



*Figure 25. General-Purpose Port Timing*

### ADC Controller Module (ACM) Timing

Table 41 and Figure 30 describe ACM operations.

Note that the ACM clock (ACLK) frequency in MHz is set by the following equation (in which ACMCKDIV ranges from 0 to 255).

$$t_{ACLK} = \frac{1}{f_{ACLK}}$$

$$f_{ACLK} = \frac{f_{SCLK}}{(2 \times ACMCKDIV) + 2}$$

**Table 41. ACM Timing**

| Parameter | | $V_{DDEXT}$ = 1.8 V Min | $V_{DDEXT}$ = 1.8 V Max | $V_{DDEXT}$ = 2.5 V/3.3 V Min | $V_{DDEXT}$ = 2.5 V/3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SDR}$ | SPORT DRxPRI/DRxSEC Setup Before ACLK | 8.0 | | 7.0 | | ns |
| $t_{HDR}$ | SPORT DRxPRI/DRxSEC Hold After ACLK | 0 | | 0 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{DO}$ | ACM Controls (ACM_A[2:0], ACM_RANGE, ACM_SGLDIFF) Delay After Falling Edge of CLKOUT | | 8.4 | | 8.4 | ns |
| $t_{DACLK}$ | ACLK Delay After Falling Edge of CLKOUT | | 4.5 | | 4.5 | ns |
| $t_{DCS}$ | $\overline{CS}$ Active Edge Delay After Falling Edge of CLKOUT | | 5.6 | | 5.3 | ns |
| $t_{DCSACLK}$ | The Delay Between the Active Edge of $\overline{CS}$ and the First Edge of ACLK | $t_{ACLK}$ – 5 | | $t_{ACLK}$ – 5 | | ns |

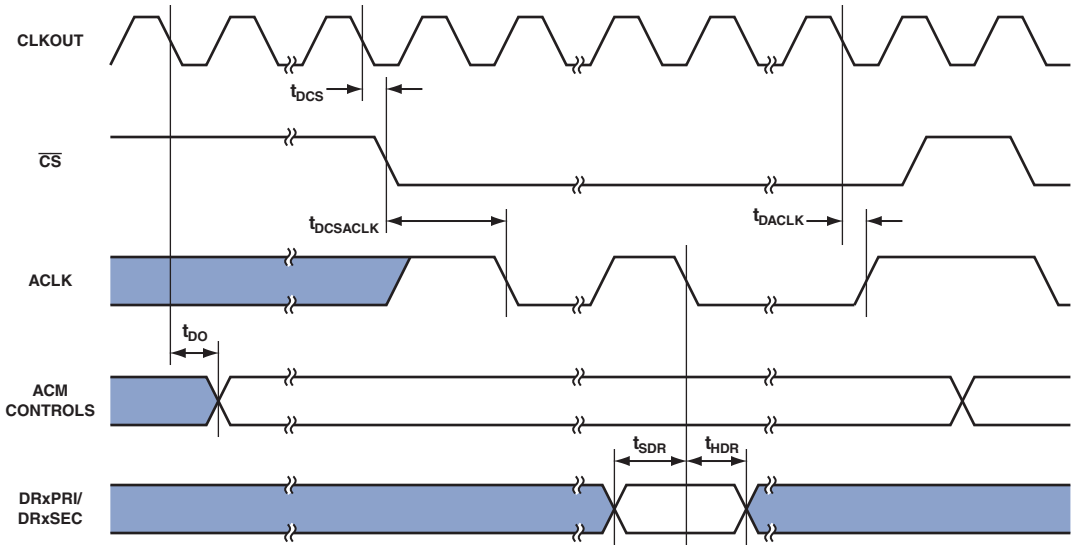



*Figure 30. ACM Timing*

## PROCESSOR—OUTPUT DRIVE CURRENTS

Figure 32 through Figure 40 show typical current-voltage characteristics for the output drivers of the ADSP-BF50xF processors.

The curves represent the current drive capability of the output drivers. See Table 11 on Page 22 for information about which driver type corresponds to a particular pin.

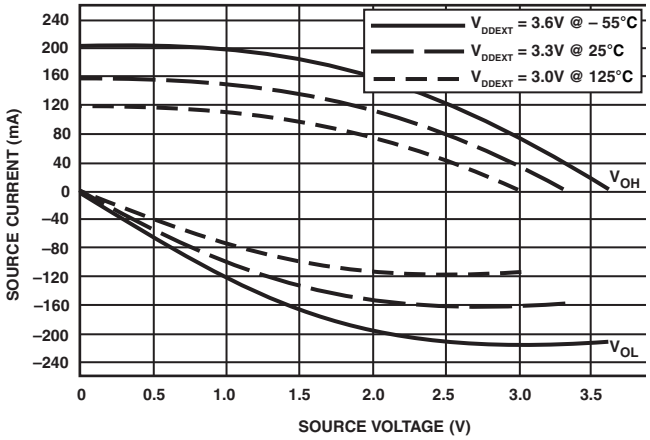



*Figure 32. Driver Type B Current (3.3 V $V_{DDEXT}$)*

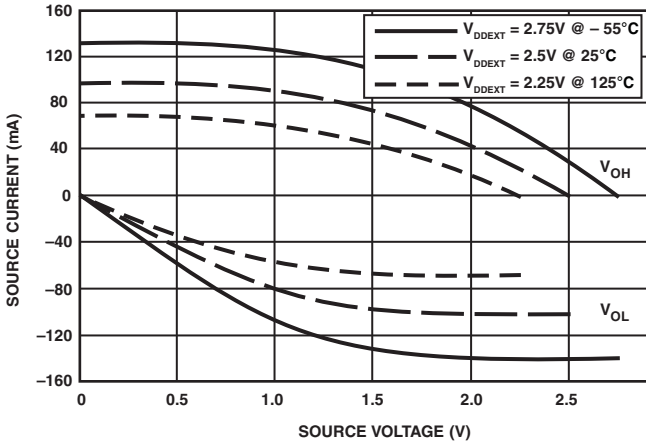



*Figure 33. Driver Type B Current (2.5 V $V_{DDEXT}$)*

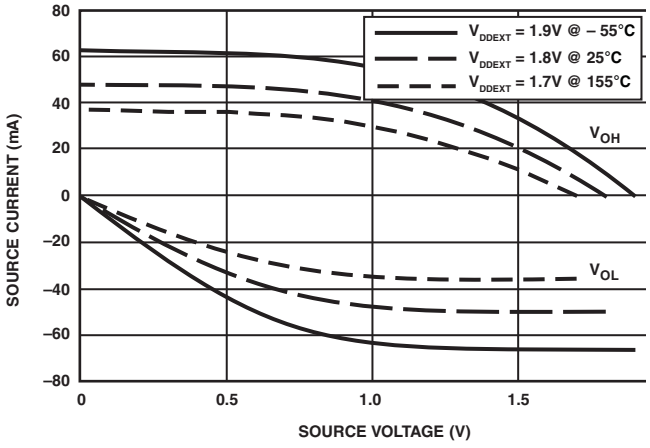



*Figure 34. Driver Type B Current (1.8 V $V_{DDEXT}$)*

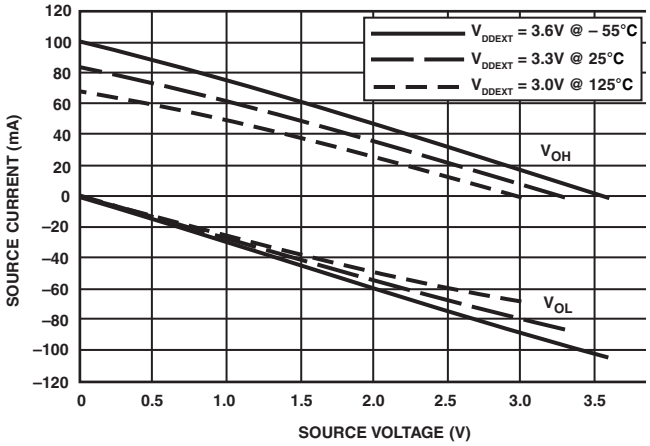



*Figure 35. Driver Type C Current (3.3 V $V_{DDEXT}$)*

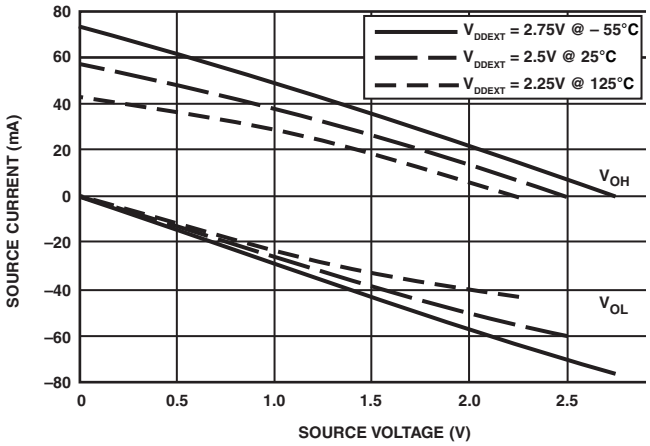



*Figure 36. Drive Type C Current (2.5 V $V_{DDEXT}$)*

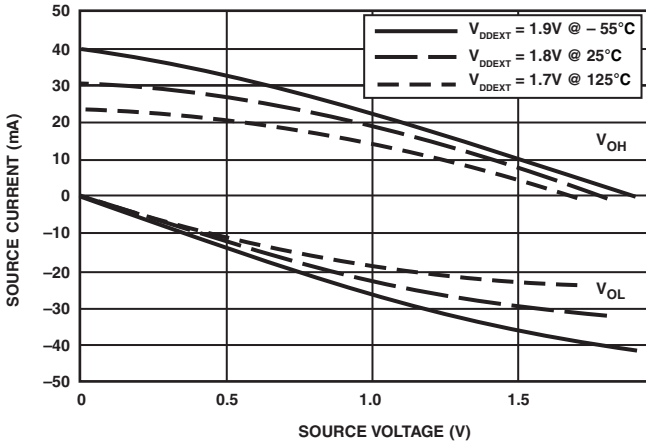



*Figure 37. Driver Type C Current (1.8 V $V_{DDEXT}$)*

supply using the 0 to $V_{REF}$ range or 2 × $V_{REF}$ range, respectively. The common mode must be in this range to guarantee the functionality of the ADC.

When a conversion takes place, the common mode is rejected, resulting in a virtually noise free signal of amplitude –$V_{REF}$ to +$V_{REF}$ corresponding to the digital codes of 0 to 4096. If the 2 × $V_{REF}$ range is used, then the input signal amplitude extends from – 2 $V_{REF}$ to +2 $V_{REF}$ after conversion.

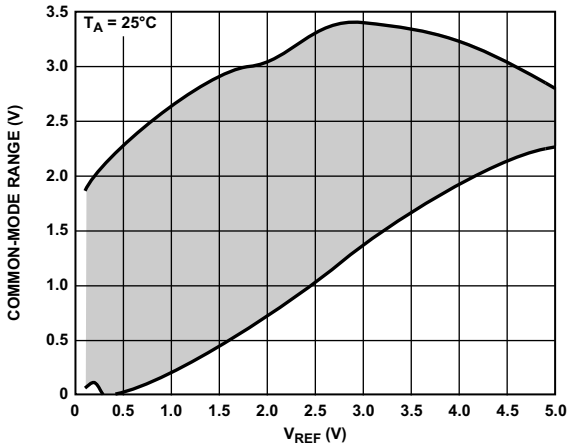



*Figure 70. Input Common-Mode Range vs. $V_{REF}$ (0 to $V_{REF}$ Range, $V_{DD}$ = 5 V)*

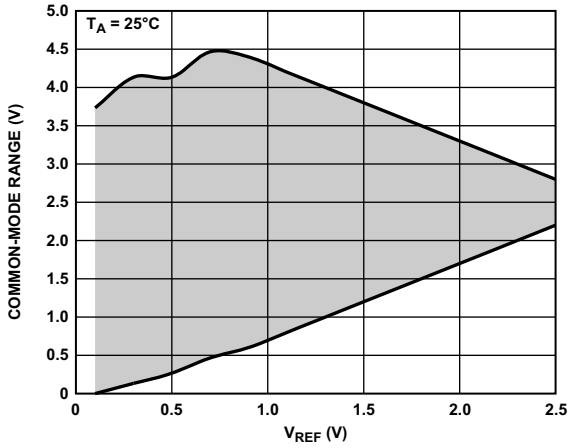



*Figure 71. Input Common-Mode Range vs. $V_{REF}$ (2 × $V_{REF}$ Range, $V_{DD}$ = 5 V)*

### Driving Differential Inputs

Differential operation requires that $V_{IN+}$ and $V_{IN–}$ be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally. The common-mode range is determined by $V_{REF}$, the power supply, and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion.

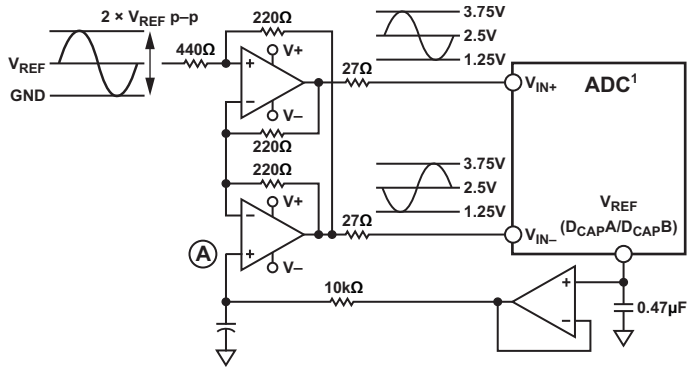
### Using an Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the ADC. The circuit configurations illustrated in Figure 72 (Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal Into a Differential Signal) and Figure 73 (Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal) show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, it is connected in some way to the reference, but any value in the common-mode range can be input here to set up the common mode. The AD8022 is a suitable dual op amp that can be used in this configuration to provide differential drive to the ADC.

Take care when choosing the op amp; the selection depends on the required power supply and system performance objectives. The driver circuits in Figure 72 (Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal Into a Differential Signal) and Figure 73 (Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal) are optimized for dc coupling applications requiring best distortion performance.

The circuit configuration shown in Figure 72 (Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal Into a Differential Signal) converts a unipolar, single-ended signal into a differential signal.




[1]ADDITIONAL PINS OMITTED FOR CLARITY.

*Figure 72. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal Into a Differential Signal*

The differential op amp driver circuit shown in Figure 73 (Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal) is configured to convert and level shift a single-ended, ground-referenced (bipolar) signal to a differential signal centered at the $V_{REF}$ level of the ADC.

### Pseudo Differential Mode

The ADC can have a total of six pseudo differential pairs. In this mode, $V_{IN+}$ is connected to the signal source that must have an amplitude of $V_{REF}$ (or 2 × $V_{REF}$, depending on the range chosen)

down for a relatively long duration between these bursts of several conversions. When the ADC is in partial power-down, all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter partial power-down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of ADSCLK and before the 10th falling edge of ADSCLK, as shown in Figure 81 (Entering Partial Power-Down Mode). Once $\overline{CS}$ is brought high in this window of ADSCLKs, the part enters partial power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is brought high before the second ADSCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the $\overline{CS}$ line.

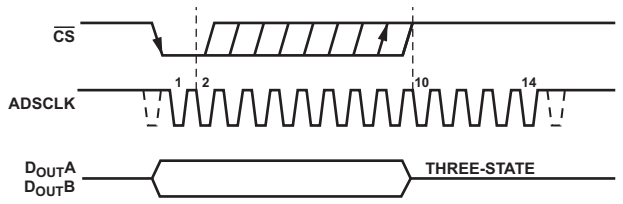



*Figure 81. Entering Partial Power-Down Mode*

To exit this mode of operation and power up the ADC again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th ADSCLK. The device is fully powered up after approximately 1 µs has elapsed, and valid data results from the next conversion, as shown in Figure 82 (Exiting Partial Power-Down Mode). If $\overline{CS}$ is brought high before the second falling edge of ADSCLK, the ADC again goes into partial power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line. Although the device may begin to power up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$. If the ADC is already in partial power-down mode and $\overline{CS}$ is brought high between the second and 10th falling edges of ADSCLK, the device enters full power-down mode.

### *Full Power-Down Mode*

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required, as power-up from a full power-down takes substantially longer than that from partial power-down. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus power-down. When the ADC is in full power-down, all analog circuitry is powered down. Full power-down is entered in a similar way as partial power-down, except the timing sequence shown in Figure 81 (Entering Partial Power-Down Mode) must be executed twice. The conversion process must be interrupted in a similar fashion by bringing $\overline{CS}$ high anywhere after the second falling edge of ADSCLK and before the 10th falling edge of ADSCLK. The device enters partial power-down at this point. To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure 83 (Entering Full Power-Down Mode). Once $\overline{CS}$ is brought high in this window of ADSCLKs, the part completely powers down.

Note that it is not necessary to complete the 14 ADSCLKs once $\overline{CS}$ is brought high to enter a power-down mode.

To exit full power-down and power up the ADC, a dummy conversion is performed, as when powering up from partial power-down. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up, as long as $\overline{CS}$ is held low until after the falling edge of the 10th ADSCLK. The required power-up time must elapse before a conversion can be initiated, as shown in Figure 84 (Exiting Full Power-Down Mode). See the Power-Up Times section for the power-up times associated with the ADC.

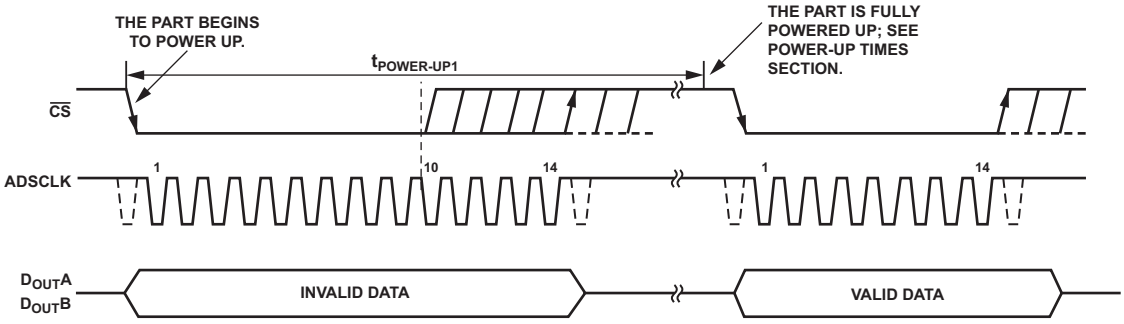



*Figure 82. Exiting Partial Power-Down Mode*

# 120-LEAD LQFP LEAD ASSIGNMENT

Table 54 lists the LQFP leads by signal mnemonic. Table 55 on Page 74 lists the LQFP leads by lead number.

**Table 54. 120-Lead LQFP Lead Assignment (Alphabetical by Signal)**

| Signal | Lead No. | Signal | Lead No. | Signal | Lead No. | Signal | Lead No. |
|---|---|---|---|---|---|---|---|
| A0 | 100 | NC | 72 | PG11 | 46 | $V_{B5}$ | 88 |
| A1 | 98 | $\overline{NMI}$ | 11 | PG12 | 47 | $V_{B6}$ | 87 |
| A2 | 97 | PF0 | 118 | PG13 | 48 | $V_{DDEXT}$ | 1 |
| AGND | 73 | PF1 | 119 | PG14 | 49 | $V_{DDEXT}$ | 6 |
| AGND | 78 | PF2 | 2 | PG15 | 50 | $V_{DDEXT}$ | 15 |
| AGND | 79 | PF3 | 4 | PH0 | 113 | $V_{DDEXT}$ | 20 |
| AGND | 82 | PF4 | 3 | PH1 | 115 | $V_{DDEXT}$ | 23 |
| AGND | 93 | PF5 | 5 | PH2 | 114 | $V_{DDEXT}$ | 26 |
| AGND | 99 | PF6 | 7 | RANGE | 95 | $V_{DDEXT}$ | 30 |
| $AV_{DD}$ | 76 | PF7 | 8 | REF_SELECT | 75 | $V_{DDEXT}$ | 41 |
| BMODE0 | 58 | PF8 | 9 | $\overline{RESET}$ | 12 | $V_{DDEXT}$ | 51 |
| BMODE1 | 57 | PF9 | 10 | SCL | 55 | $V_{DDEXT}$ | 59 |
| BMODE2 | 56 | PF10 | 14 | ADSCLK | 102 | $V_{DDEXT}$ | 62 |
| CLKIN | 110 | PF11 | 16 | SDA | 54 | $V_{DDEXT}$ | 64 |
| $\overline{CS}$ | 101 | PF12 | 18 | SGL/$\overline{DIFF}$ | 96 | $V_{DDEXT}$ | 66 |
| $D_{CAP}A$ | 77 | PF13 | 19 | TCK | 34 | $V_{DDEXT}$ | 67 |
| $D_{CAP}B$ | 94 | PF14 | 21 | TDI | 33 | $V_{DDEXT}$ | 112 |
| DGND | 74 | PF15 | 22 | TDO | 36 | $V_{DDEXT}$ | 116 |
| DGND | 104 | $\overline{PG}$ | 71 | TMS | 35 | $V_{DDFLASH}$ | 25 |
| $D_{OUT}A$ | 105 | PG0 | 27 | $\overline{TRST}$ | 37 | $V_{DDFLASH}$ | 63 |
| $D_{OUT}B$ | 103 | PG1 | 28 | $V_{A1}$ | 80 | $V_{DDFLASH}$ | 69 |
| $DV_{DD}$ | 107 | PG2 | 29 | $V_{A2}$ | 81 | $V_{DDINT}$ | 24 |
| $\overline{EMU}$ | 68 | PG3 | 31 | $V_{A3}$ | 83 | $V_{DDINT}$ | 42 |
| EXT_WAKE | 70 | PG4 | 32 | $V_{A4}$ | 84 | $V_{DDINT}$ | 52 |
| EXTCLK | 120 | PG5 | 38 | $V_{A5}$ | 85 | $V_{DDINT}$ | 53 |
| GND | 13 | PG6 | 39 | $V_{A6}$ | 86 | $V_{DDINT}$ | 61 |
| GND | 17 | PG7 | 40 | $V_{B1}$ | 92 | $V_{DDINT}$ | 65 |
| GND | 108 | PG8 | 43 | $V_{B2}$ | 91 | $V_{DDINT}$ | 117 |
| GND | 109 | PG9 | 44 | $V_{B3}$ | 90 | $V_{DRIVE}$ | 106 |
| NC | 60 | PG10 | 45 | $V_{B4}$ | 89 | XTAL | 111 |
| | | | | | | GND | 121* |
| | | | | | | AGND | 122** |

* Pin no. 121 is the GND supply (see Figure 89 and Figure 90) for the processor (4.6mm × 6.17mm); this pad **must** connect to GND.
** Pin no. 122 is the AGND supply (see Figure 89 and Figure 90) for the ADC (2.81mm × 2.81mm); this pad **must** connect to AGND.

# 88-LEAD LFCSP LEAD ASSIGNMENT

Table 56 lists the LFCSP leads by signal mnemonic. Table 57 on Page 77 lists the LFCSP by lead number.

**Table 56. 88-Lead LFCSP Lead Assignment (Alphabetical by Signal)**

| Signal | Lead No. | Signal | Lead No. | Signal | Lead No. | Signal | Lead No. |
|---|---|---|---|---|---|---|---|
| BMODE0 | 51 | PF4 | 82 | PG9 | 34 | $V_{DDEXT}$ | 20 |
| BMODE1 | 50 | PF5 | 83 | PG10 | 35 | $V_{DDEXT}$ | 31 |
| BMODE2 | 49 | PF6 | 85 | PG11 | 36 | $V_{DDEXT}$ | 41 |
| CLKIN | 68 | PF7 | 86 | PG12 | 37 | $V_{DDEXT}$ | 52 |
| $\overline{EMU}$ | 60 | PF8 | 87 | PG13 | 38 | $V_{DDEXT}$ | 54 |
| EXT_WAKE | 62 | PF9 | 88 | PG14 | 39 | $V_{DDEXT}$ | 56 |
| EXTCLK | 78 | PF10 | 4 | PG15 | 40 | $V_{DDEXT}$ | 58 |
| GND | 3 | PF11 | 6 | PH0 | 71 | $V_{DDEXT}$ | 59 |
| GND | 7 | PF12 | 8 | PH1 | 72 | $V_{DDEXT}$ | 70 |
| GND | 67 | PF13 | 9 | PH2 | 73 | $V_{DDEXT}$ | 74 |
| NC | 45 | PF14 | 11 | $\overline{RESET}$ | 2 | $V_{DDEXT}$ | 79 |
| NC | 46 | PF15 | 12 | SCL | 44 | $V_{DDEXT}$ | 84 |
| NC | 47 | $\overline{PG}$ | 63 | SDA | 43 | $V_{DDFLASH}$ | 15 |
| NC | 48 | PG0 | 17 | TCK | 24 | $V_{DDFLASH}$ | 55 |
| NC | 64 | PG1 | 18 | TDI | 23 | $V_{DDFLASH}$ | 61 |
| NC | 65 | PG2 | 19 | TDO | 27 | $V_{DDINT}$ | 14 |
| NC | 66 | PG3 | 21 | TMS | 25 | $V_{DDINT}$ | 32 |
| $\overline{NMI}$ | 1 | PG4 | 22 | $\overline{TRST}$ | 26 | $V_{DDINT}$ | 42 |
| PF0 | 76 | PG5 | 28 | $V_{DDEXT}$ | 5 | $V_{DDINT}$ | 53 |
| PF1 | 77 | PG6 | 29 | $V_{DDEXT}$ | 10 | $V_{DDINT}$ | 57 |
| PF2 | 80 | PG7 | 30 | $V_{DDEXT}$ | 13 | $V_{DDINT}$ | 75 |
| PF3 | 81 | PG8 | 33 | $V_{DDEXT}$ | 16 | XTAL | 69 |
| | | | | | | GND | 89* |

* Pin no. 89 is the GND supply (see Figure 92) for the processor; this pad **must** connect to GND.