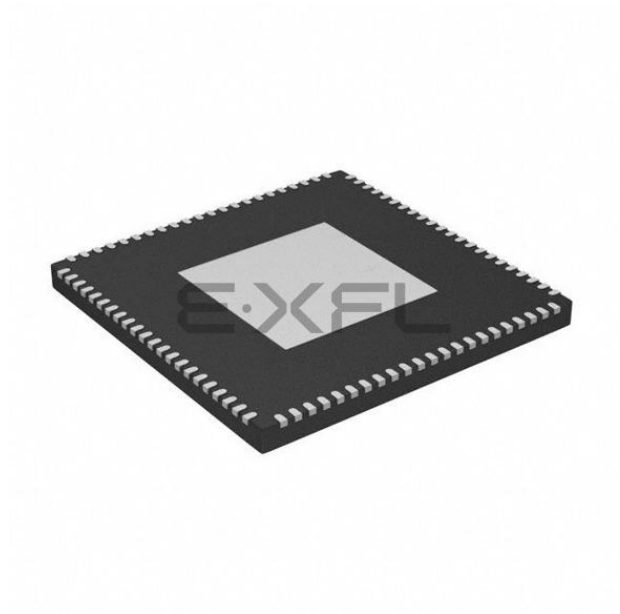

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, EBI/EMI, I²C, IrDA, PPI, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	68kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.29V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP-VQ (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf504bcpz-4

GENERAL DESCRIPTION

The ADSP-BF50x processors are members of the Blackfin® family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF50x processors are completely code compatible with other Blackfin processors. ADSP-BF50x processors offer performance up to 400 MHz and reduced static power consumption. Differences with respect to peripheral combinations are shown in Table 1.

Table 1. Processor Comparison

Feature		ADSP-BF504	ADSP-BF504F	ADSP-BF506F
Up/Down/Rotary Counters		2	2	2
Timer/Counters with PWM		8	8	8
3-Phase PWM Units		2	2	2
SPORTs		2	2	2
SPIs		2	2	2
UARTs		2	2	2
Parallel Peripheral Interface		1	1	1
Removable Storage Interface		1	1	1
CAN		1	1	1
TWI		1	1	1
Internal 32M Bit Flash		–	1	1
ADC Control Module (ACM)		1	1	1
Internal ADC		–	–	1
GPIOs		35	35	35
Memory (bytes)	L1 Instruction SRAM	16K	16K	16K
	L1 Instruction SRAM/Cache	16K	16K	16K
	L1 Data SRAM	16K	16K	16K
	L1 Data SRAM/Cache	16K	16K	16K
	L1 Scratchpad	4K	4K	4K
	L3 Boot ROM	4K	4K	4K
Maximum Speed Grade[1]		400 MHz		
Maximum System Clock Speed		100 MHz		
Package Options		88-Lead LFCSP	88-Lead LFCSP	120-Lead LQFP

[1] For valid clock combinations, see Table 14, Table 15, Table 16, and Table 24.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW-POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which provides the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF50x processors are highly integrated system-on-a-chip solutions for the next generation of embedded industrial, instrumentation, and power/motion control applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include a watchdog timer; two 32-bit up/down counters with rotary support; eight 32-bit timers/counters with PWM support; six pairs of 3-phase 16-bit center-based PWM units; two dual-channel, full-duplex synchronous serial ports (SPORTs); two serial peripheral interface (SPI) compatible ports; two UARTs with IrDA® support; a parallel peripheral interface (PPI); a removable storage interface (RSI) controller; an internal ADC with 12 channels, 12 bits, up to 2 MSPS, and ACM controller; a controller area network (CAN) controller; a 2-wire interface (TWI) controller; and an internal 32M bit flash.

PROCESSOR PERIPHERALS

The ADSP-BF50x processors contain a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). These Blackfin processors contain high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The SPORT, SPI, UART, PPI, and RSI peripherals are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including boot ROM and internal 32M bit synchronous burst flash. Multiple on-chip buses running at up to 100 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF50x processors include an interface to an off-chip voltage regulator in support of the processor's dynamic power management capability.

FLASH MEMORY

The ADSP-BF504F and ADSP-BF506F processors include an on-chip 32M bit (×16, multiple bank, burst) Flash memory. The features of this memory include:

- Synchronous/asynchronous read
  - Synchronous burst read mode: 50 MHz
  - Asynchronous/synchronous read mode
  - Random access times: 70 ns
- Synchronous burst read suspend
- Memory blocks
  - Multiple bank memory array: 4M bit banks
  - Parameter blocks (top location)
- Dual operations
  - Program erase in one bank while read in others
  - No delay between read and write operations
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked or locked down
- Security
  - 128-bit user programmable OTP cells
  - 64-bit unique device number
- Common Flash interface (CFI)
- 100,000 program/erase cycles per block

Flash memory ships from the factory in an erased state *except* for block 0 of the parameter bank. Block 0 of the Flash memory parameter bank ships from the factory in an unknown state. An erase operation should be performed prior to programming this block.

DMA CONTROLLERS

The processor has multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interface. DMA-capable peripherals include the SPORTs, SPI ports, UARTs, RSI, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The processor DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the processor DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels, which are provided for transfers between the various memories of the processor system with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

WATCHDOG TIMER

The processor includes a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a core and system reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine whether the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK) at a maximum frequency of f_{SCLK}.

TIMERS

There are nine general-purpose programmable timer units in the processors. Eight timers have an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF pins, to an external clock input to the PPI_CLK input pin, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

- DMA operations with single-cycle overhead—Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts—Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability—Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF50x processors have two SPI-compatible ports that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins MOSI (Master Output-Slave Input) and MISO (Master Input-Slave Output) and a clock pin, serial clock (SCK). An SPI chip select input pin ($\overline{\text{SPIx\_SS}}$) lets other SPI devices select the processor, and three SPI chip select output pins ($\overline{\text{SPIx\_SEL3–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS (UARTS)

The ADSP-BF50x Blackfin processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports. Each UART port provides a simplified UART interface to other peripherals or hosts, enabling full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits; one or two stop bits; and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O). The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access). The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates. Flexible interrupt timing options are available on the transmit side.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16^{(1-EDBO)} \times UART\_Divisor}$$

Where the 16-bit UART divisor comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant eight bits), and the EDBO is a bit in the UARTx_GCTL register.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The UARTs feature a pair of $\overline{\text{UAx\_RTS}}$ (request to send) and $\overline{\text{UAx\_CTS}}$ (clear to send) signals for hardware flow purposes. The transmitter hardware is automatically prevented from sending further data when the $\overline{\text{UAx\_CTS}}$ input is de-asserted. The receiver can automatically de-assert its $\overline{\text{UAx\_RTS}}$ output when the enhanced receive FIFO exceeds a certain high-water level. The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

- Input mode—Frame syncs and data are inputs into the PPI.
- Frame capture mode—Frame syncs are outputs from the PPI, but data are inputs.
- Output mode—Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF50x processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

RSI INTERFACE

The removable storage interface (RSI) controller acts as the host interface for multimedia cards (MMC), secure digital memory cards (SD), secure digital input/output cards (SDIO), and CE-ATA hard disk drives. The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card or CE-ATA hard disk drive
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit, and 8-bit MMC modes
- Support for 4-bit and 8-bit CE-ATA hard disk drives
- A ten-signal external interface with clock, command, and up to eight data lines
- Card detection using one of the data signals
- Card interface clock generation from SCLK
- SDIO interrupt and read wait features
- CE-ATA command completion signal recognition and disable

CONTROLLER AREA NETWORK (CAN) INTERFACE

The ADSP-BF50x processors provide a CAN controller that is a communication controller implementing the Controller Area Network (CAN) V2.0B protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. CAN is well suited for control applications due to its capability to communicate reliably over a network since the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller is based on a 32-entry mailbox RAM and supports both the standard and extended identifier (ID) message formats specified in the CAN protocol specification, revision 2.0, part B.

- Boot from serial SPI memory, EEPROM or flash (BMODE = 0x3)—8-, 16-, 24-, or 32-bit addressable devices are supported. The processor uses the PF13 GPIO pin to select a single SPI EEPROM/flash device (connected to the SPI0 interface) and submits a read command and successive address bytes (0x00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected. Pull-up resistors are required on the SPI0_SEL1 and MISO pins. By default, a value of 0x85 is written to the SPI_BAUD register.
- Boot from SPI host device (BMODE = 0x4)—The processor operates in SPI slave mode and is configured to receive the bytes of the LDR file from an SPI host (master) agent. The HWAIT signal must be interrogated by the host before every transmitted byte. A pull-up resistor is required on the SPI0_SS input. A pull-down on the serial clock (SCK) may improve signal quality and booting robustness.
- Boot from PPI host device (BMODE = 0x5)—The processor operates in PPI slave mode and is configured to receive the bytes of the LDR file from a PPI host (master) agent.
- Boot from UART0 host on Port G (BMODE = 0x7)—Using an autobaud handshake sequence, a boot-stream formatted program is downloaded by the host. The host selects a bit rate within the UART clocking capabilities.

  When performing the autobaud detection, the UART expects an "@" (0x40) character (eight bits data, one start bit, one stop bit, no parity bit) on the UA0_RX pin to determine the bit rate. The UART then replies with an acknowledgement composed of 4 bytes (0xBF, the value of UART0_DLL, the value of UART0_DLH, then 0x00). The host can then download the boot stream. The processor deasserts the UA0_RTS output to hold off the host; UA0_CTS functionality is not enabled at boot time.

For each of the boot modes, a 16 byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the address stored in the EVT1 register.

The boot kernel differentiates between a regular hardware reset and a wakeup-from-hibernate event to speed up booting in the later case. Bits 6-4 in the system reset configuration (SYSCR) register can be used to bypass the pre-boot routine and/or boot kernel in case of a software reset. They can also be used to simulate a wakeup-from-hibernate boot in the software reset case.

The boot process can be further customized by "initialization code." This is a piece of code that is loaded and executed prior to the regular application boot. Typically, this is used to speed up booting by managing the PLL, clock frequencies, wait states, or serial bit rates.

The boot ROM also features C-callable functions that can be called by the user application at run time. This enables second-stage boot or boot management schemes to be implemented with ease.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

Table 12. ADC—Signal Descriptions (ADSP-BF506F Processor Only)

Signal Name	Type	Function
DGND	G	Digital Ground. This is the ground reference point for all digital circuitry on the internal ADC. Both DGND pins should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
REF SELECT	I	Internal/External Reference Selection. Logic input. If this pin is tied to DGND, the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. In addition, Pin $D_{CAP}A$ and Pin $D_{CAP}B$ must be tied to decoupling capacitors. If the REF SELECT pin is tied to a logic high, an external reference can be supplied to the internal ADC through the $D_{CAP}A$ and/or $D_{CAP}B$ pins.
AV_{DD}	P	Analog Supply Voltage, 2.7 V to 5.25 V. This is the only supply voltage for all analog circuitry on the internal ADC. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. This supply should be decoupled to AGND.
$D_{CAP}A$, $D_{CAP}B$ (V_{REF})	I	Decoupling Capacitor Pins. Decoupling capacitors (470 nF recommended) are connected to these pins to decouple the reference buffer for each respective ADC. Provided the output is buffered, the on-chip reference can be taken from these pins and applied externally to the rest of a system. The range of the external reference is dependent on the analog input range selected.
AGND	G	Analog Ground. Ground reference point for all analog circuitry on the internal ADC. All analog input signals and any external reference signal should be referred to this AGND voltage. All three of these AGND pins should connect to the AGND plane of a system. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
V_{A1} to V_{A6}	I	Analog Inputs of ADC A. These may be programmed as six single-ended channels or three true differential analog input channel pairs. See Table 53 (Analog Input Type and Channel Selection).
V_{B1} to V_{B6}	I	Analog Inputs of ADC B. These may be programmed as six single-ended channels or three true differential analog input channel pairs. See Table 53 (Analog Input Type and Channel Selection).
RANGE	I	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic low, the analog input range is 0 V to V_{REF}. If this pin is tied to a logic high when $\overline{CS}$ goes low, the analog input range is $2 \times V_{REF}$. For details, see Table 53 (Analog Input Type and Channel Selection).
SGL/$\overline{DIFF}$	I	Logic Input. This pin selects whether the analog inputs are configured as differential pairs or single ended. A logic low selects differential operation while a logic high selects single-ended operation. For details, see Table 53 (Analog Input Type and Channel Selection).
A0 to A2	I	Multiplexer Select. Logic inputs. These inputs are used to select the pair of channels to be simultaneously converted, such as Channel 1 of both ADC A and ADC B, Channel 2 of both ADC A and ADC B, and so on. The pair of channels selected may be two single-ended channels or two differential pairs. The logic states of these pins need to be set up prior to the acquisition time and subsequent falling edge of $\overline{CS}$ to correctly set up the multiplexer for that conversion. For further details, see Table 53 (Analog Input Type and Channel Selection).
$\overline{CS}$	I	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the internal ADC and framing the serial data transfer. When connecting $\overline{CS}$ to a processor signal that is three-stated during reset and/or hibernate, adding a pull-up resistor may prove useful to avoid random ADC operation.
ADSCLK	I	Serial Clock. Logic input. A serial clock input provides the ADSCLK for accessing the data from the internal ADC. This clock is also used as the clock source for the conversion process.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}	High Level Output Voltage	V_{DDEXT} = 1.7 V, I_{OH} = –0.5 mA	1.35			V
	High Level Output Voltage	V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA	2.0			V
	High Level Output Voltage	V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{DDEXT} = 1.7 V/2.25 V/3.0 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	High Level Input Current[1]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10.0	µA
I_{IL}	Low Level Input Current[1]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10.0	µA
I_{IHP}	High Level Input Current JTAG[2]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			75.0	µA
I_{OZH}	Three-State Leakage Current[3]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10.0	µA
I_{OZHTWI}	Three-State Leakage Current[4]	V_{DDEXT} = 3.0 V, V_{IN} = 5.5 V			10.0	µA
I_{OZL}	Three-State Leakage Current[3]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10.0	µA
C_{IN}	Input Capacitance[5,6]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		5	8	pF
C_{INTWI}	Input Capacitance[4,6]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V			10	pF
$I_{DDDEEPSLEEP}$[7]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.2 V, f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		1.85		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.2 V, f_{SCLK} = 25 MHz, T_J = 25°C		2.1		mA
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.2 V, f_{CCLK} = 50 MHz, T_J = 25°C, ASF = 0.42		18		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.40 V, f_{CCLK} = 400 MHz, T_J = 25°C, ASF = 1.00		104		mA
	V_{DDINT} Current	V_{DDINT} = 1.225 V, f_{CCLK} = 300 MHz, T_J = 25°C, ASF = 1.00		69		mA
	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 200 MHz, T_J = 25°C, ASF = 1.00		51		mA
$I_{DDHIBERNATE}$[8]	Hibernate State Current	V_{DDEXT} = 3.30 V, $V_{DDFLASH}$ = 1.8 V, T_J = 25°C, CLKIN = 0 MHz (V_{DDINT} = 0 V)		40		µA
$I_{DDSLEEP}$[9]	V_{DDINIT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			Table 18 + (.16 × V_{DDINT} × f_{SCLK})	mA[10]
$I_{DDDEEPSLEEP}$[9]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 18	mA
I_{DDINT}[9]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} ≥ 0 MHz			Table 18 + (Table 19 × ASF) + (.16 × V_{DDINT} × f_{SCLK})	mA
$I_{DDFLASH1}$	Flash Memory Supply Current 1 — Asynchronous Read (5 MHz NORCLK[11])			10	20	mA
	Flash Memory Supply Current 1 — Synchronous Read (50 MHz NORCLK[11])	4 Word		18	20	mA
		8 Word		20	22	mA
		16 Word		25	27	mA
		Continuous		28	30	mA

Parameter		Test Conditions	Min	Typical	Max	Unit
$I_{DDFLASH2}$	Flash Memory Supply Current 2 — Reset/Powerdown			15	50	µA
$I_{DDFLASH3}$	Flash Memory Supply Current 3 — Standby			15	50	µA
$I_{DDFLASH4}$	Flash Memory Supply Current 4 — Automatic Standby			15	50	µA
$I_{DDFLASH5}$	Flash Memory Supply Current 5 — Program			15	40	mA
	Flash Memory Supply Current 5 — Erase			15	40	mA
$I_{DDFLASH6}$	Flash Memory Supply Current 6 — Dual Operations	Program/Erase in one bank, asynchronous read in another bank		25	60	mA
		Program/Erase in one bank, synchronous read in another bank		43	70	mA
$I_{DDFLASH7}$	Flash Memory Supply Current 7 — Program/Erase Suspended (Standby)			15	50	µA

[1] Applies to input pins.
[2] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[3] Applies to three-statable pins.
[4] Applies to bidirectional pins SCL and SDA.
[5] Applies to all signal pins, except SCL and SDA.
[6] Guaranteed, but not tested.
[7] See the *ADSP-BF50x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[8] Applies to V_{DDEXT} supply only. Clock inputs are tied high or low.
[9] Guaranteed maximum specifications.
[10] Unit for V_{DDINT} is V (Volts). Unit for f_{SCLK} is MHz. Example: 1.4 V, 75 MHz would be $0.16 \times 1.4 \times 75 = 16.8$ mA adder.
[11] See the *ADSP-BF50x Blackfin Processor Hardware Reference Manual* for definition of NORCLK.

Parallel Peripheral Interface Timing

Table 27 and Figure 14 on Page 35, Figure 20 on Page 40, and Figure 22 on Page 41 describe parallel peripheral interface operations.

Table 27. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{PCLKW}	PPI_CLK Width[1]	t_{SCLK} – 1.5		t_{SCLK} – 1.5		ns
t_{PCLK}	PPI_CLK Period[1]	2 × t_{SCLK} – 1.5		2 × t_{SCLK} – 1.5		ns
Timing Requirements—GP Input and Frame Capture Modes						
t_{PSUD}	External Frame Sync Startup Delay[2]	4 × t_{PCLK}		4 × t_{PCLK}		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.7		6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.5		1.5		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	4.1		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	2		1.6		ns
Switching Characteristics—GP Output and Frame Capture Modes						
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		8.7		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		8.7		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	2.3		1.9		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$

[2] The PPI port is fully enabled 4 PPI clock cycles after the PAB write to the PPI port enable bit. Only after the PPI port is fully enabled are external frame syncs and data words guaranteed to be received correctly by the PPI peripheral.

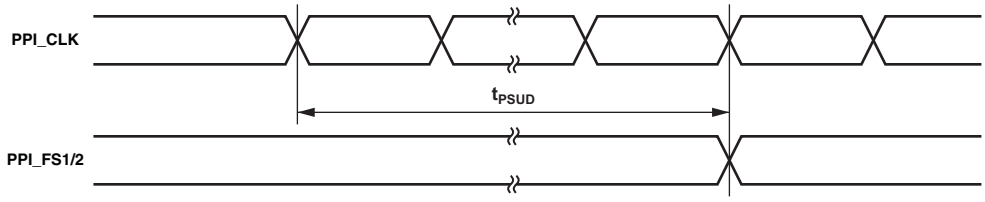


Figure 13. PPI with External Frame Sync Timing

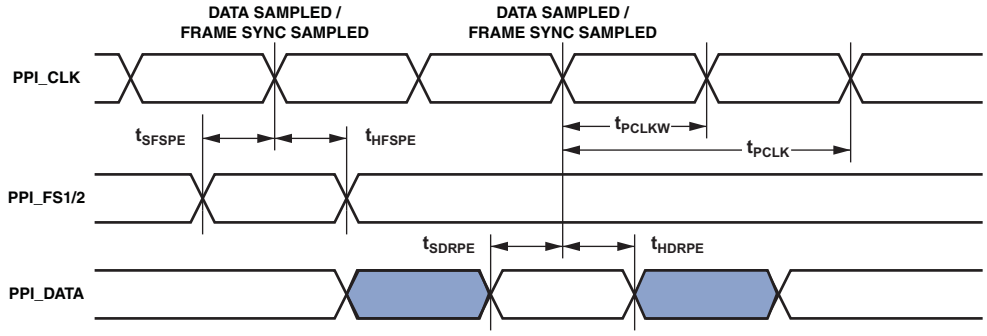


Figure 14. PPI GP Rx Mode with External Frame Sync Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the *ADSP-BF50x Hardware Reference Manual*.

General-Purpose Port Timing

Table 36 and Figure 25 describe general-purpose port operations.

Table 36. General-Purpose Port Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirement						
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
Switching Characteristic						
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT High	0	11.0	0	8.9	ns

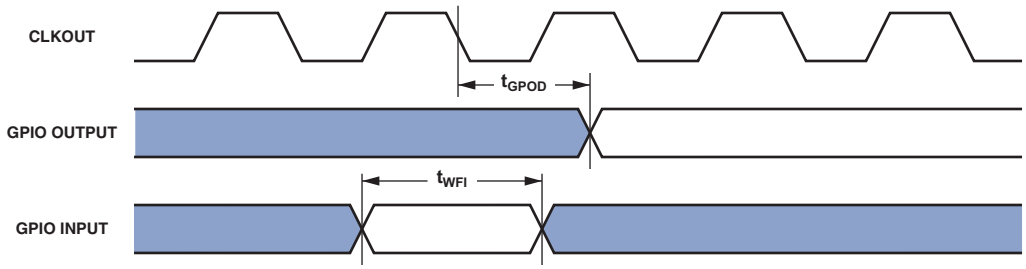


Figure 25. General-Purpose Port Timing

PROCESSOR—OUTPUT DRIVE CURRENTS

Figure 32 through Figure 40 show typical current-voltage characteristics for the output drivers of the ADSP-BF50xF processors.

The curves represent the current drive capability of the output drivers. See Table 11 on Page 22 for information about which driver type corresponds to a particular pin.

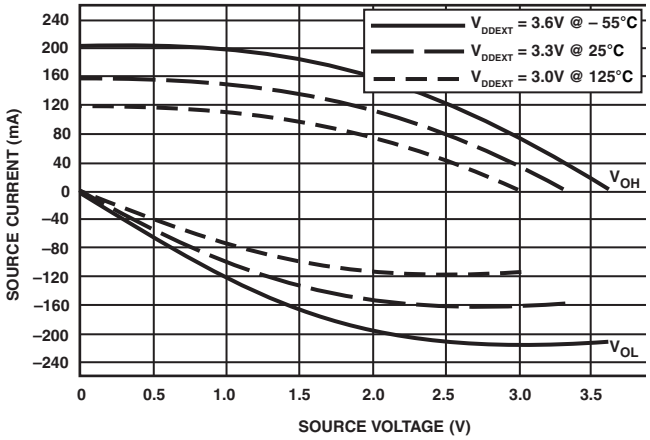


Figure 32. Driver Type B Current (3.3 V V_{DDEXT})

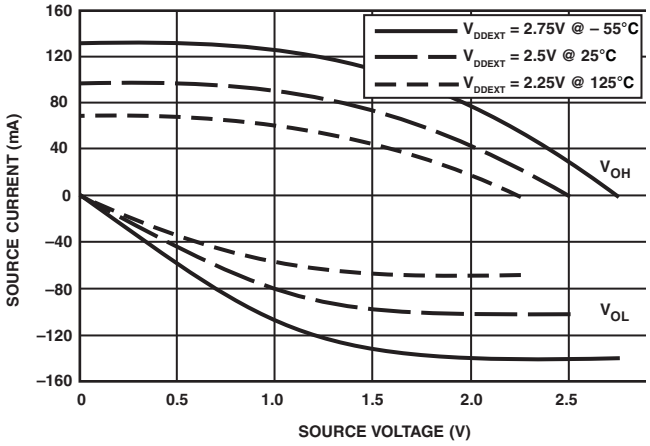


Figure 33. Driver Type B Current (2.5 V V_{DDEXT})

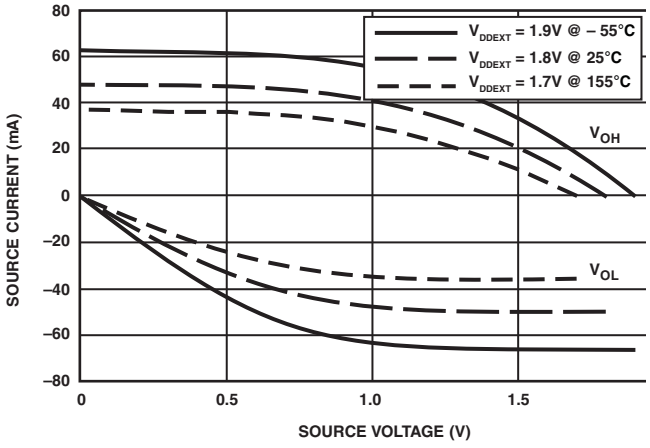


Figure 34. Driver Type B Current (1.8 V V_{DDEXT})

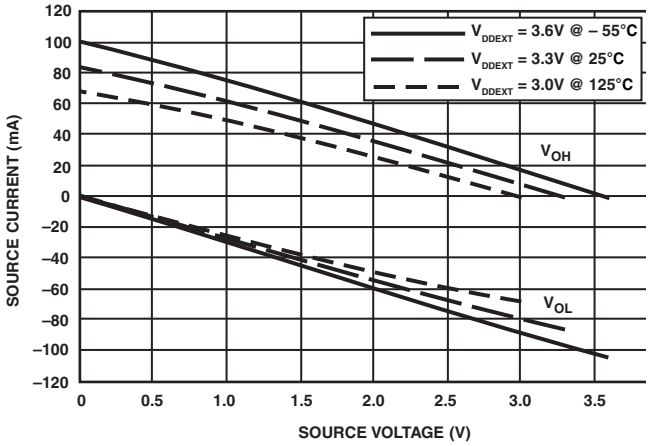


Figure 35. Driver Type C Current (3.3 V V_{DDEXT})

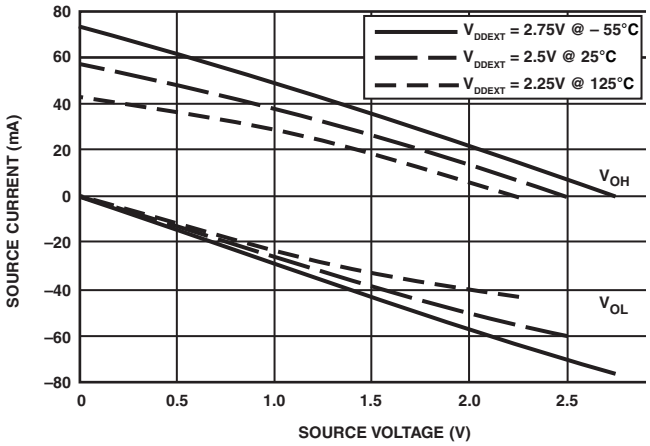


Figure 36. Drive Type C Current (2.5 V V_{DDEXT})

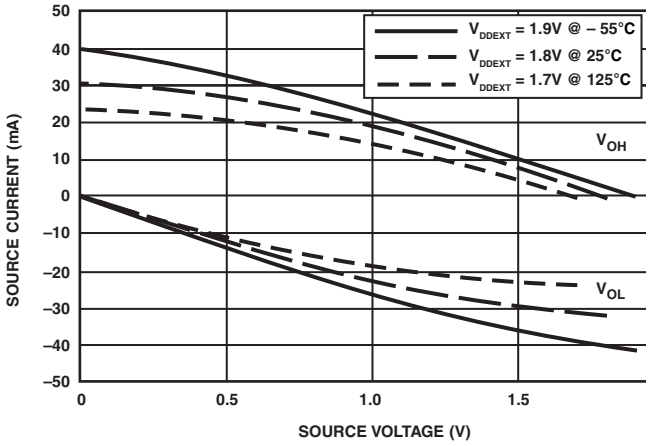


Figure 37. Driver Type C Current (1.8 V V_{DDEXT})

Table 47. Operating Conditions (Analog, Voltage Reference, and Logic I/O) (Continued)

Parameter	Specification	Unit	Test Conditions/Comments
DIGITAL LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V min	No DC load (I_{OH} = 0 mA)
Output Low Voltage, V_{OL}	0.4	V max	No DC load (I_{OL} = 0 mA)
Floating State Leakage Current	±1	µA max	V_{IN} = 0 V or V_{DRIVE}
Floating State Output Capacitance[4]	7	pF typ	
Output Coding[8]	Straight (natural) binary twos complement		

[1] V_{IN-} or V_{IN+} must remain within GND/V_{DD}.
[2] V_{IN-} = 0 V for specified performance. For full input range on V_{IN-} pin, see Figure 74 and Figure 75.
[3] For full common-mode range, see Figure 70 and Figure 71.
[4] Sample tested during initial release to ensure compliance.
[5] Relates to Pin D_{CAP}A or Pin D_{CAP}B (V_{REF}).
[6] See ADC—Terminology on Page 61.
[7] External voltage reference applied to Pins D_{CAP}A, Pin D_{CAP}B (V_{REF}).
[8] See Table 52 and Table 53.

Table 48. Operating Conditions (ADC Performance/Accuracy)

Parameter	Specification	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal-to-Noise Ratio (SNR)	71	dB min	f_{IN} = 14 kHz sine wave; differential mode
	69	dB min	f_{IN} = 14 kHz sine wave; single-ended and pseudo differential modes
Signal-to-(Noise + Distortion) Ratio (SINAD)[1]	70	dB min	f_{IN} = 14 kHz sine wave; differential mode
	68	dB min	f_{IN} = 14 kHz sine wave; single-ended and pseudo differential modes
Total Harmonic Distortion (THD)[1]	–77	dB max	f_{IN} = 14 kHz sine wave; differential mode
	–73	dB max	f_{IN} = 14 kHz sine wave; single-ended and pseudo differential modes
Spurious-Free Dynamic Range (SFDR)[1]	–75	dB max	f_{IN} = 50 kHz sine wave
Intermodulation Distortion (IMD)[1,2]			f_a = 30 kHz, fb = 50 kHz
Second-Order Terms	–88	dB typ	
Third-Order Terms	–88	dB typ	
Channel-to-Channel Isolation	–88	dB typ	
SAMPLE AND HOLD			
Aperture Delay[2]	11	ns max	
Aperture Jitter[2]	50	ps typ	
Aperture Delay Matching[2]	200	ps max	
Full Power Bandwidth	33/26	MHz typ	@ 3 dB, AV_{DD}, DV_{DD} = 5 V/AV_{DD}, DV_{DD} = 3 V
	3.5/3	MHz typ	@ 0.1 dB, AV_{DD}, DV_{DD} = 5 V/AV_{DD}, DV_{DD} = 3 V

Table 48. Operating Conditions (ADC Performance/Accuracy) (Continued)

Parameter	Specification	Unit	Test Conditions/Comments
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity (INL)[1]	±1	LSB max	±0.7 LSB typ; differential mode
	±1.5	LSB max	±0.9 LSB typ; single-ended and pseudo differential modes
Differential Nonlinearity (DNL)[1, 3]	±0.99	LSB max	Differential mode
	–0.99/+1.5	LSB max	Single-ended and pseudo differential modes
Straight Natural Binary Output Coding			
Offset Error[1,2]	±7	LSB max	
Offset Error Match[1,2]	±2	LSB typ	
Gain Error[1,2]	±2.5	LSB max	
Gain Error Match[1,2]	±0.5	LSB typ	
Twos Complement Output Coding			
Positive Gain Error[1,2]	±2	LSB max	
Positive Gain Error Match[1,2]	±0.5	LSB typ	
Zero Code Error[1,2]	±5	LSB max	
Zero Code Error Match[1,2]	±1	LSB typ	
Negative Gain Error[1,2]	±2	LSB max	
Negative Gain Error Match[1,2]	±0.5	LSB typ	
CONVERSION RATE			
Conversion Time	14	ADSCLK cycles	437.5 ns with ADSCLK = 32 MHz
Track-and-Hold Acquisition Time[2]	90	ns max	Full-scale step input; AV_{DD}, DV_{DD} = 5 V
	110	ns max	Full-scale step input; AV_{DD}, DV_{DD} = 3 V
Throughput Rate	2	MSPS max	

[1] See ADC—Terminology on Page 61.
[2] Sample tested during initial release to ensure compliance.
[3] Guaranteed no missed codes to 12 bits.

Table 49. Operating Conditions (Power[1])

Parameter	Specification	Unit	Test Conditions/Comments
POWER SUPPLY REQUIREMENTS			
V_{DD}	2.7/5.25	V min/V max	
V_{DRIVE}	2.7/5.25	V min/V max	
I_{DD}			Digital Logic Inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	2.3	mA max	V_{DD} = 5.25 V
Operational			
f_S = 2 MSPS	6.4	mA max	V_{DD} = 5.25 V; 5.7 mA typ
f_S = 1.5 MSPS	4	mA max	V_{DD} = 3.6 V; 3.4 mA typ
Partial Power-Down Mode	500	µA max	Static
Full Power-Down Mode (V_{DD})	2.8	µA max	Static
POWER DISSIPATION			
Normal Mode (Operational)	33.6	mW max	V_{DD} = 5.25 V
Partial Power-Down (Static)	2.625	mW max	V_{DD} = 5.25 V
Full Power-Down (Static)	14.7	µW max	V_{DD} = 5.25 V

[1] In this table, V_{DD} refers to both AV_{DD} and DV_{DD}.

determining how much that signal is attenuated in the selected channel with a 50 kHz signal (0 V to V_{REF}). The result obtained is the worst-case across all 12 channels for the ADC.

Intermodulation Distortion (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with non-linearities create distortion products at sum, and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa fb), while the third-order terms include (2fa + fb), (2fa fb), (fa + 2fb), and (fa 2fb).

The ADC is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second-order and third-order terms are specified separately. The calculation of the inter-modulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and V_{IN} of frequency f_S as:

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:

Pf is the power at frequency *f* in the ADC output.

Pf_S is the power at frequency f_S in the ADC output.

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the converter's linearity. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see Figure 50 (PSRR vs. Supply Ripple Frequency Without Supply Decoupling).

Thermal Hysteresis

Thermal hysteresis is defined as the absolute maximum change of reference output voltage (V_{REF}) after the device is cycled through temperature from either:

$$T\_HYS+ = +25°\text{C to } T_{MAX} \text{ to } +25°\text{C}$$

or

$$T\_HYS = +25°\text{C to } T_{MIN} \text{ to } +25°\text{C}$$

It is expressed in ppm by:

$$V_{HYS}\,(ppm) = \left|\frac{V_{REF}(25°\text{C}) - V_{REF}(T\_HYS)}{V_{REF}(25°\text{C})}\right| \times 10^6$$

where:

V_{REF} (25°C) is V_{REF} at 25°C.

V_{REF} *(T_HYS)* is the maximum change of V_{REF} at T_HYS+ or T_HYS.

ADC—THEORY OF OPERATION

The following sections describe the ADC theory of operation.

Circuit Information

The ADC is a fast, micropower, dual, 12-bit, single-supply, ADC that operates from a 2.7 V to a 5.25 V supply. When operated from a 5 V supply, the ADC is capable of throughput rates of up to 2 MSPS when provided with a 32 MHz clock, and a throughput rate of up to 1.5 MSPS at 3 V.

The ADC contains two on-chip, differential track-and-hold amplifiers, two successive approximation ADCs, and a serial interface with two separate data output pins.

The serial clock input accesses data from the part but also provides the clock source for each successive approximation ADC. The analog input range for the part can be selected to be a 0 V to V_{REF} input or a 2 × V_{REF} input, configured with either single-ended or differential analog inputs. The ADC has an on-chip 2.5 V reference that can be overdriven when an external reference is preferred. If the internal reference is to be used elsewhere in a system, then the output needs to buffered first.

The ADC also features power-down options to allow power saving between conversions. The power-down feature is implemented via the standard serial interface, as described in the ADC—Modes of Operation section.

Converter Operation

The ADC has two successive approximation ADCs, each based around two capacitive DACs. Figure 62 (ADC Acquisition Phase) and Figure 63 (ADC Conversion Phase) show simplified schematics of one of these ADCs in acquisition and conversion phase, respectively. The ADC is comprised of control logic, a SAR, and two capacitive DACs. In Figure 62 (ADC Acquisition Phase) (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

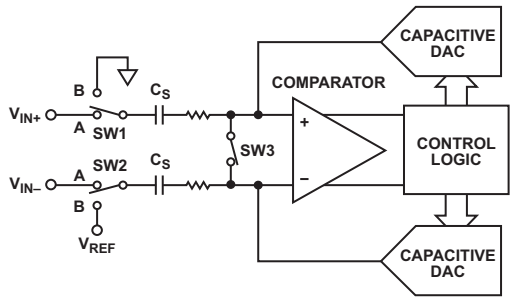


Figure 62. ADC Acquisition Phase

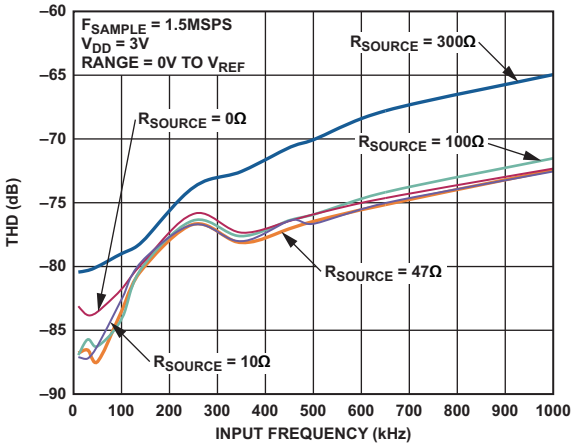


Figure 66. THD vs. Analog Input Frequency for Various Source Impedances, Differential Mode

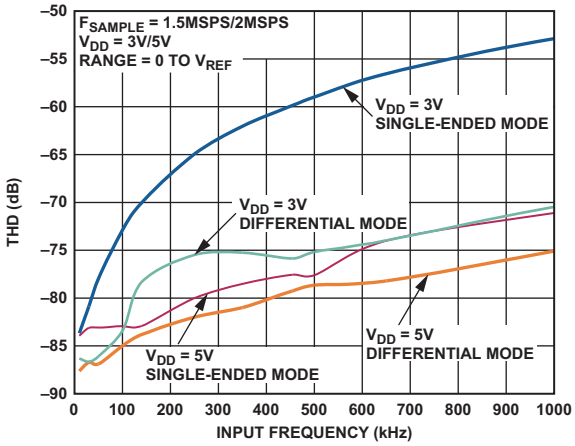


Figure 67. THD vs. Analog Input Frequency for Various Supply Voltages

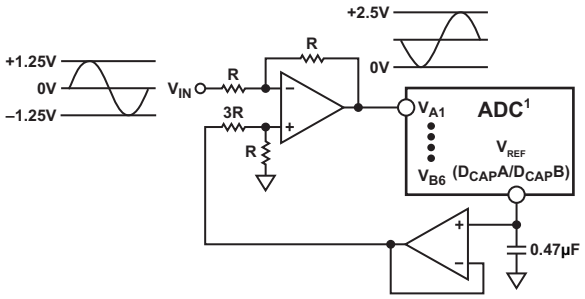
Analog Inputs

The ADC has a total of 12 analog inputs. Each on-board ADC has six analog inputs that can be configured as six single-ended channels, three pseudo differential channels, or three fully differential channels. These may be selected as described in the Analog Input Selection section.

Single-Ended Mode

The ADC can have a total of 12 single-ended analog input channels. In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 to V_{REF} or 0 to 2 × V_{REF}.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal to make it correctly formatted for the ADC. Figure 68 shows a typical connection diagram when operating the ADC in single-ended mode.



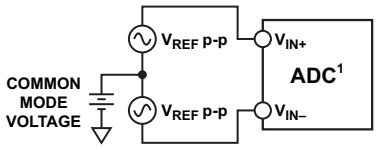
[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 68. Single-Ended Mode Connection Diagram

Differential Mode

The ADC can have a total of six differential analog input pairs.

Differential signals have some benefits over single-ended signals, including noise immunity based on the device's common-mode rejection and improvements in distortion performance. Figure 69 (Differential Input Definition) defines the fully differential analog input of the ADC.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 69. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair (V_{IN+} V_{IN-}). V_{IN+} and V_{IN-} should be simultaneously driven by two signals each of amplitude V_{REF} (or 2 × V_{REF}, depending on the range chosen) that are 180° out of phase. The amplitude of the differential signal is, therefore (assuming the 0 to V_{REF} range is selected) –V_{REF} to +V_{REF} peak-to-peak (2 × V_{REF}), regardless of the common mode (CM).

The common mode is the average of the two signals

$$(V_{IN+} + V_{IN-})/2$$

and is, therefore, the voltage on which the two inputs are centered.

This results in the span of each input being CM ± V_{REF}/2. This voltage has to be set up externally and its range varies with the reference value, V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the amplifier's output voltage swing.

Figure 70 (Input Common-Mode Range vs. VREF (0 to VREF Range, VDD = 5 V)) and Figure 71 (Input Common-Mode Range vs. VREF (2 × VREF Range, VDD = 5 V)) show how the common-mode range typically varies with V_{REF} for a 5 V power

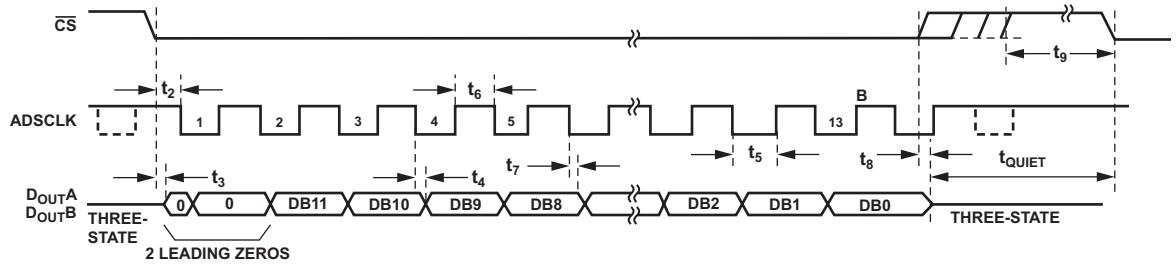


Figure 87. Serial Interface Timing Diagram

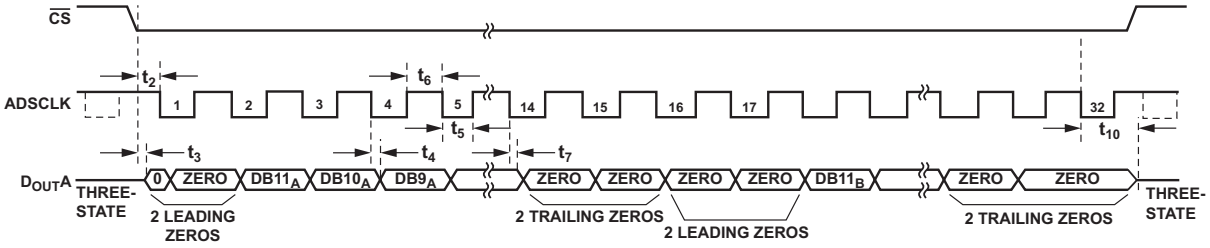


Figure 88. Reading Data from Both ADCs on One D_{OUT} Line with 32 ADSCLKs

Table 55. 120-Lead LQFP Lead Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	V_{DDEXT}	31	PG3	61	V_{DDINT}	91	V_{B2}
2	PF2	32	PG4	62	V_{DDEXT}	92	V_{B1}
3	PF4	33	TDI	63	$V_{DDFLASH}$	93	AGND
4	PF3	34	TCK	64	V_{DDEXT}	94	$D_{CAP}B$
5	PF5	35	TMS	65	V_{DDINT}	95	RANGE
6	V_{DDEXT}	36	TDO	66	V_{DDEXT}	96	SGL/$\overline{DIFF}$
7	PF6	37	$\overline{TRST}$	67	V_{DDEXT}	97	A2
8	PF7	38	PG5	68	$\overline{EMU}$	98	A1
9	PF8	39	PG6	69	$V_{DDFLASH}$	99	AGND
10	PF9	40	PG7	70	EXT_WAKE	100	A0
11	$\overline{NMI}$	41	V_{DDEXT}	71	$\overline{PG}$	101	$\overline{CS}$
12	$\overline{RESET}$	42	V_{DDINT}	72	NC	102	ADSCLK
13	GND	43	PG8	73	AGND	103	$D_{OUT}B$
14	PF10	44	PG9	74	DGND	104	DGND
15	V_{DDEXT}	45	PG10	75	REF_SELECT	105	$D_{OUT}A$
16	PF11	46	PG11	76	AV_{DD}	106	V_{DRIVE}
17	GND	47	PG12	77	$D_{CAP}A$	107	DV_{DD}
18	PF12	48	PG13	78	AGND	108	GND
19	PF13	49	PG14	79	AGND	109	GND
20	V_{DDEXT}	50	PG15	80	V_{A1}	110	CLKIN
21	PF14	51	V_{DDEXT}	81	V_{A2}	111	XTAL
22	PF15	52	V_{DDINT}	82	AGND	112	V_{DDEXT}
23	V_{DDEXT}	53	V_{DDINT}	83	V_{A3}	113	PH0
24	V_{DDINT}	54	SDA	84	V_{A4}	114	PH2
25	$V_{DDFLASH}$	55	SCL	85	V_{A5}	115	PH1
26	V_{DDEXT}	56	BMODE2	86	V_{A6}	116	V_{DDEXT}
27	PG0	57	BMODE1	87	V_{B6}	117	V_{DDINT}
28	PG1	58	BMODE0	88	V_{B5}	118	PF0
29	PG2	59	V_{DDEXT}	89	V_{B4}	119	PF1
30	V_{DDEXT}	60	NC	90	V_{B3}	120	EXTCLK
						121*	GND
						122**	AGND

* Pin no. 121 is the GND supply (see Figure 89 and Figure 90) for the processor (4.6mm × 6.17mm); this pad **must** connect to GND.
** Pin no. 122 is the AGND supply (see Figure 89 and Figure 90) for the ADC (2.81mm × 2.81mm); this pad **must** connect to AGND.

Figure 89 shows the top view of the 120-lead LQFP package lead configuration.

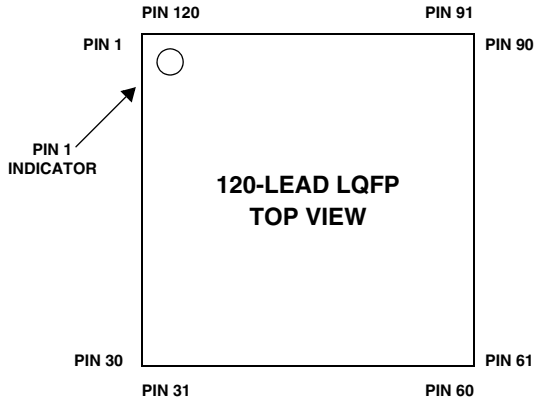


Figure 89. 120-Lead LQFP Package Lead Configuration (Top View)

Figure 90 shows the bottom view of the 120-lead LQFP package lead configuration.

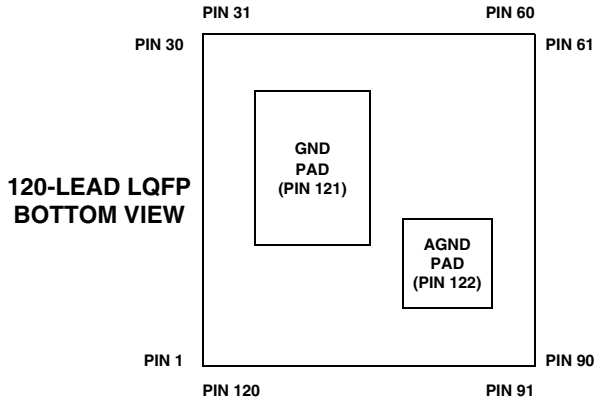


Figure 90. 120-Lead LQFP Package Lead Configuration (Bottom View)

AUTOMOTIVE PRODUCTS

The ADBF504W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 58 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 58. Automotive Products

Automotive Models[1,2]	Temperature Range[3]	Processor Instruction Rate (Maximum)	Flash Memory	Package Description	Package Option
ADBF504WYCPZ4XX	–40°C to +105°C	400 MHz	N/A	88-Lead LFCSP_VQ	CP-88-5

[1] Z = RoHS compliant part.
[2] The use of xx designates silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 26 for junction temperature (T_J) specification which is the only temperature specification.

ORDERING GUIDE

Model[1,2]	Temperature Range[3,4]	Processor Instruction Rate (Maximum)	Flash Memory	Package Description	Package Option
ADSP-BF504BCPZ-3F	–40°C to +85°C	300 MHz	32M bit	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504BCPZ-4	–40°C to +85°C	400 MHz	N/A	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504BCPZ-4F	–40°C to +85°C	400 MHz	32M bit	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504KCPZ-3F	0°C to +70°C	300 MHz	32M bit	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504KCPZ-4	0°C to +70°C	400 MHz	N/A	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504KCPZ-4F	0°C to +70°C	400 MHz	32M bit	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF506BSWZ-3F	–40°C to +85°C	300 MHz	32M bit	120-Lead LQFP_EP	SW-120-2
ADSP-BF506BSWZ-4F	–40°C to +85°C	400 MHz	32M bit	120-Lead LQFP_EP	SW-120-2
ADSP-BF506KSWZ-3F	0°C to +70°C	300 MHz	32M bit	120-Lead LQFP_EP	SW-120-2
ADSP-BF506KSWZ-4F	0°C to +70°C	400 MHz	32M bit	120-Lead LQFP_EP	SW-120-2

[1] Z = RoHS compliant part.
[2] For feature comparison between ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors, see the Processor Comparison in Table 1 on Page 3.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 26 for junction temperature (T_J) specification which is the only temperature specification.
[4] Temperature range 0°C to +70°C is classified as commercial, and temperature range –40°C to +85°C is classified as industrial.

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