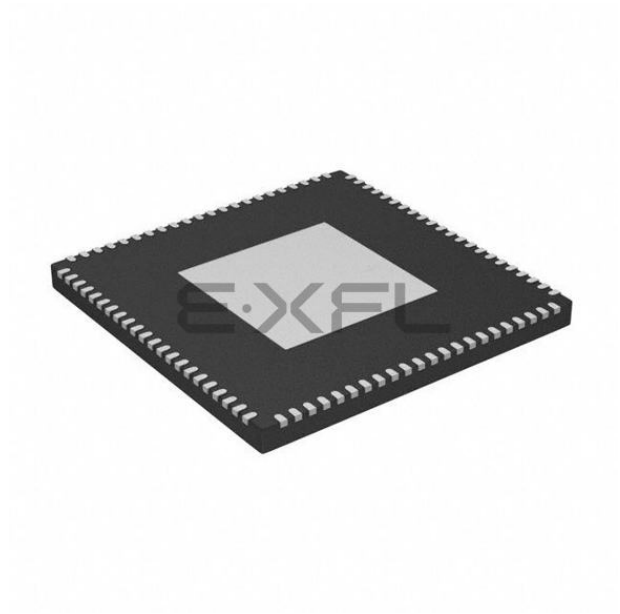

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, EBI/EMI, I²C, IrDA, PPI, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	FLASH (16MB)
On-Chip RAM	68kB
Voltage - I/O	3.30V
Voltage - Core	1.29V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP-VQ (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf504bcpz-4f

GENERAL DESCRIPTION

The ADSP-BF50x processors are members of the Blackfin® family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF50x processors are completely code compatible with other Blackfin processors. ADSP-BF50x processors offer performance up to 400 MHz and reduced static power consumption. Differences with respect to peripheral combinations are shown in Table 1.

Table 1. Processor Comparison

Feature		ADSP-BF504	ADSP-BF504F	ADSP-BF506F
Up/Down/Rotary Counters		2	2	2
Timer/Counters with PWM		8	8	8
3-Phase PWM Units		2	2	2
SPORTs		2	2	2
SPIs		2	2	2
UARTs		2	2	2
Parallel Peripheral Interface		1	1	1
Removable Storage Interface		1	1	1
CAN		1	1	1
TWI		1	1	1
Internal 32M Bit Flash		–	1	1
ADC Control Module (ACM)		1	1	1
Internal ADC		–	–	1
GPIOs		35	35	35
Memory (bytes)	L1 Instruction SRAM	16K	16K	16K
	L1 Instruction SRAM/Cache	16K	16K	16K
	L1 Data SRAM	16K	16K	16K
	L1 Data SRAM/Cache	16K	16K	16K
	L1 Scratchpad	4K	4K	4K
	L3 Boot ROM	4K	4K	4K
Maximum Speed Grade[1]		400 MHz		
Maximum System Clock Speed		100 MHz		
Package Options		88-Lead LFCSP	88-Lead LFCSP	120-Lead LQFP

[1] For valid clock combinations, see Table 14, Table 15, Table 16, and Table 24.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW-POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which provides the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF50x processors are highly integrated system-on-a-chip solutions for the next generation of embedded industrial, instrumentation, and power/motion control applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include a watchdog timer; two 32-bit up/down counters with rotary support; eight 32-bit timers/counters with PWM support; six pairs of 3-phase 16-bit center-based PWM units; two dual-channel, full-duplex synchronous serial ports (SPORTs); two serial peripheral interface (SPI) compatible ports; two UARTs with IrDA® support; a parallel peripheral interface (PPI); a removable storage interface (RSI) controller; an internal ADC with 12 channels, 12 bits, up to 2 MSPS, and ACM controller; a controller area network (CAN) controller; a 2-wire interface (TWI) controller; and an internal 32M bit flash.

PROCESSOR PERIPHERALS

The ADSP-BF50x processors contain a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). These Blackfin processors contain high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The SPORT, SPI, UART, PPI, and RSI peripherals are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including boot ROM and internal 32M bit synchronous burst flash. Multiple on-chip buses running at up to 100 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF50x processors include an interface to an off-chip voltage regulator in support of the processor's dynamic power management capability.

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The data memory holds data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The Blackfin processor views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency core-accessible memory as cache or SRAM and to provide larger, lower cost and performance interface-accessible memory systems. See Figure 3.

The core-accessible L1 memory system is the highest performance memory available to the Blackfin processor. The interface-accessible memory system, accessed through the external bus interface unit (EBIU), provides access to the internal flash memory and boot ROM.

The memory DMA controller provides high bandwidth data movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (Core-Accessible) Memory

The processor has three blocks of core-accessible memory, providing high-bandwidth access to the core.

The first block is the L1 instruction memory, consisting of 32K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory is accessed at full processor speed.

The second core-accessible memory block is the L1 data memory, consisting of 32K bytes of SRAM, of which 16K bytes may be configured as cache. This memory block is accessed at full processor speed.

The third memory block is 4K bytes of scratchpad SRAM, which runs at the same speed as the L1 memories, but this memory is only accessible as data SRAM and cannot be configured as cache memory.

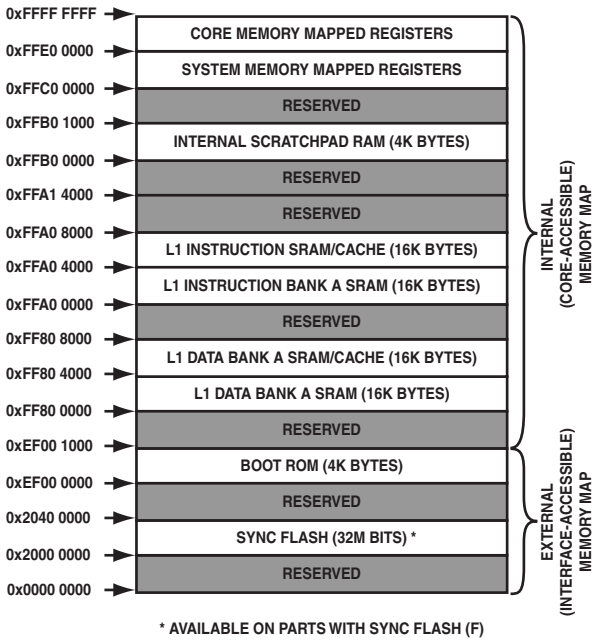


Figure 3. Internal/External Memory Map

External (Interface-Accessible) Memory

External memory is accessed via the EBIU memory port. This 16-bit interface provides a glueless connection to the internal flash memory and boot ROM. Internal flash memory ships from the factory in an erased state except for Block 0 of the parameter bank. Block 0 of the Flash memory parameter bank ships from the factory in an unknown state. An erase operation should be performed prior to programming this block.

I/O Memory Space

The processor does not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks. One contains the control MMRs for all core functions, and the other contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor and emulation modes and appear as reserved space to on-chip peripherals.

- DMA operations with single-cycle overhead—Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts—Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability—Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF50x processors have two SPI-compatible ports that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins MOSI (Master Output-Slave Input) and MISO (Master Input-Slave Output) and a clock pin, serial clock (SCK). An SPI chip select input pin ($\overline{\text{SPIx\_SS}}$) lets other SPI devices select the processor, and three SPI chip select output pins ($\overline{\text{SPIx\_SEL3–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS (UARTS)

The ADSP-BF50x Blackfin processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports. Each UART port provides a simplified UART interface to other peripherals or hosts, enabling full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits; one or two stop bits; and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O). The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access). The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates. Flexible interrupt timing options are available on the transmit side.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16^{(1-EDBO)} \times UART\_Divisor}$$

Where the 16-bit UART divisor comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant eight bits), and the EDBO is a bit in the UARTx_GCTL register.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The UARTs feature a pair of $\overline{\text{UAx\_RTS}}$ (request to send) and $\overline{\text{UAx\_CTS}}$ (clear to send) signals for hardware flow purposes. The transmitter hardware is automatically prevented from sending further data when the $\overline{\text{UAx\_CTS}}$ input is de-asserted. The receiver can automatically de-assert its $\overline{\text{UAx\_RTS}}$ output when the enhanced receive FIFO exceeds a certain high-water level. The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

where the variables in the equations are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

T_{NOM} is the duration running at $f_{CCLKNOM}$

T_{RED} is the duration running at $f_{CCLKRED}$

ADSP-BF50x VOLTAGE REGULATION

The ADSP-BF50x processors require an external voltage regulator to power the V_{DDINT} domain. To reduce standby power consumption, the external voltage regulator can be signaled through EXT_WAKE to remove power from the processor core. This signal is high-true for power-up and may be connected directly to the low-true shut-down input of many common regulators.

While in the hibernate state, all external supplies (V_{DDEXT}, $V_{DDFLASH}$) can still be applied, eliminating the need for external buffers. The external voltage regulator can be activated from this power down state by asserting the $\overline{\text{RESET}}$ pin, which then initiates a boot sequence. EXT_WAKE indicates a wakeup to the external voltage regulator.

The power good ($\overline{\text{PG}}$) input signal allows the processor to start only after the internal voltage has reached a chosen level. In this way, the startup time of the external regulator is detected after hibernation. For a complete description of the power good functionality, refer to the *ADSP-BF50x Blackfin Processor Hardware Reference*.

CLOCK SIGNALS

The processor can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

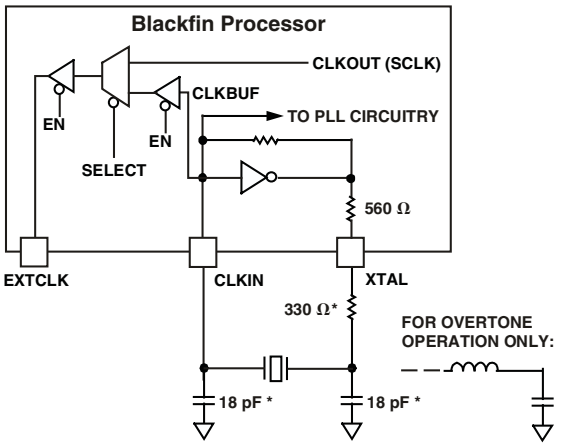
If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 4 fine tune phase and amplitude of the sine frequency.

The capacitor and resistor values shown in Figure 4 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 4. A design procedure for third-overtone operation is discussed in detail in *(EE-168) Using Third Overtone Crystals with the ADSP-218x DSP* on the Analog Devices website (www.analog.com)—use site search on "EE-168."

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 5, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 6×, but it can be modified by a software instruction sequence.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. PLEASE ANALYZE CAREFULLY. FOR FREQUENCIES ABOVE 33 MHz, THE SUGGESTED CAPACITOR VALUE OF 18 pF SHOULD BE TREATED AS A MAXIMUM, AND THE SUGGESTED RESISTOR VALUE SHOULD BE REDUCED TO 0 Ω.

Figure 4. External Crystal Connections

On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register. The maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT} and V_{DDEXT}; the VCO is always permitted to run up to the CCLK frequency specified by the part's speed grade. The EXTCLK pin can be configured to output either the SCLK frequency or the input buffered CLKIN frequency, called CLKBUF. When configured to output SCLK (CLKOUT), the EXTCLK pin acts as a reference signal in many timing specifications. While active by default, it can be disabled using the EBIU_AMGCTL register.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADC AND ACM INTERFACE

This section describes the ADC and ACM interface. System designers should also consult the *ADSP-BF50x Blackfin Processor Hardware Reference* for additional information.

The ADC control module (ACM) provides an interface that synchronizes the controls between the processor and the internal analog-to-digital converter (ADC) module. The ACM is available on the ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors, and the ADC is available on the ADSP-BF506F processor only. The analog-to-digital conversions are initiated by the processor, based on external or internal events.

The ACM allows for flexible scheduling of sampling instants and provides precise sampling signals to the ADC.

ADC APPLICATION HINTS

The following sections provide application hints for using the ADC.

Grounding and Layout Considerations

The analog and digital supplies to the ADC are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the ADC should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All AGND pins should be sunk in the AGND plane. Digital and analog ground planes should be joined in only one place. If the ADC is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the ground pins on the ADC.

Avoid running digital lines under the device as this couples noise onto the die. Avoid running digital lines in the area of the AGND pad as this couples noise onto the ADC die and into the AGND plane. The power supply lines to the ADC should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feed through within the board, traces on opposite sides of the board should run at right angles to each other.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF50x processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF50x Blackfin Processor Hardware Reference* (volumes 1 and 2)
- *Blackfin Processor Programming Reference*
- *ADSP-BF50x Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http:\\www.analog.com\signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 11. Processor—Signal Descriptions (Continued)

Signal Name	Type	Function	Driver Type
PG14/*UA0_RTS*/SD_D6/TMR0/PPI_FS1/CUD1	I/O	GPIO/*UART0 RTS*/SD Data 6/Timer0/PPI FS1/Count Up Dir 1	C
PG15/*UA0_CTS*/SD_D7/TMR1/PPI_FS2/CDG1	I/O	GPIO/*UART0 CTS*/SD Data 7/Timer1/PPI FS2/Count Down Dir 1	C
Port H: *GPIO and Multiplexed Peripherals*			
PH0/*ACM_A2*/DT1PRI/*SPI0_SEL3*/WAKEUP	I/O	GPIO/*ADC CM A2*/SPORT1 TX Pri Data/SPI0 Slave Select 3/Wake-up Input	C
PH1/*ACM_A1*/TFS1/*SPI1_SEL3*/TACLK3	I/O	GPIO/*ADC CM A1*/SPORT1 TX Frame Sync/SPI1 Slave Select 3/Alt Timer CLK 3	C
PH2/*ACM_A0*/TSCLK1/*SPI1_SEL2*/TACI7	I/O	GPIO/*ADC CM A0*/SPORT1 TX Serial CLK/SPI1 Slave Select 2/Alt Capture In 7	C
TWI (2-Wire Interface) Port			
SCL	I/O 5 V	TWI Serial Clock (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	D
SDA	I/O 5 V	TWI Serial Data (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	D
JTAG Port			
TCK	I	JTAG CLK	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$	I	JTAG Reset (This signal should be pulled low if the JTAG port is not used.)	
$\overline{\text{EMU}}$	O	Emulation Output	C
Clock			
CLKIN	I	CLK/Crystal In	
XTAL	O	Crystal Output	
EXTCLK	O	Clock Output	B
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Nonmaskable Interrupt (This signal should be pulled high when not used.)	
BMODE2–0	I	Boot Mode Strap 2-0	
ADSP-BF50x Voltage Regulation I/F			
EXT_WAKE	O	Wake up Indication	C
$\overline{\text{PG}}$	I	Power Good	
Power Supplies		**ALL SUPPLIES MUST BE POWERED** See Operating Conditions on Page 26.	
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Internal Power Supply	
$V_{DDFLASH}$	P	Flash Memory Power Supply	
GND	G	Ground for All Supplies	

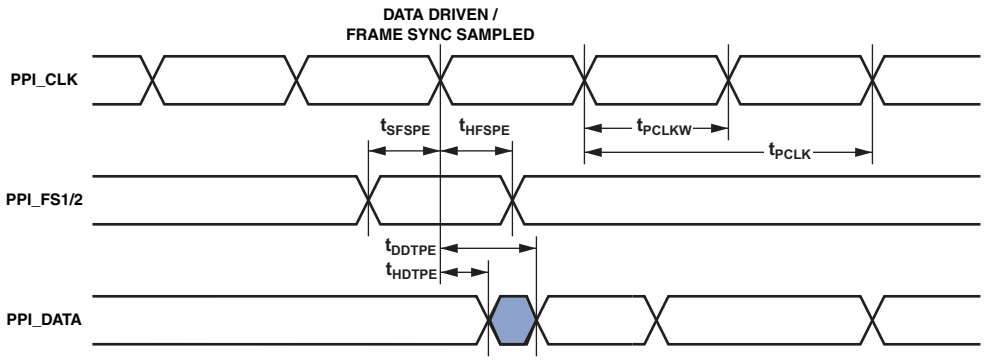


Figure 15. PPI GP Tx Mode with External Frame Sync Timing

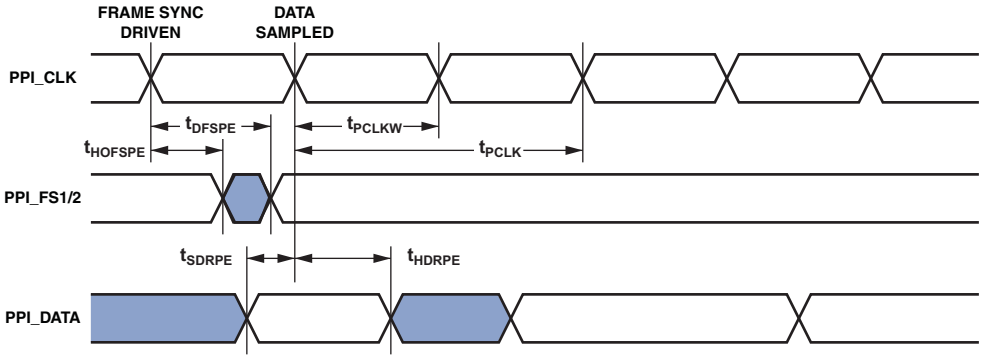


Figure 16. PPI GP Rx Mode with Internal Frame Sync Timing

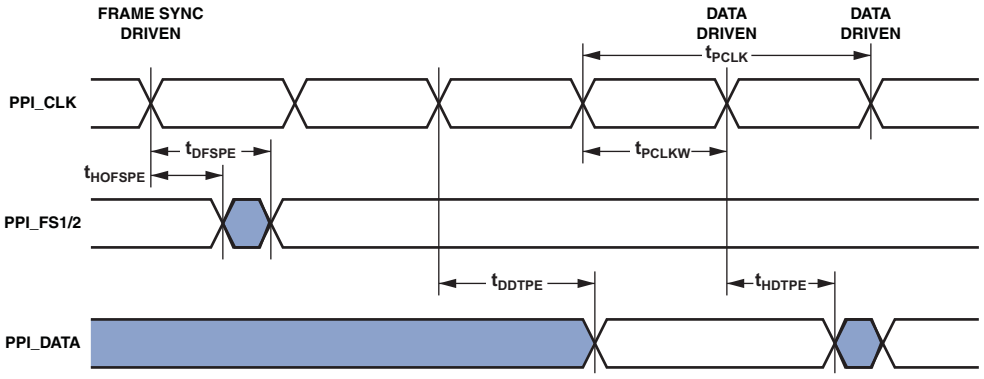


Figure 17. PPI GP Tx Mode with Internal Frame Sync Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the *ADSP-BF50x Hardware Reference Manual*.

General-Purpose Port Timing

Table 36 and Figure 25 describe general-purpose port operations.

Table 36. General-Purpose Port Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirement						
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
Switching Characteristic						
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT High	0	11.0	0	8.9	ns

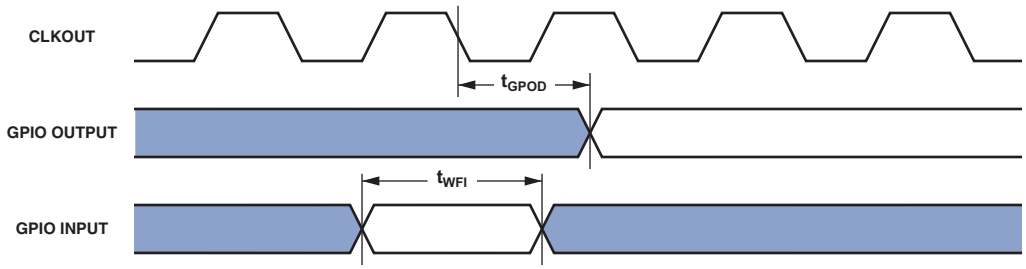


Figure 25. General-Purpose Port Timing

Pulse Width Modulator (PWM) Timing

Table 40 and Figure 29 describe PWM operations.

Table 40. PWM Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{ES}	External Sync Pulse Width	$2 \times t_{SCLK} + 1$		ns
Switching Characteristics				
t_{DODIS}	Output[1] Inactive (OFF) After Trip Input		12	ns
t_{DOE}	Output[1] Delay After External Sync[2]	$2 \times t_{SCLK}$	$5 \times t_{SCLK} + 13$	ns
t_{OD}	Output[1] Delay After Falling Edge of CLKOUT		5	ns

[1] PWM outputs are: PWMx_AH, PWMx_AL, PWMx_BH, PWMx_BL, PWMx_CH, and PWMx_CL.

[2] When the external sync signal is synchronous to the peripheral clock, it takes fewer clock cycles for the output to appear compared to when the external sync signal is asynchronous to the peripheral clock. For more information, see the *ADSP-BF50x Blackfin Processor Hardware Reference*.

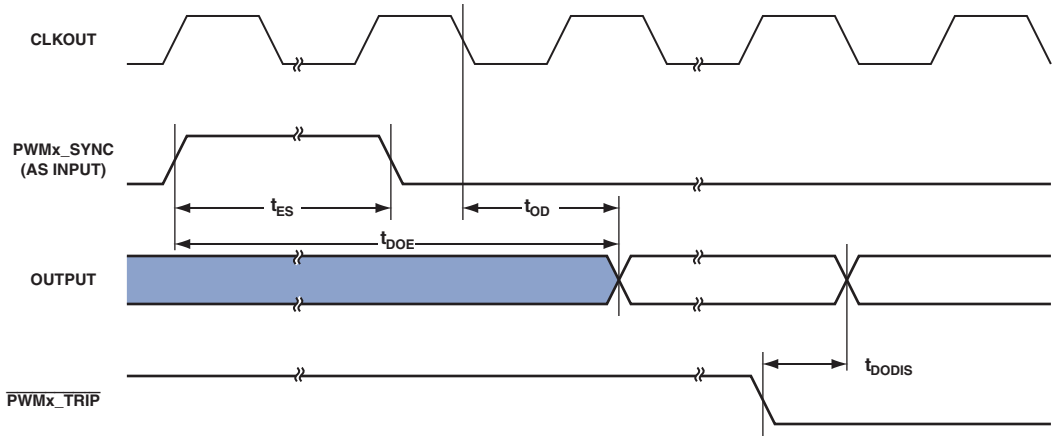


Figure 29. PWM Timing

ADC—SPECIFICATIONS

Specifications are subject to change without notice.

ADC—OPERATING CONDITIONS

Parameter	Conditions	Min	Nominal	Max	Unit
V_{DD}[1] (AV_{DD}, DV_{DD}, V_{DRIVE})	f_{ADSCLK} = 24 MHz, f_S up to 1.5 MSPS, internal or external reference = 2.5 V ± 1% unless otherwise noted	2.7		3.6	V
	f_{ADSCLK} = 25 MHz, f_S up to 1.56 MSPS, internal or external reference = 2.5 V ± 1% unless otherwise noted	3.0		3.6	V
	f_{ADSCLK} = 32 MHz, f_S up to 2.0 MSPS, internal or external reference = 2.5 V ± 1% unless otherwise noted	4.75 (AV_{DD}, DV_{DD}) 2.7 (V_{DRIVE})		5.25 (AV_{DD}, DV_{DD}) 5.25 (V_{DRIVE})	V V
T_J Junction Temperature	120-Lead LQFP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C

[1] Throughout the ADC sections of this data sheet, V_{DD} refers to both AV_{DD} and DV_{DD}.

Table 47. Operating Conditions (Analog, Voltage Reference, and Logic I/O)

Parameter	Specification	Unit	Test Conditions/Comments
ANALOG INPUT[1]			
Single-Ended Input Range	0 V to V_{REF}	V	RANGE= low
	0 V to 2 × V_{REF}	V	RANGE = high
Pseudo Differential Input Range: V_{IN+} – V_{IN-}[2]	0 V to V_{REF}	V	RANGE = low
	2 × V_{REF}	V	RANGE = high
Fully Differential Input Range: V_{IN+} and V_{IN-}	V_{CM} ± V_{REF}/2	V	V_{CM} = common-mode voltage[3] = V_{REF}/2, RANGE = low
	V_{CM} ± V_{REF}	V	V_{CM} = V_{REF}, RANGE = high
DC Leakage Current	±1	µA max	V_{A1} to V_{A6}, V_{B1} to V_{B6}
Input Capacitance[4]	45	pF typ	When in track
	10	pF typ	When in hold
INTERNAL VOLTAGE REFERENCE (OUTPUT)[5]			
Reference Output Voltage	2.5 ± 0.4%	V	@ 25°C, AV_{DD} = 2.7 V to 5.25 V
Long-Term Stability[4]	150	ppm typ	For 1000 hours
Output Voltage Thermal Hysteresis[6]	50	ppm typ	
D_{CAP}A, D_{CAP}B Output Impedance[4]	10	Ω typ	
Reference Temperature Coefficient[4]	60 max, 20 typ	ppm/°C	
V_{REF} Noise[4]	20	µV rms typ	
EXTERNAL VOLTAGE REFERENCE (INPUT)[5]			
Reference Input Voltage Range[7]	0.1 to AV_{DD}	V	See ADC—Typical Performance Characteristics
DC Leakage Current[7]	±2	µA max	
Input Capacitance[4]	25	pF typ	
DIGITAL LOGIC INPUTS			
Input High Voltage, V_{INH}	2.8	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±15	nA typ	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[4]	5	pF typ	

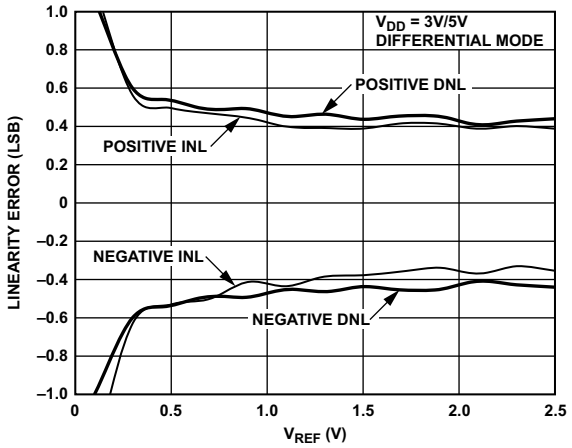


Figure 56. Linearity Error vs. V_{REF}

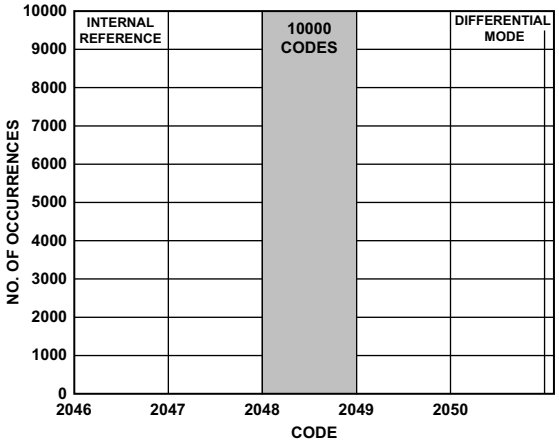


Figure 59. Histogram of Codes for 10k Samples in Differential Mode

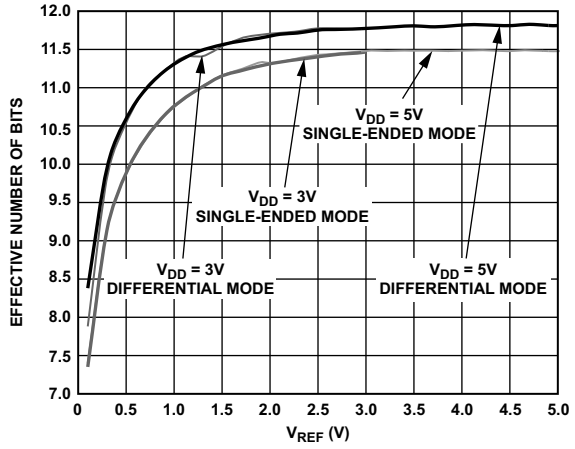


Figure 57. Effective Number of Bits vs. V_{REF}

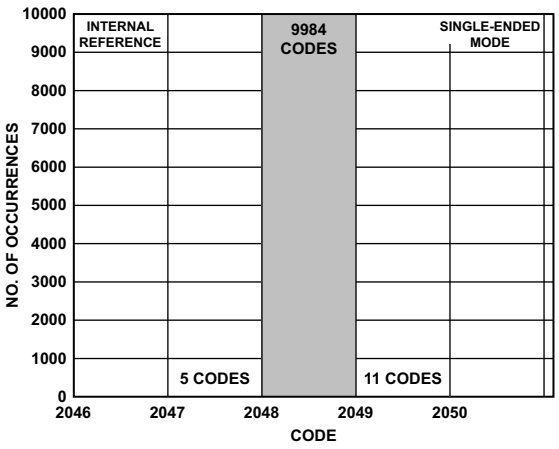


Figure 60. Histogram of Codes for 10k Samples in Single-Ended Mode

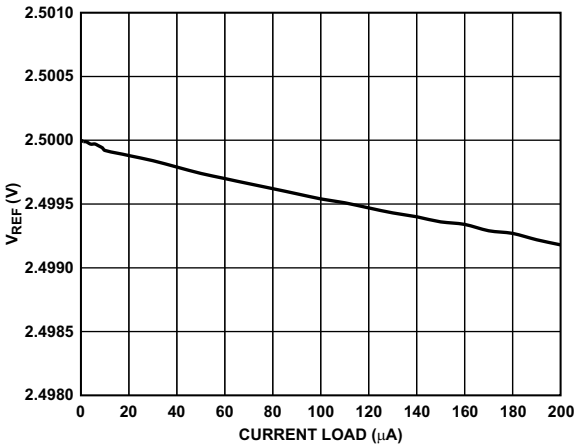


Figure 58. V_{REF} vs. Reference Output Current Drive

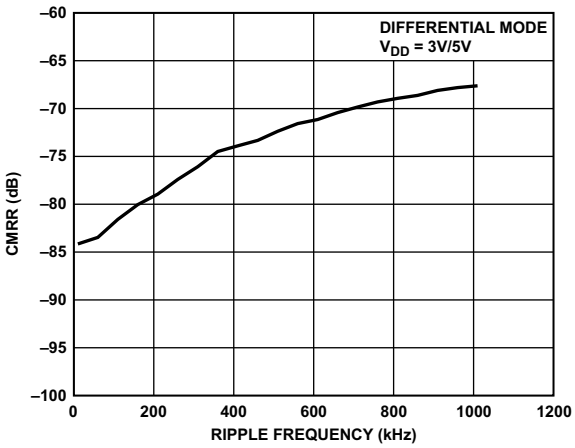


Figure 61. CMRR vs. Common-Mode Ripple Frequency

ADC—TERMINOLOGY

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale with a single (1) LSB point below the first code transition, and full scale with a 1 LSB point above the last code transition.

Offset Error
Offset error applies to straight binary output coding. It is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal (AGND + 1 LSB).

Offset Error Match
Offset error match is the difference in offset error across all 12 channels.

Gain Error
Gain error applies to straight binary output coding. It is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (V_{REF} 1 LSB) after the offset error is adjusted out. Gain error does not include reference error.

Gain Error Match
Gain error match is the difference in gain error across all 12 channels.

Positive Gain Error
This applies when using twos complement output coding with, for example, the 2 × V_{REF} input range as –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the last code transition (011…110) to (011…111) from the ideal (+V_{REF} – 1 LSB) after the zero code error is adjusted out.

Positive Gain Error Match
This is the difference in positive gain error across all 12 channels.

Zero Code Error
Zero code error applies when using twos complement output coding with, for example, the 2 × V_{REF} input range as –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the mid-scale transition (all 0s to all 1s) from the ideal V_{IN} voltage (V_{REF}).

Zero Code Error Match
Zero code error match refers to the difference in zero code error across all 12 channels.

Negative Gain Error
This applies when using twos complement output coding option, in particular the 2 × V_{REF} input range as –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the first code transition (100…000) to (100…001) from the ideal (that is, –V_{REF} + 1 LSB) after the zero code error is adjusted out.

Negative Gain Error Match
This is the difference in negative gain error across all 12 channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode after the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal-to-(Noise + Distortion) Ratio (SINAD)
This ratio is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitalization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02N + 1.76)\ dB$$

Therefore, for a 12-bit converter, theoretical SINAD is 74 dB.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the ADC, it is defined as:

$$THD(dB) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.

V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Effective Number of Bits (ENOB)
This is a figure of merit which characterizes the dynamic performance of the ADC at a specified input frequency and sampling rate. ENOB is expressed in bits. For a full scale sinusoidal input, ENOB is defined as:

$$ENOB = (SINAD - 1.76)/6.02$$

Peak Harmonic or Spurious Noise (SFDR)
Peak harmonic, or spurious noise, is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale (2 × V_{REF} when V_{DD} = 5 V, V_{REF} when V_{DD} = 3 V), 10 kHz sine wave signal to all un-selected input channels and

When the ADC starts a conversion (see Figure 63 (ADC Conversion Phase)), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} pins must be matched; otherwise, the two inputs will have different settling times, resulting in errors.

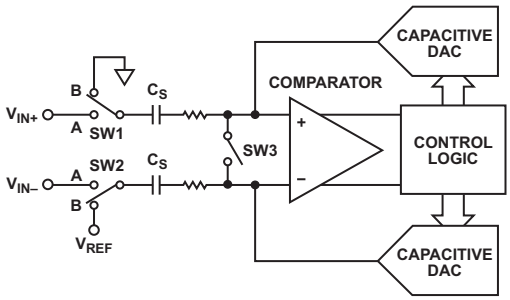


Figure 63. ADC Conversion Phase

Analog Input Structure

Figure 64 (Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed) shows the equivalent circuit of the analog input structure of the ADC in differential/pseudo differential mode. In single-ended mode, V_{IN} is internally tied to AGND. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and starts conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

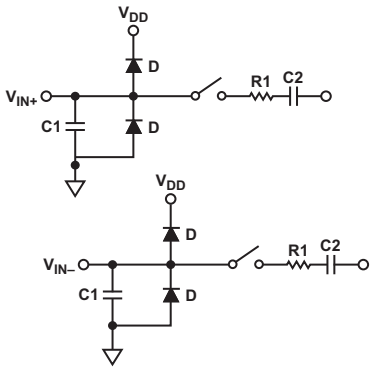


Figure 64. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed

The C1 capacitors in Figure 64 (Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed) are typically 4 pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the ADC's sampling capacitors with a capacitance of 45 pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins with optimum values of 47 Ω and 10 pF. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated.

The THD increases as the source impedance increases and performance degrades. Figure 65 (THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode shows a graph of the THD vs. the analog input signal frequency for different source impedances in single-ended mode, while Figure 66 (THD vs. Analog Input Frequency for Various Source Impedances, Differential Mode) shows the THD vs. the analog input signal frequency for different source impedances in differential mode.

Figure 67 (THD vs. Analog Input Frequency for Various Supply Voltages) shows a graph of the THD vs. the analog input frequency for various supplies while sampling at 2 MSPS. In this case, the source impedance is 47 Ω.

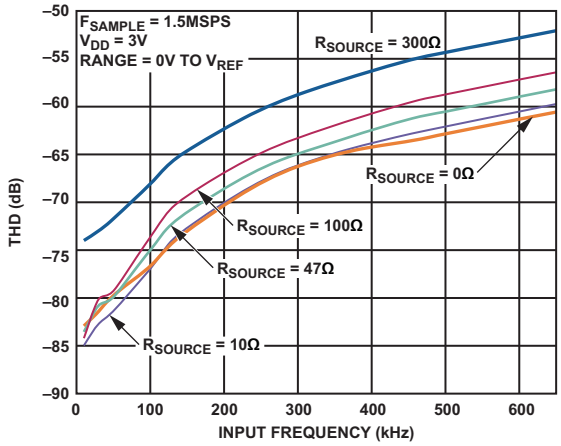


Figure 65. THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode

down for a relatively long duration between these bursts of several conversions. When the ADC is in partial power-down, all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter partial power-down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of ADSCLK and before the 10th falling edge of ADSCLK, as shown in Figure 81 (Entering Partial Power-Down Mode). Once $\overline{CS}$ is brought high in this window of ADSCLKs, the part enters partial power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is brought high before the second ADSCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the $\overline{CS}$ line.

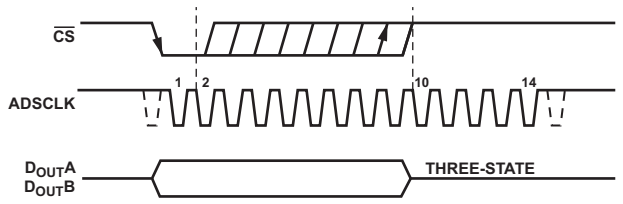


Figure 81. Entering Partial Power-Down Mode

To exit this mode of operation and power up the ADC again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th ADSCLK. The device is fully powered up after approximately 1 µs has elapsed, and valid data results from the next conversion, as shown in Figure 82 (Exiting Partial Power-Down Mode). If $\overline{CS}$ is brought high before the second falling edge of ADSCLK, the ADC again goes into partial power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line. Although the device may begin to power up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$. If the ADC is already in partial power-down mode and $\overline{CS}$ is brought high between the second and 10th falling edges of ADSCLK, the device enters full power-down mode.

Full Power-Down Mode

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required, as power-up from a full power-down takes substantially longer than that from partial power-down. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus power-down. When the ADC is in full power-down, all analog circuitry is powered down. Full power-down is entered in a similar way as partial power-down, except the timing sequence shown in Figure 81 (Entering Partial Power-Down Mode) must be executed twice. The conversion process must be interrupted in a similar fashion by bringing $\overline{CS}$ high anywhere after the second falling edge of ADSCLK and before the 10th falling edge of ADSCLK. The device enters partial power-down at this point. To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure 83 (Entering Full Power-Down Mode). Once $\overline{CS}$ is brought high in this window of ADSCLKs, the part completely powers down.

Note that it is not necessary to complete the 14 ADSCLKs once $\overline{CS}$ is brought high to enter a power-down mode.

To exit full power-down and power up the ADC, a dummy conversion is performed, as when powering up from partial power-down. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up, as long as $\overline{CS}$ is held low until after the falling edge of the 10th ADSCLK. The required power-up time must elapse before a conversion can be initiated, as shown in Figure 84 (Exiting Full Power-Down Mode). See the Power-Up Times section for the power-up times associated with the ADC.

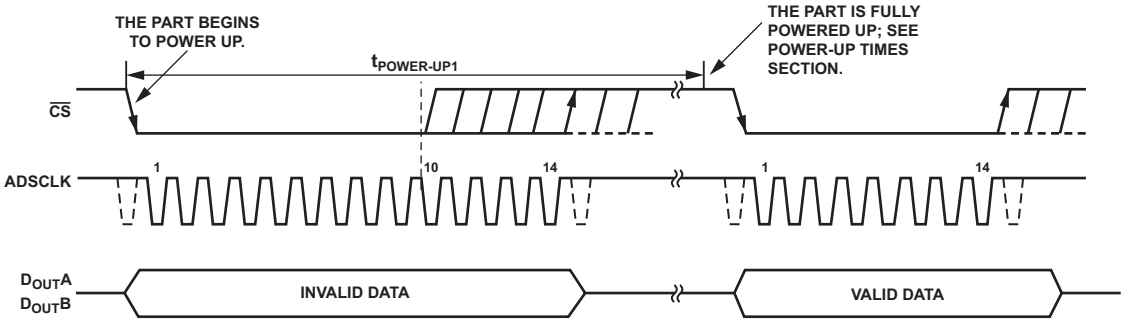


Figure 82. Exiting Partial Power-Down Mode

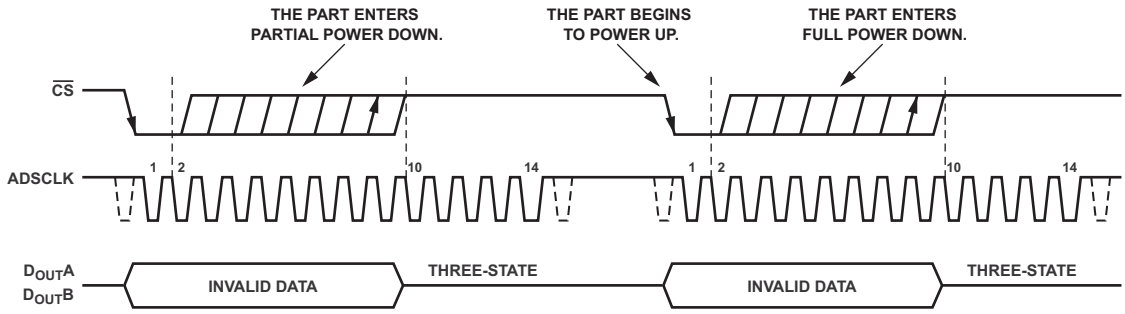


Figure 83. Entering Full Power-Down Mode

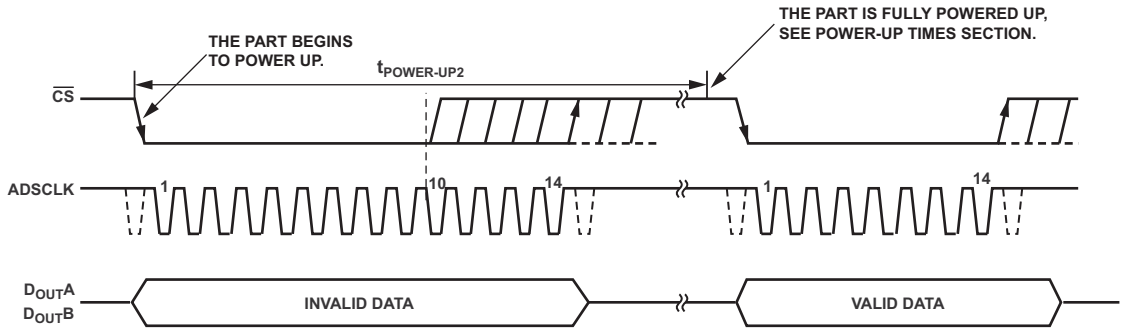


Figure 84. Exiting Full Power-Down Mode

Power-Up Times

As described in detail, the ADC has two power-down modes, partial power-down and full power-down. This section deals with the power-up time required when coming out of either of these modes. It should be noted that the power-up times, as explained in this section, apply with the recommended capacitors in place on the $D_{CAP}A$ and $D_{CAP}B$ pins.

To power up from full power-down, approximately 1.5 ms should be allowed from the falling edge of $\overline{CS}$, shown as $t_{POWER-UP2}$ in Figure 84 (Exiting Full Power-Down Mode). Powering up from partial power-down requires much less time. The power-up time from partial power-down is typically 1 µs; however, if using the internal reference, then the ADC must be in partial power-down for at least 67 µs in order for this power-up time to apply.

When power supplies are first applied to the ADC, the ADC may power up in either of the power-down modes or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the partial power-down mode immediately after the supplies are applied, then two dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th ADSCLK falling edge (see Figure 80 (Normal Mode Operation)); in the second cycle, $\overline{CS}$ must be brought high before the 10th ADSCLK edge but after the second ADSCLK falling edge (see Figure 81 (Entering Partial Power-Down Mode)). Alternatively, if it is intended to place the part in full power-down mode when the supplies are applied, then three dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th ADSCLK falling edge (see Figure 80 (Normal Mode Operation)); the second and third dummy cycles place the part in full power-down (see Figure 83 (Entering Full Power-Down Mode)).

Once supplies are applied to the ADC, enough time must be allowed for any external reference to power up and charge the various reference buffer decoupling capacitors to their final values.

Power vs. Throughput Rate

The power consumption of the ADC varies with the throughput rate. When using very slow throughput rates and as fast an ADSCLK frequency as possible, the various power-down options can be used to make significant power savings. However, the ADC quiescent current is low enough that even without using the power-down options, there is a noticeable variation in power consumption with sampling rate. This is true whether a fixed ADSCLK value is used or if it is scaled with the sampling rate. Figure 85 (Power vs. Throughput in Normal Mode with VDD = 3 V) and Figure 86 (Power vs. Throughput in Normal Mode with VDD = 5 V) show plots of power vs. the throughput rate when operating in normal mode for a fixed

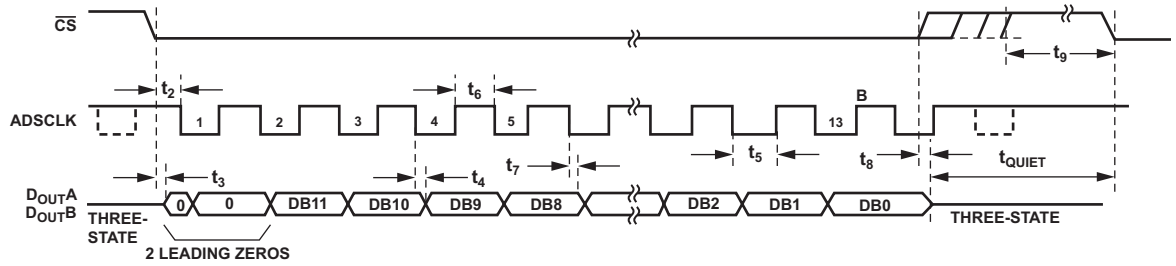


Figure 87. Serial Interface Timing Diagram

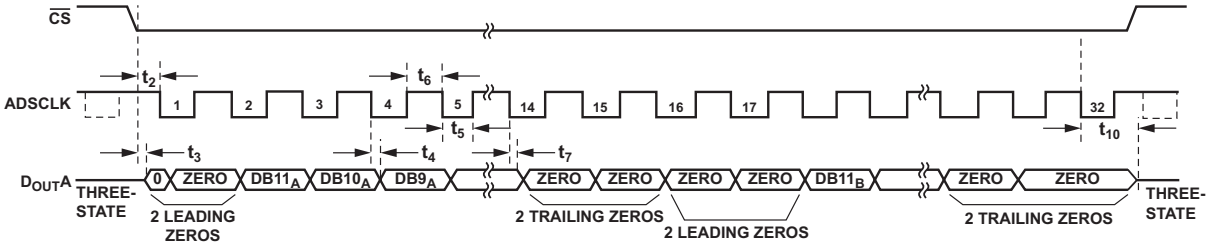


Figure 88. Reading Data from Both ADCs on One D_{OUT} Line with 32 ADSCLKs

Table 55. 120-Lead LQFP Lead Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	V_{DDEXT}	31	PG3	61	V_{DDINT}	91	V_{B2}
2	PF2	32	PG4	62	V_{DDEXT}	92	V_{B1}
3	PF4	33	TDI	63	$V_{DDFLASH}$	93	AGND
4	PF3	34	TCK	64	V_{DDEXT}	94	$D_{CAP}B$
5	PF5	35	TMS	65	V_{DDINT}	95	RANGE
6	V_{DDEXT}	36	TDO	66	V_{DDEXT}	96	SGL/$\overline{DIFF}$
7	PF6	37	$\overline{TRST}$	67	V_{DDEXT}	97	A2
8	PF7	38	PG5	68	$\overline{EMU}$	98	A1
9	PF8	39	PG6	69	$V_{DDFLASH}$	99	AGND
10	PF9	40	PG7	70	EXT_WAKE	100	A0
11	$\overline{NMI}$	41	V_{DDEXT}	71	$\overline{PG}$	101	$\overline{CS}$
12	$\overline{RESET}$	42	V_{DDINT}	72	NC	102	ADSCLK
13	GND	43	PG8	73	AGND	103	$D_{OUT}B$
14	PF10	44	PG9	74	DGND	104	DGND
15	V_{DDEXT}	45	PG10	75	REF_SELECT	105	$D_{OUT}A$
16	PF11	46	PG11	76	AV_{DD}	106	V_{DRIVE}
17	GND	47	PG12	77	$D_{CAP}A$	107	DV_{DD}
18	PF12	48	PG13	78	AGND	108	GND
19	PF13	49	PG14	79	AGND	109	GND
20	V_{DDEXT}	50	PG15	80	V_{A1}	110	CLKIN
21	PF14	51	V_{DDEXT}	81	V_{A2}	111	XTAL
22	PF15	52	V_{DDINT}	82	AGND	112	V_{DDEXT}
23	V_{DDEXT}	53	V_{DDINT}	83	V_{A3}	113	PH0
24	V_{DDINT}	54	SDA	84	V_{A4}	114	PH2
25	$V_{DDFLASH}$	55	SCL	85	V_{A5}	115	PH1
26	V_{DDEXT}	56	BMODE2	86	V_{A6}	116	V_{DDEXT}
27	PG0	57	BMODE1	87	V_{B6}	117	V_{DDINT}
28	PG1	58	BMODE0	88	V_{B5}	118	PF0
29	PG2	59	V_{DDEXT}	89	V_{B4}	119	PF1
30	V_{DDEXT}	60	NC	90	V_{B3}	120	EXTCLK
						121*	GND
						122**	AGND

* Pin no. 121 is the GND supply (see Figure 89 and Figure 90) for the processor (4.6mm × 6.17mm); this pad **must** connect to GND.
** Pin no. 122 is the AGND supply (see Figure 89 and Figure 90) for the ADC (2.81mm × 2.81mm); this pad **must** connect to AGND.

88-LEAD LFCSP LEAD ASSIGNMENT

Table 56 lists the LFCSP leads by signal mnemonic. Table 57 on Page 77 lists the LFCSP by lead number.

Table 56. 88-Lead LFCSP Lead Assignment (Alphabetical by Signal)

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
BMODE0	51	PF4	82	PG9	34	V_{DDEXT}	20
BMODE1	50	PF5	83	PG10	35	V_{DDEXT}	31
BMODE2	49	PF6	85	PG11	36	V_{DDEXT}	41
CLKIN	68	PF7	86	PG12	37	V_{DDEXT}	52
$\overline{EMU}$	60	PF8	87	PG13	38	V_{DDEXT}	54
EXT_WAKE	62	PF9	88	PG14	39	V_{DDEXT}	56
EXTCLK	78	PF10	4	PG15	40	V_{DDEXT}	58
GND	3	PF11	6	PH0	71	V_{DDEXT}	59
GND	7	PF12	8	PH1	72	V_{DDEXT}	70
GND	67	PF13	9	PH2	73	V_{DDEXT}	74
NC	45	PF14	11	$\overline{RESET}$	2	V_{DDEXT}	79
NC	46	PF15	12	SCL	44	V_{DDEXT}	84
NC	47	$\overline{PG}$	63	SDA	43	$V_{DDFLASH}$	15
NC	48	PG0	17	TCK	24	$V_{DDFLASH}$	55
NC	64	PG1	18	TDI	23	$V_{DDFLASH}$	61
NC	65	PG2	19	TDO	27	V_{DDINT}	14
NC	66	PG3	21	TMS	25	V_{DDINT}	32
$\overline{NMI}$	1	PG4	22	$\overline{TRST}$	26	V_{DDINT}	42
PF0	76	PG5	28	V_{DDEXT}	5	V_{DDINT}	53
PF1	77	PG6	29	V_{DDEXT}	10	V_{DDINT}	57
PF2	80	PG7	30	V_{DDEXT}	13	V_{DDINT}	75
PF3	81	PG8	33	V_{DDEXT}	16	XTAL	69
						GND	89*

* Pin no. 89 is the GND supply (see Figure 92) for the processor; this pad **must** connect to GND.