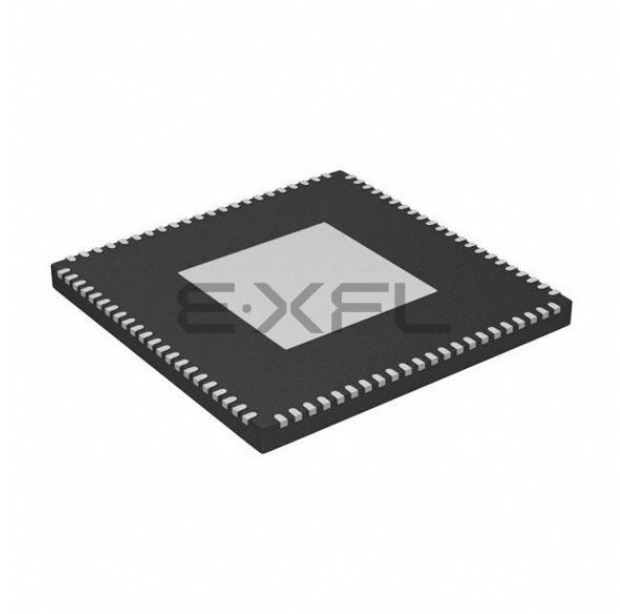

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, EBI/EMI, I²C, IrDA, PPI, SPI, SPORT, UART/USART
Clock Rate	300MHz
Non-Volatile Memory	FLASH (16MB)
On-Chip RAM	68kB
Voltage - I/O	3.30V
Voltage - Core	1.31V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP-VQ (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf504kcpz-3f

GENERAL DESCRIPTION

The ADSP-BF50x processors are members of the Blackfin® family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF50x processors are completely code compatible with other Blackfin processors. ADSP-BF50x processors offer performance up to 400 MHz and reduced static power consumption. Differences with respect to peripheral combinations are shown in Table 1.

Table 1. Processor Comparison

Feature		ADSP-BF504	ADSP-BF504F	ADSP-BF506F
Up/Down/Rotary Counters		2	2	2
Timer/Counters with PWM		8	8	8
3-Phase PWM Units		2	2	2
SPORTs		2	2	2
SPIs		2	2	2
UARTs		2	2	2
Parallel Peripheral Interface		1	1	1
Removable Storage Interface		1	1	1
CAN		1	1	1
TWI		1	1	1
Internal 32M Bit Flash		–	1	1
ADC Control Module (ACM)		1	1	1
Internal ADC		–	–	1
GPIOs		35	35	35
Memory (bytes)	L1 Instruction SRAM	16K	16K	16K
	L1 Instruction SRAM/Cache	16K	16K	16K
	L1 Data SRAM	16K	16K	16K
	L1 Data SRAM/Cache	16K	16K	16K
	L1 Scratchpad	4K	4K	4K
	L3 Boot ROM	4K	4K	4K
Maximum Speed Grade[1]		400 MHz		
Maximum System Clock Speed		100 MHz		
Package Options		88-Lead LFCSP	88-Lead LFCSP	120-Lead LQFP

[1] For valid clock combinations, see Table 14, Table 15, Table 16, and Table 24.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW-POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which provides the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF50x processors are highly integrated system-on-a-chip solutions for the next generation of embedded industrial, instrumentation, and power/motion control applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include a watchdog timer; two 32-bit up/down counters with rotary support; eight 32-bit timers/counters with PWM support; six pairs of 3-phase 16-bit center-based PWM units; two dual-channel, full-duplex synchronous serial ports (SPORTs); two serial peripheral interface (SPI) compatible ports; two UARTs with IrDA® support; a parallel peripheral interface (PPI); a removable storage interface (RSI) controller; an internal ADC with 12 channels, 12 bits, up to 2 MSPS, and ACM controller; a controller area network (CAN) controller; a 2-wire interface (TWI) controller; and an internal 32M bit flash.

PROCESSOR PERIPHERALS

The ADSP-BF50x processors contain a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). These Blackfin processors contain high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The SPORT, SPI, UART, PPI, and RSI peripherals are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including boot ROM and internal 32M bit synchronous burst flash. Multiple on-chip buses running at up to 100 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF50x processors include an interface to an off-chip voltage regulator in support of the processor's dynamic power management capability.

- DMA operations with single-cycle overhead—Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts—Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability—Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF50x processors have two SPI-compatible ports that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins MOSI (Master Output-Slave Input) and MISO (Master Input-Slave Output) and a clock pin, serial clock (SCK). An SPI chip select input pin ($\overline{\text{SPIx\_SS}}$) lets other SPI devices select the processor, and three SPI chip select output pins ($\overline{\text{SPIx\_SEL3–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS (UARTS)

The ADSP-BF50x Blackfin processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports. Each UART port provides a simplified UART interface to other peripherals or hosts, enabling full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits; one or two stop bits; and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O). The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access). The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates. Flexible interrupt timing options are available on the transmit side.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16^{(1-EDBO)} \times UART\_Divisor}$$

Where the 16-bit UART divisor comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant eight bits), and the EDBO is a bit in the UARTx_GCTL register.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The UARTs feature a pair of $\overline{\text{UAx\_RTS}}$ (request to send) and $\overline{\text{UAx\_CTS}}$ (clear to send) signals for hardware flow purposes. The transmitter hardware is automatically prevented from sending further data when the $\overline{\text{UAx\_CTS}}$ input is de-asserted. The receiver can automatically de-assert its $\overline{\text{UAx\_RTS}}$ output when the enhanced receive FIFO exceeds a certain high-water level. The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

- Boot from serial SPI memory, EEPROM or flash (BMODE = 0x3)—8-, 16-, 24-, or 32-bit addressable devices are supported. The processor uses the PF13 GPIO pin to select a single SPI EEPROM/flash device (connected to the SPI0 interface) and submits a read command and successive address bytes (0x00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected. Pull-up resistors are required on the SPI0_SEL1 and MISO pins. By default, a value of 0x85 is written to the SPI_BAUD register.
- Boot from SPI host device (BMODE = 0x4)—The processor operates in SPI slave mode and is configured to receive the bytes of the LDR file from an SPI host (master) agent. The HWAIT signal must be interrogated by the host before every transmitted byte. A pull-up resistor is required on the SPI0_SS input. A pull-down on the serial clock (SCK) may improve signal quality and booting robustness.
- Boot from PPI host device (BMODE = 0x5)—The processor operates in PPI slave mode and is configured to receive the bytes of the LDR file from a PPI host (master) agent.
- Boot from UART0 host on Port G (BMODE = 0x7)—Using an autobaud handshake sequence, a boot-stream formatted program is downloaded by the host. The host selects a bit rate within the UART clocking capabilities.

  When performing the autobaud detection, the UART expects an "@" (0x40) character (eight bits data, one start bit, one stop bit, no parity bit) on the UA0_RX pin to determine the bit rate. The UART then replies with an acknowledgement composed of 4 bytes (0xBF, the value of UART0_DLL, the value of UART0_DLH, then 0x00). The host can then download the boot stream. The processor deasserts the UA0_RTS output to hold off the host; UA0_CTS functionality is not enabled at boot time.

For each of the boot modes, a 16 byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the address stored in the EVT1 register.

The boot kernel differentiates between a regular hardware reset and a wakeup-from-hibernate event to speed up booting in the later case. Bits 6-4 in the system reset configuration (SYSCR) register can be used to bypass the pre-boot routine and/or boot kernel in case of a software reset. They can also be used to simulate a wakeup-from-hibernate boot in the software reset case.

The boot process can be further customized by "initialization code." This is a piece of code that is loaded and executed prior to the regular application boot. Typically, this is used to speed up booting by managing the PLL, clock frequencies, wait states, or serial bit rates.

The boot ROM also features C-callable functions that can be called by the user application at run time. This enables second-stage boot or boot management schemes to be implemented with ease.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADC AND ACM INTERFACE

This section describes the ADC and ACM interface. System designers should also consult the *ADSP-BF50x Blackfin Processor Hardware Reference* for additional information.

The ADC control module (ACM) provides an interface that synchronizes the controls between the processor and the internal analog-to-digital converter (ADC) module. The ACM is available on the ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors, and the ADC is available on the ADSP-BF506F processor only. The analog-to-digital conversions are initiated by the processor, based on external or internal events.

The ACM allows for flexible scheduling of sampling instants and provides precise sampling signals to the ADC.

Table 12. ADC—Signal Descriptions (ADSP-BF506F Processor Only) (Continued)

Signal Name	Type	Function
$D_{OUT}A$, $D_{OUT}B$	O	Serial Data Outputs. The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the ADSCLK input and 14 ADSCLKs are required to access the data. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data stream consists of two leading zeros followed by the 12 bits of conversion data. The data is provided MSB first. If $\overline{CS}$ is held low for 16 ADSCLK cycles rather than 14, then two trailing zeros will appear after the 12 bits of data. If $\overline{CS}$ is held low for a further 16 ADSCLK cycles on either $D_{OUT}A$ or $D_{OUT}B$, the data from the other ADC follows on the D_{OUT} pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either $D_{OUT}A$ or $D_{OUT}B$ using only one serial port. For more information, see the ADC—Serial Interface section.
V_{DRIVE}	P	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the digital I/O interface operates. This pin should be decoupled to DGND. The voltage at this pin may be different than that at AV_{DD} and DV_{DD} but should never exceed either by more than 0.3 V.
DV_{DD}	P	Digital Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for all digital circuitry on the internal ADC. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND.

SPECIFICATIONS

Specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage	Industrial Models	1.14		1.47	V
	Internal Supply Voltage	Commercial Models	1.10		1.47	V
	Internal Supply Voltage	Automotive Models	1.33		1.47	V
V_{DDEXT}[1, 2]	External Supply Voltage	1.8 V I/O, ADSP-BF504, Nonautomotive and Non Flash Models	1.7	1.8	1.9	V
	External Supply Voltage	2.5 V I/O, ADSP-BF504, Nonautomotive and Non Flash Models	2.25	2.5	2.75	V
	External Supply Voltage	3.3 V I/O, ADSP-BF50x, All Models	2.7	3.3	3.6	V
$V_{DDFLASH}$[1, 3]	Flash Memory Supply Voltage		1.7	1.8	2.0	V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = 1.90 V	1.2			V
	High Level Input Voltage[4, 6]	V_{DDEXT} = 2.75 V	1.7			V
	High Level Input Voltage[4, 6]	V_{DDEXT} = 3.6 V	2.0			V
V_{IHTWI}	High Level Input Voltage[5]	V_{DDEXT} = 1.90 V/2.75 V/3.6 V	0.7 × V_{BUSTWI}[7, 8]		V_{BUSTWI}[7, 8]	V
V_{IL}	Low Level Input Voltage[4, 5]	V_{DDEXT} = 1.7 V			0.6	V
	Low Level Input Voltage[4, 6]	V_{DDEXT} = 2.25 V			0.7	V
	Low Level Input Voltage[4, 6]	V_{DDEXT} = 3.0 V			0.8	V
V_{ILTWI}	Low Level Input Voltage[5]	V_{DDEXT} = minimum			0.3 × V_{BUSTWI}[8]	V
T_J	Junction Temperature	88-Lead LFCSP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
	Junction Temperature	88-Lead LFCSP @ $T_{AMBIENT}$ = 0°C to +70°C	0		+90	°C
	Junction Temperature	120-Lead LQFP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
	Junction Temperature	120-Lead LQFP @ $T_{AMBIENT}$ = 0°C to +70°C	0		+90	°C
	Junction Temperature	88-Lead LFCSP @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] Must remain powered (even if the associated function is not used).
[2] 1.8 V and 2.5 V I/O are supported only on ADSP-BF504 nonautomotive models. All ADSP-BF50x flash and automotive models support 3.3 V I/O only.
[3] For ADSP-BF504, $V_{DDFLASH}$ pins should be connected to GND.
[4] Parameter value applies to all input and bidirectional pins, except SDA and SCL.
[5] Bidirectional pins (PF15–0, PG15–0, PH15–0) and input pins (TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF50x processors are 2.5 V tolerant (always accept up to 2.7 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.
[6] Bidirectional pins (PF15–0, PG15–0, PH2–0) and input pins (TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF50x processors are 3.3 V tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.
[7] The V_{IHTWI} min and max value vary with the selection in the TWI_DT field of the NONGPIO_DRIVE register. See V_{BUSTWI} min and max values in Table 13.
[8] SDA and SCL are pulled up to V_{BUSTWI}. See Table 13.

Table 13 shows settings for TWI_DT in the NONGPIO_DRIVE register. Set this register prior to using the TWI port.

Table 13. TWI_DT Field Selections and V_{DDEXT}/V_{BUSTWI}

TWI_DT	V_{DDEXT} Nominal	V_{BUSTWI} Minimum	V_{BUSTWI} Nominal	V_{BUSTWI} Maximum	Unit
000 (default)	3.3	2.97	3.3	3.63	V
001	1.8	1.7	1.8	1.98	V
010	2.5	2.97	3.3	3.63	V
011	1.8	2.97	3.3	3.63	V
100	3.3	4.5	5	5.5	V
101	1.8	2.25	2.5	2.75	V
110	2.5	2.25	2.5	2.75	V
111 (reserved)	—	—	—	—	—

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 9 and Table 23 provides details about the package branding for the ADSP-BF50x processors.

Figure 9. Product Information on Package

Table 23. Package Brand Information[1]

Brand Key	Field Description
ADSP-BF50x	Product Name[2]
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliance Designator
yyww	Date Code

[1] Nonautomotive only. For branding information specific to Automotive products, contact Analog Devices Inc.
[2] See product names in the Ordering Guide on Page 81.

Table 25. Clock Out Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Switching Characteristics						
t_{SCLK}	CLKOUT[1] Period[2,3]	10		10		ns
t_{SCLKH}	CLKOUT[1] Width High	4		4		ns
t_{SCLKL}	CLKOUT[1] Width Low	4		4		ns

[1] The ADSP-BF504/ADSP-BF504F/ADSP-BF506F processor does not have a dedicated CLKOUT pin. Rather, the EXTCLK pin may be programmed to serve as CLKBUF or CLKOUT. This parameter applies when EXTCLK is programmed to output CLKOUT.

[2] The t_{SCLK} value is the inverse of the f_{SCLK} specification. Reduced supply voltages affect the best-case value of 10 ns listed here.

[3] The t_{SCLK} value does not account for the effects of jitter.

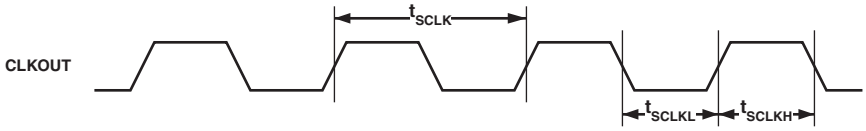
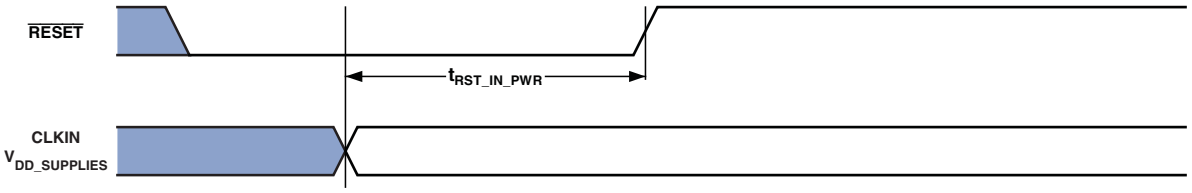


Figure 11. Clock Out Timing

Table 26. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{RESET}$ Deasserted after the V_{DDINT}, V_{DDEXT}, $V_{DDFLASH}$, and CLKIN Pins are Stable and Within Specification	3500 × t_{CKIN}		ns



In Figure 12, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, and $V_{DDFLASH}$.

Figure 12. Power-Up Reset Timing

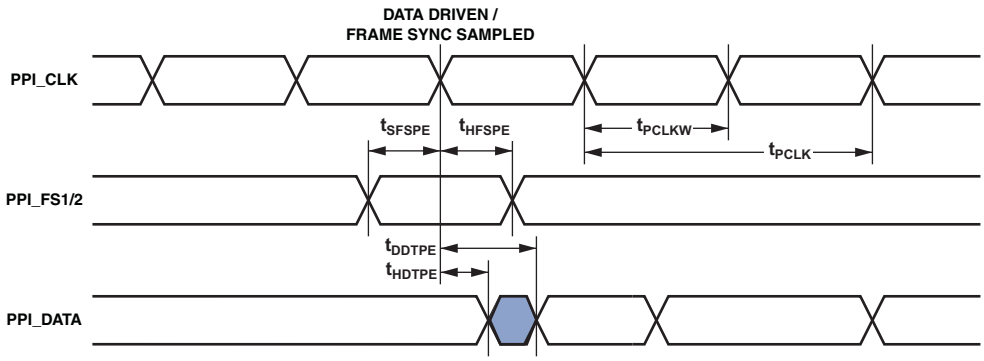


Figure 15. PPI GP Tx Mode with External Frame Sync Timing

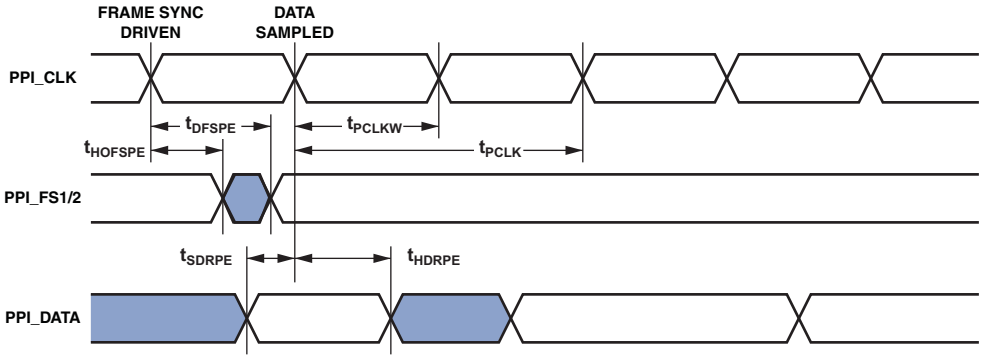


Figure 16. PPI GP Rx Mode with Internal Frame Sync Timing

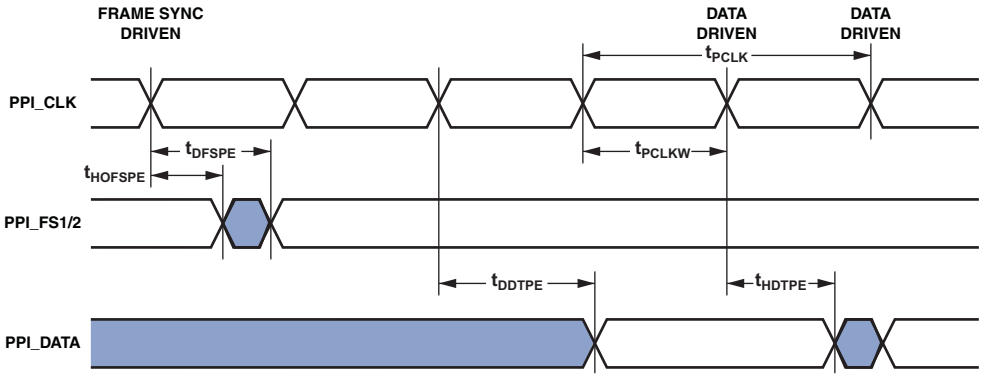


Figure 17. PPI GP Tx Mode with Internal Frame Sync Timing

RSI Controller Timing

Table 28 and Figure 18 describe RSI Controller Timing.
Table 29 and Figure 19 describe RSI controller (high speed) timing.

Table 28. RSI Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	5.75		ns
t_{IH}	Input Hold Time	2		ns
Switching Characteristics				
f_{PP}[1]	Clock Frequency Data Transfer Mode	0	25	MHz
f_{OD}	Clock Frequency Identification Mode	100[2]	400	kHz
t_{WL}	Clock Low Time	10		ns
t_{WH}	Clock High Time	10		ns
t_{TLH}	Clock Rise Time		10	ns
t_{THL}	Clock Fall Time		10	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		14	ns
t_{ODLY}	Output Delay Time During Identification Mode		50	ns

[1] $t_{PP} = 1/f_{PP}$.
[2] Specification can be 0 kHz, which means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

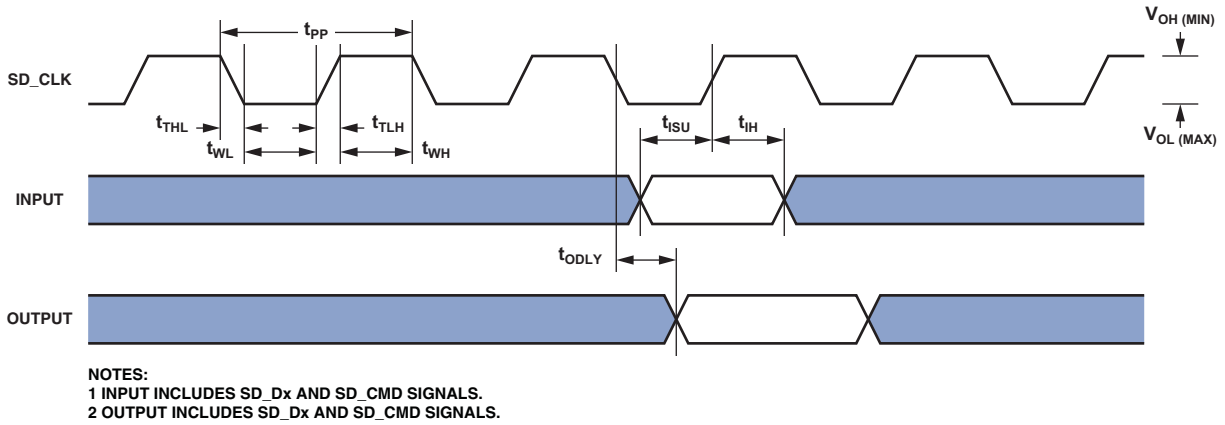


Figure 18. RSI Controller Timing

Serial Peripheral Interface (SPI) Port—Master Timing

Table 34 and Figure 23 describe SPI port master operations.

Table 34. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	11.6		9.6		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPISELx}$ low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 2.0$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)	0	6	0	6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0		–1.0		ns

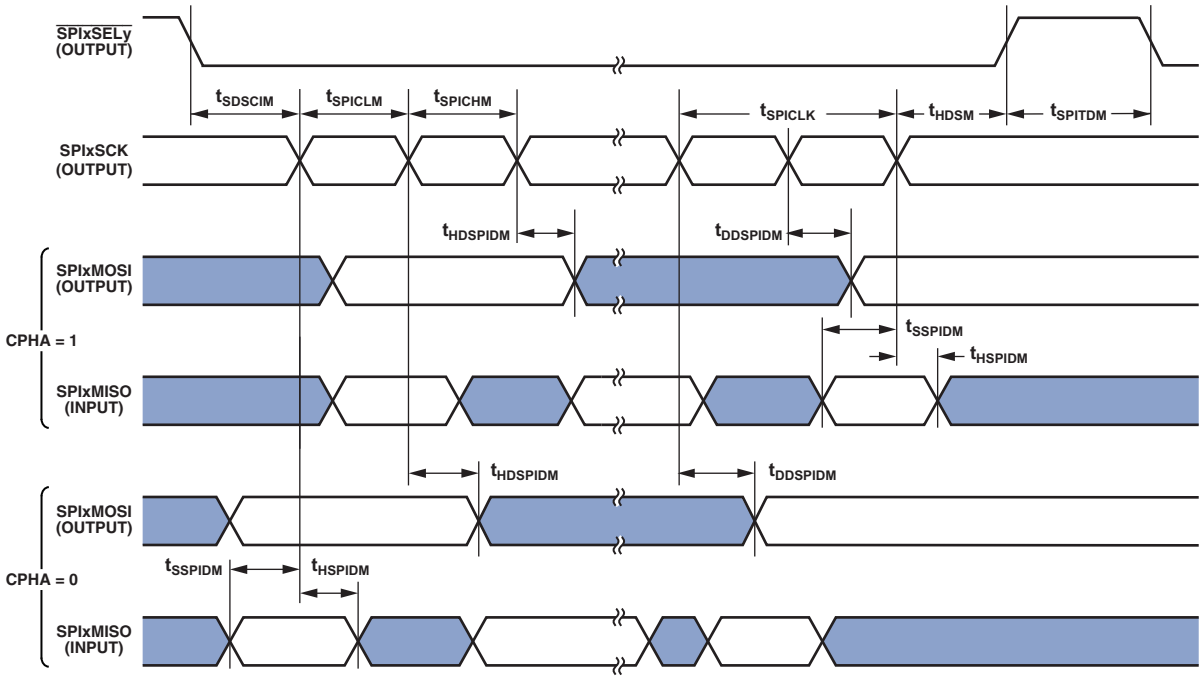


Figure 23. Serial Peripheral Interface (SPI) Port—Master Timing

ADC Controller Module (ACM) Timing

Table 41 and Figure 30 describe ACM operations.

Note that the ACM clock (ACLK) frequency in MHz is set by the following equation (in which ACMCKDIV ranges from 0 to 255).

$$t_{ACLK} = \frac{1}{f_{ACLK}}$$

$$f_{ACLK} = \frac{f_{SCLK}}{(2 \times ACMCKDIV) + 2}$$

Table 41. ACM Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SDR}	SPORT DRxPRI/DRxSEC Setup Before ACLK	8.0		7.0		ns
t_{HDR}	SPORT DRxPRI/DRxSEC Hold After ACLK	0		0		ns
Switching Characteristics						
t_{DO}	ACM Controls (ACM_A[2:0], ACM_RANGE, ACM_SGLDIFF) Delay After Falling Edge of CLKOUT		8.4		8.4	ns
t_{DACLK}	ACLK Delay After Falling Edge of CLKOUT		4.5		4.5	ns
t_{DCS}	$\overline{CS}$ Active Edge Delay After Falling Edge of CLKOUT		5.6		5.3	ns
$t_{DCSACLK}$	The Delay Between the Active Edge of $\overline{CS}$ and the First Edge of ACLK	t_{ACLK} – 5		t_{ACLK} – 5		ns

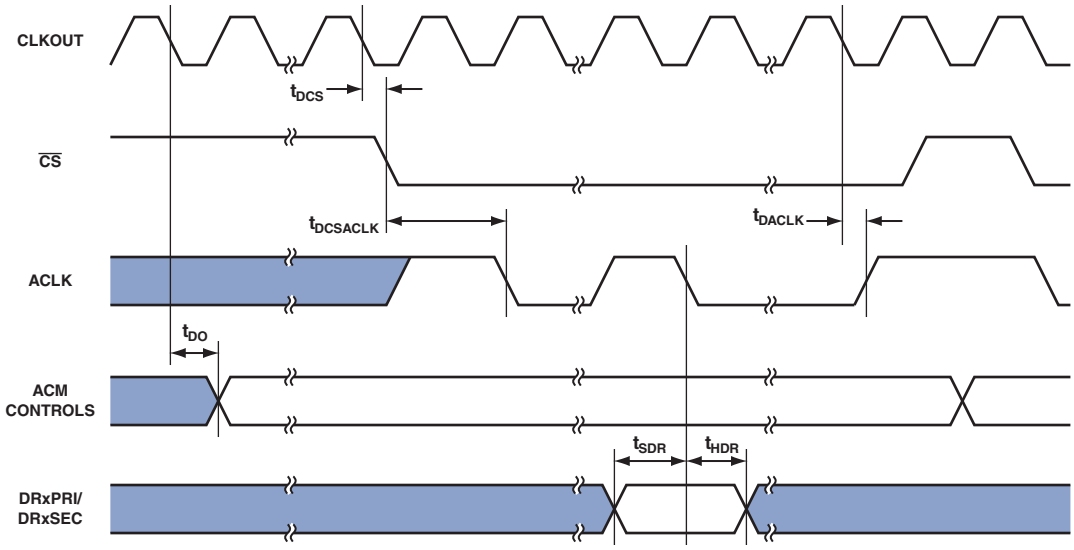


Figure 30. ACM Timing

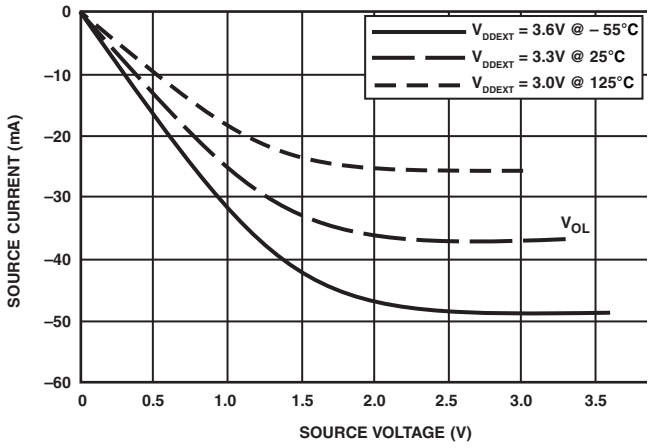


Figure 38. Driver Type D Current (3.3 V V_{DDEXT})

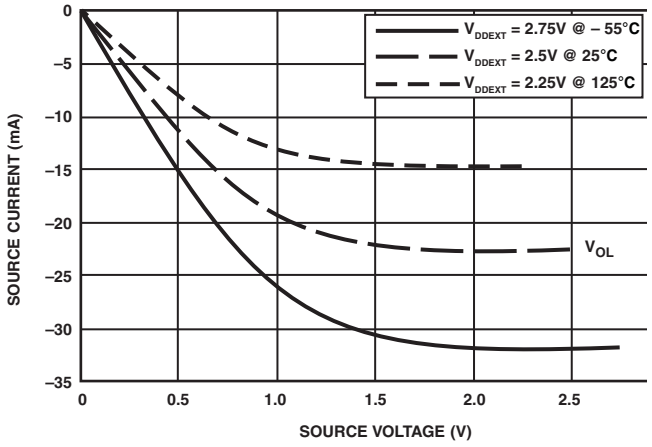


Figure 39. Driver Type D Current (2.5 V V_{DDEXT})

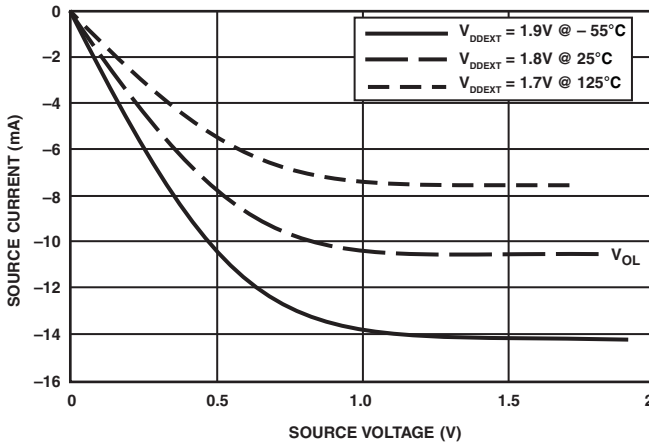


Figure 40. Driver Type D Current (1.8 V V_{DDEXT})

PROCESSOR—TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 41 shows the measurement point for AC measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DDEXT}/2$ for V_{DDEXT} (nominal) = 1.8 V/2.5 V/3.3 V.

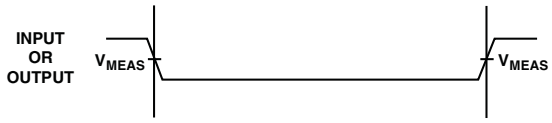


Figure 41. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 42.

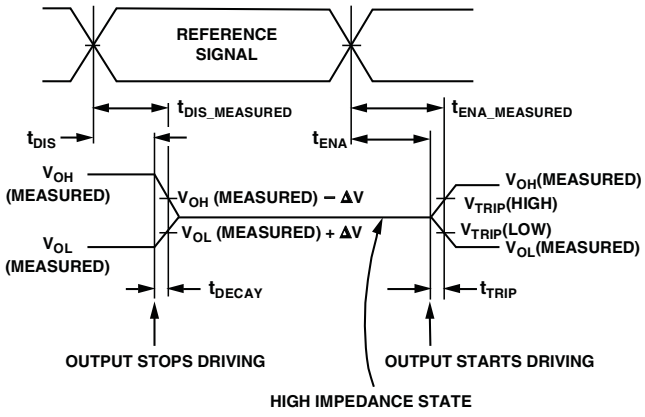


Figure 42. Output Enable/Disable

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP}(low). For V_{DDEXT} (nominal) = 1.8 V, V_{TRIP} (high) is 1.05 V, and V_{TRIP} (low) is 0.75 V. For V_{DDEXT} (nominal) = 2.5 V, V_{TRIP} (high) is 1.5 V and V_{TRIP} (low) is 1.0 V. For V_{DDEXT} (nominal) = 3.3 V, V_{TRIP} (high) is 1.9 V, and V_{TRIP} (low) is 1.4 V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP}(high) or V_{TRIP}(low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins are enabled, the measurement value is that of the first pin to start driving.

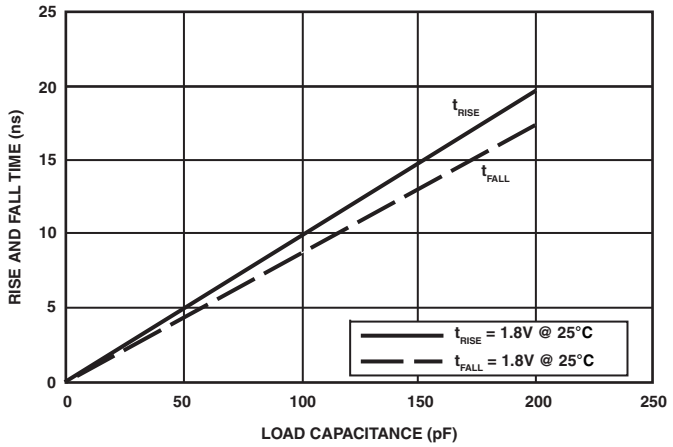


Figure 47. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8 V V_{DDEXT})

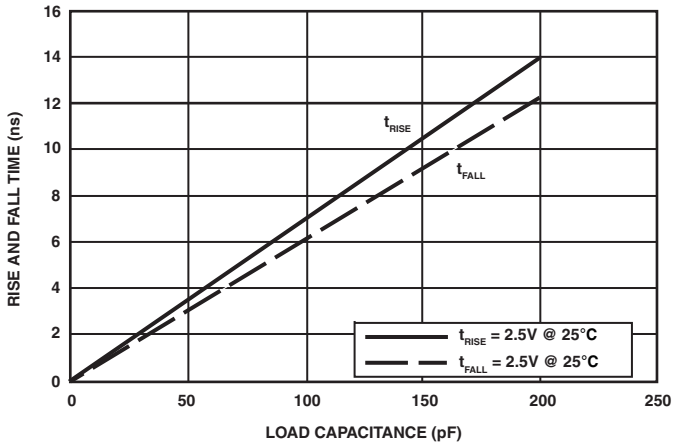


Figure 48. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5 V V_{DDEXT})

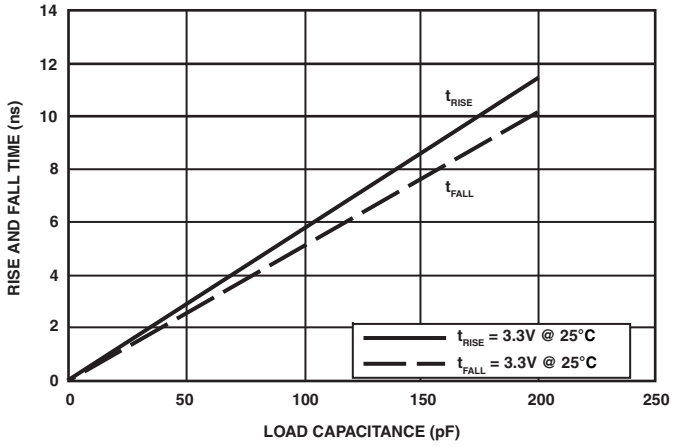


Figure 49. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3 V V_{DDEXT})

PROCESSOR—ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where: T_J = junction temperature (°C).

T_{CASE} = case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = from Table 43 and Table 44.

P_D = power dissipation (see Total Power Dissipation on Page 30 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A = ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 43 and Table 44, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Table 43. Thermal Characteristics (88-Lead LFCSP)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	26.2	°C/W
θ_{JMA}	1 linear m/s air flow	23.7	°C/W
θ_{JMA}	2 linear m/s air flow	22.9	°C/W
θ_{JB}		16.0	°C/W
θ_{JC}		9.8	°C/W
Ψ_{JT}	0 linear m/s air flow	0.21	°C/W
Ψ_{JT}	1 linear m/s air flow	0.36	°C/W
Ψ_{JT}	2 linear m/s air flow	0.43	°C/W

Table 44. Thermal Characteristics (120-Lead LQFP)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	26.9	°C/W
θ_{JMA}	1 linear m/s air flow	24.2	°C/W
θ_{JMA}	2 linear m/s air flow	23.3	°C/W
θ_{JB}		16.4	°C/W
θ_{JC}		12.7	°C/W
Ψ_{JT}	0 linear m/s air flow	0.50	°C/W
Ψ_{JT}	1 linear m/s air flow	0.77	°C/W
Ψ_{JT}	2 linear m/s air flow	1.02	°C/W

Table 48. Operating Conditions (ADC Performance/Accuracy) (Continued)

Parameter	Specification	Unit	Test Conditions/Comments
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity (INL)[1]	±1	LSB max	±0.7 LSB typ; differential mode
	±1.5	LSB max	±0.9 LSB typ; single-ended and pseudo differential modes
Differential Nonlinearity (DNL)[1, 3]	±0.99	LSB max	Differential mode
	–0.99/+1.5	LSB max	Single-ended and pseudo differential modes
Straight Natural Binary Output Coding			
Offset Error[1,2]	±7	LSB max	
Offset Error Match[1,2]	±2	LSB typ	
Gain Error[1,2]	±2.5	LSB max	
Gain Error Match[1,2]	±0.5	LSB typ	
Twos Complement Output Coding			
Positive Gain Error[1,2]	±2	LSB max	
Positive Gain Error Match[1,2]	±0.5	LSB typ	
Zero Code Error[1,2]	±5	LSB max	
Zero Code Error Match[1,2]	±1	LSB typ	
Negative Gain Error[1,2]	±2	LSB max	
Negative Gain Error Match[1,2]	±0.5	LSB typ	
CONVERSION RATE			
Conversion Time	14	ADSCLK cycles	437.5 ns with ADSCLK = 32 MHz
Track-and-Hold Acquisition Time[2]	90	ns max	Full-scale step input; AV_{DD}, DV_{DD} = 5 V
	110	ns max	Full-scale step input; AV_{DD}, DV_{DD} = 3 V
Throughput Rate	2	MSPS max	

[1] See ADC—Terminology on Page 61.
[2] Sample tested during initial release to ensure compliance.
[3] Guaranteed no missed codes to 12 bits.

Table 49. Operating Conditions (Power[1])

Parameter	Specification	Unit	Test Conditions/Comments
POWER SUPPLY REQUIREMENTS			
V_{DD}	2.7/5.25	V min/V max	
V_{DRIVE}	2.7/5.25	V min/V max	
I_{DD}			Digital Logic Inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	2.3	mA max	V_{DD} = 5.25 V
Operational			
f_S = 2 MSPS	6.4	mA max	V_{DD} = 5.25 V; 5.7 mA typ
f_S = 1.5 MSPS	4	mA max	V_{DD} = 3.6 V; 3.4 mA typ
Partial Power-Down Mode	500	µA max	Static
Full Power-Down Mode (V_{DD})	2.8	µA max	Static
POWER DISSIPATION			
Normal Mode (Operational)	33.6	mW max	V_{DD} = 5.25 V
Partial Power-Down (Static)	2.625	mW max	V_{DD} = 5.25 V
Full Power-Down (Static)	14.7	µW max	V_{DD} = 5.25 V

[1] In this table, V_{DD} refers to both AV_{DD} and DV_{DD}.

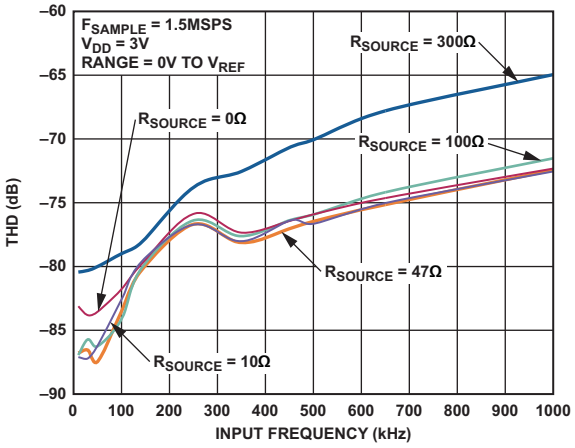


Figure 66. THD vs. Analog Input Frequency for Various Source Impedances, Differential Mode

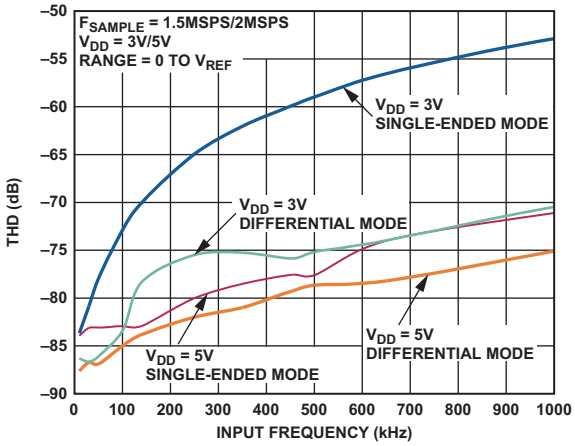


Figure 67. THD vs. Analog Input Frequency for Various Supply Voltages

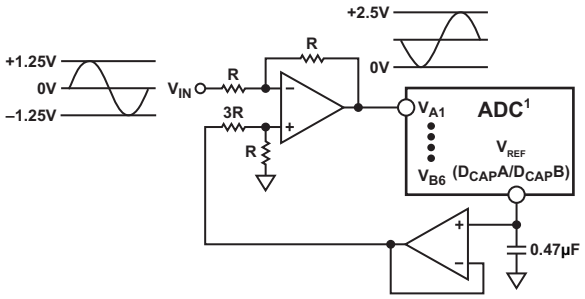
Analog Inputs

The ADC has a total of 12 analog inputs. Each on-board ADC has six analog inputs that can be configured as six single-ended channels, three pseudo differential channels, or three fully differential channels. These may be selected as described in the Analog Input Selection section.

Single-Ended Mode

The ADC can have a total of 12 single-ended analog input channels. In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 to V_{REF} or 0 to 2 × V_{REF}.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal to make it correctly formatted for the ADC. Figure 68 shows a typical connection diagram when operating the ADC in single-ended mode.



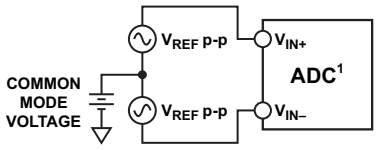
[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 68. Single-Ended Mode Connection Diagram

Differential Mode

The ADC can have a total of six differential analog input pairs.

Differential signals have some benefits over single-ended signals, including noise immunity based on the device's common-mode rejection and improvements in distortion performance. Figure 69 (Differential Input Definition) defines the fully differential analog input of the ADC.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 69. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair (V_{IN+} V_{IN-}). V_{IN+} and V_{IN-} should be simultaneously driven by two signals each of amplitude V_{REF} (or 2 × V_{REF}, depending on the range chosen) that are 180° out of phase. The amplitude of the differential signal is, therefore (assuming the 0 to V_{REF} range is selected) –V_{REF} to +V_{REF} peak-to-peak (2 × V_{REF}), regardless of the common mode (CM).

The common mode is the average of the two signals

$$(V_{IN+} + V_{IN-})/2$$

and is, therefore, the voltage on which the two inputs are centered.

This results in the span of each input being CM ± V_{REF}/2. This voltage has to be set up externally and its range varies with the reference value, V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the amplifier's output voltage swing.

Figure 70 (Input Common-Mode Range vs. VREF (0 to VREF Range, VDD = 5 V)) and Figure 71 (Input Common-Mode Range vs. VREF (2 × VREF Range, VDD = 5 V)) show how the common-mode range typically varies with V_{REF} for a 5 V power

Table 55. 120-Lead LQFP Lead Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	V_{DDEXT}	31	PG3	61	V_{DDINT}	91	V_{B2}
2	PF2	32	PG4	62	V_{DDEXT}	92	V_{B1}
3	PF4	33	TDI	63	$V_{DDFLASH}$	93	AGND
4	PF3	34	TCK	64	V_{DDEXT}	94	$D_{CAP}B$
5	PF5	35	TMS	65	V_{DDINT}	95	RANGE
6	V_{DDEXT}	36	TDO	66	V_{DDEXT}	96	SGL/$\overline{DIFF}$
7	PF6	37	$\overline{TRST}$	67	V_{DDEXT}	97	A2
8	PF7	38	PG5	68	$\overline{EMU}$	98	A1
9	PF8	39	PG6	69	$V_{DDFLASH}$	99	AGND
10	PF9	40	PG7	70	EXT_WAKE	100	A0
11	$\overline{NMI}$	41	V_{DDEXT}	71	$\overline{PG}$	101	$\overline{CS}$
12	$\overline{RESET}$	42	V_{DDINT}	72	NC	102	ADSCLK
13	GND	43	PG8	73	AGND	103	$D_{OUT}B$
14	PF10	44	PG9	74	DGND	104	DGND
15	V_{DDEXT}	45	PG10	75	REF_SELECT	105	$D_{OUT}A$
16	PF11	46	PG11	76	AV_{DD}	106	V_{DRIVE}
17	GND	47	PG12	77	$D_{CAP}A$	107	DV_{DD}
18	PF12	48	PG13	78	AGND	108	GND
19	PF13	49	PG14	79	AGND	109	GND
20	V_{DDEXT}	50	PG15	80	V_{A1}	110	CLKIN
21	PF14	51	V_{DDEXT}	81	V_{A2}	111	XTAL
22	PF15	52	V_{DDINT}	82	AGND	112	V_{DDEXT}
23	V_{DDEXT}	53	V_{DDINT}	83	V_{A3}	113	PH0
24	V_{DDINT}	54	SDA	84	V_{A4}	114	PH2
25	$V_{DDFLASH}$	55	SCL	85	V_{A5}	115	PH1
26	V_{DDEXT}	56	BMODE2	86	V_{A6}	116	V_{DDEXT}
27	PG0	57	BMODE1	87	V_{B6}	117	V_{DDINT}
28	PG1	58	BMODE0	88	V_{B5}	118	PF0
29	PG2	59	V_{DDEXT}	89	V_{B4}	119	PF1
30	V_{DDEXT}	60	NC	90	V_{B3}	120	EXTCLK
						121*	GND
						122**	AGND

* Pin no. 121 is the GND supply (see Figure 89 and Figure 90) for the processor (4.6mm × 6.17mm); this pad **must** connect to GND.
** Pin no. 122 is the AGND supply (see Figure 89 and Figure 90) for the ADC (2.81mm × 2.81mm); this pad **must** connect to AGND.

88-LEAD LFCSP LEAD ASSIGNMENT

Table 56 lists the LFCSP leads by signal mnemonic. Table 57 on Page 77 lists the LFCSP by lead number.

Table 56. 88-Lead LFCSP Lead Assignment (Alphabetical by Signal)

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
BMODE0	51	PF4	82	PG9	34	V_{DDEXT}	20
BMODE1	50	PF5	83	PG10	35	V_{DDEXT}	31
BMODE2	49	PF6	85	PG11	36	V_{DDEXT}	41
CLKIN	68	PF7	86	PG12	37	V_{DDEXT}	52
$\overline{EMU}$	60	PF8	87	PG13	38	V_{DDEXT}	54
EXT_WAKE	62	PF9	88	PG14	39	V_{DDEXT}	56
EXTCLK	78	PF10	4	PG15	40	V_{DDEXT}	58
GND	3	PF11	6	PH0	71	V_{DDEXT}	59
GND	7	PF12	8	PH1	72	V_{DDEXT}	70
GND	67	PF13	9	PH2	73	V_{DDEXT}	74
NC	45	PF14	11	$\overline{RESET}$	2	V_{DDEXT}	79
NC	46	PF15	12	SCL	44	V_{DDEXT}	84
NC	47	$\overline{PG}$	63	SDA	43	$V_{DDFLASH}$	15
NC	48	PG0	17	TCK	24	$V_{DDFLASH}$	55
NC	64	PG1	18	TDI	23	$V_{DDFLASH}$	61
NC	65	PG2	19	TDO	27	V_{DDINT}	14
NC	66	PG3	21	TMS	25	V_{DDINT}	32
$\overline{NMI}$	1	PG4	22	$\overline{TRST}$	26	V_{DDINT}	42
PF0	76	PG5	28	V_{DDEXT}	5	V_{DDINT}	53
PF1	77	PG6	29	V_{DDEXT}	10	V_{DDINT}	57
PF2	80	PG7	30	V_{DDEXT}	13	V_{DDINT}	75
PF3	81	PG8	33	V_{DDEXT}	16	XTAL	69
						GND	89*

* Pin no. 89 is the GND supply (see Figure 92) for the processor; this pad **must** connect to GND.

Figure 91 shows the top view of the LFCSP pin configuration.

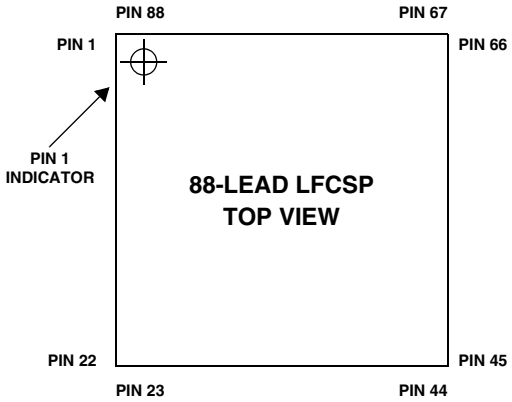


Figure 91. 88-Lead LFCSP Lead Configuration (Top View)

Figure 92 shows the bottom view of the LFCSP lead configuration.

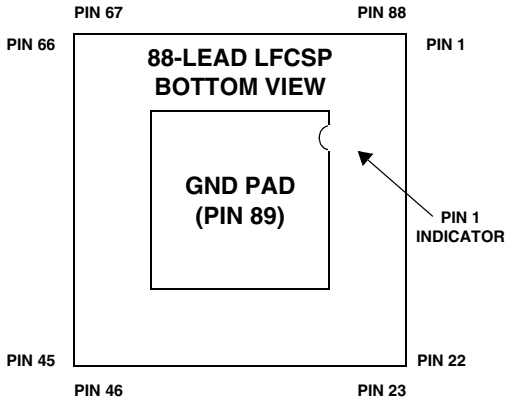


Figure 92. 88-Lead LFCSP Lead Configuration (Bottom View)

AUTOMOTIVE PRODUCTS

The ADBF504W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 58 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 58. Automotive Products

Automotive Models[1,2]	Temperature Range[3]	Processor Instruction Rate (Maximum)	Flash Memory	Package Description	Package Option
ADBF504WYCPZ4XX	–40°C to +105°C	400 MHz	N/A	88-Lead LFCSP_VQ	CP-88-5

[1] Z = RoHS compliant part.
[2] The use of xx designates silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 26 for junction temperature (T_J) specification which is the only temperature specification.

ORDERING GUIDE

Model[1,2]	Temperature Range[3,4]	Processor Instruction Rate (Maximum)	Flash Memory	Package Description	Package Option
ADSP-BF504BCPZ-3F	–40°C to +85°C	300 MHz	32M bit	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504BCPZ-4	–40°C to +85°C	400 MHz	N/A	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504BCPZ-4F	–40°C to +85°C	400 MHz	32M bit	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504KCPZ-3F	0°C to +70°C	300 MHz	32M bit	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504KCPZ-4	0°C to +70°C	400 MHz	N/A	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF504KCPZ-4F	0°C to +70°C	400 MHz	32M bit	88-Lead LFCSP_VQ	CP-88-5
ADSP-BF506BSWZ-3F	–40°C to +85°C	300 MHz	32M bit	120-Lead LQFP_EP	SW-120-2
ADSP-BF506BSWZ-4F	–40°C to +85°C	400 MHz	32M bit	120-Lead LQFP_EP	SW-120-2
ADSP-BF506KSWZ-3F	0°C to +70°C	300 MHz	32M bit	120-Lead LQFP_EP	SW-120-2
ADSP-BF506KSWZ-4F	0°C to +70°C	400 MHz	32M bit	120-Lead LQFP_EP	SW-120-2

[1] Z = RoHS compliant part.
[2] For feature comparison between ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors, see the Processor Comparison in Table 1 on Page 3.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 26 for junction temperature (T_J) specification which is the only temperature specification.
[4] Temperature range 0°C to +70°C is classified as commercial, and temperature range –40°C to +85°C is classified as industrial.