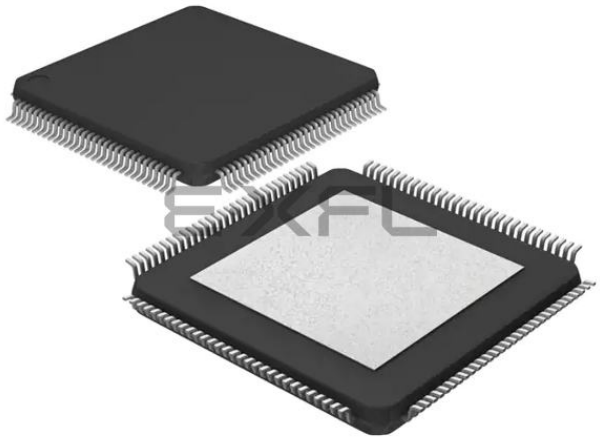

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, EBI/EMI, I²C, IrDA, PPI, SPI, SPORT, UART/USART
Clock Rate	300MHz
Non-Volatile Memory	FLASH (16MB)
On-Chip RAM	68kB
Voltage - I/O	3.30V
Voltage - Core	1.29V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP Exposed Pad
Supplier Device Package	120-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf506bswz-3f

- DMA operations with single-cycle overhead—Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts—Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability—Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF50x processors have two SPI-compatible ports that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins MOSI (Master Output-Slave Input) and MISO (Master Input-Slave Output) and a clock pin, serial clock (SCK). An SPI chip select input pin ($\overline{\text{SPIx\_SS}}$) lets other SPI devices select the processor, and three SPI chip select output pins ($\overline{\text{SPIx\_SEL3–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS (UARTS)

The ADSP-BF50x Blackfin processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports. Each UART port provides a simplified UART interface to other peripherals or hosts, enabling full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits; one or two stop bits; and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O). The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access). The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates. Flexible interrupt timing options are available on the transmit side.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16^{(1-EDBO)} \times UART\_Divisor}$$

Where the 16-bit UART divisor comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant eight bits), and the EDBO is a bit in the UARTx_GCTL register.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The UARTs feature a pair of $\overline{\text{UAx\_RTS}}$ (request to send) and $\overline{\text{UAx\_CTS}}$ (clear to send) signals for hardware flow purposes. The transmitter hardware is automatically prevented from sending further data when the $\overline{\text{UAx\_CTS}}$ input is de-asserted. The receiver can automatically de-assert its $\overline{\text{UAx\_RTS}}$ output when the enhanced receive FIFO exceeds a certain high-water level. The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

- Input mode—Frame syncs and data are inputs into the PPI.
- Frame capture mode—Frame syncs are outputs from the PPI, but data are inputs.
- Output mode—Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF50x processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

RSI INTERFACE

The removable storage interface (RSI) controller acts as the host interface for multimedia cards (MMC), secure digital memory cards (SD), secure digital input/output cards (SDIO), and CE-ATA hard disk drives. The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card or CE-ATA hard disk drive
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit, and 8-bit MMC modes
- Support for 4-bit and 8-bit CE-ATA hard disk drives
- A ten-signal external interface with clock, command, and up to eight data lines
- Card detection using one of the data signals
- Card interface clock generation from SCLK
- SDIO interrupt and read wait features
- CE-ATA command completion signal recognition and disable

CONTROLLER AREA NETWORK (CAN) INTERFACE

The ADSP-BF50x processors provide a CAN controller that is a communication controller implementing the Controller Area Network (CAN) V2.0B protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. CAN is well suited for control applications due to its capability to communicate reliably over a network since the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller is based on a 32-entry mailbox RAM and supports both the standard and extended identifier (ID) message formats specified in the CAN protocol specification, revision 2.0, part B.

ADC APPLICATION HINTS

The following sections provide application hints for using the ADC.

Grounding and Layout Considerations

The analog and digital supplies to the ADC are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the ADC should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All AGND pins should be sunk in the AGND plane. Digital and analog ground planes should be joined in only one place. If the ADC is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the ground pins on the ADC.

Avoid running digital lines under the device as this couples noise onto the die. Avoid running digital lines in the area of the AGND pad as this couples noise onto the ADC die and into the AGND plane. The power supply lines to the ADC should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feed through within the board, traces on opposite sides of the board should run at right angles to each other.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF50x processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF50x Blackfin Processor Hardware Reference* (volumes 1 and 2)
- *Blackfin Processor Programming Reference*
- *ADSP-BF50x Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http:\\www.analog.com\signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 11. Processor—Signal Descriptions (Continued)

Signal Name	Type	Function	Driver Type
PG14/*UA0_RTS*/SD_D6/TMR0/PPI_FS1/CUD1	I/O	GPIO/*UART0 RTS*/SD Data 6/Timer0/PPI FS1/Count Up Dir 1	C
PG15/*UA0_CTS*/SD_D7/TMR1/PPI_FS2/CDG1	I/O	GPIO/*UART0 CTS*/SD Data 7/Timer1/PPI FS2/Count Down Dir 1	C
Port H: *GPIO and Multiplexed Peripherals*			
PH0/*ACM_A2*/DT1PRI/*SPI0_SEL3*/WAKEUP	I/O	GPIO/*ADC CM A2*/SPORT1 TX Pri Data/SPI0 Slave Select 3/Wake-up Input	C
PH1/*ACM_A1*/TFS1/*SPI1_SEL3*/TACLK3	I/O	GPIO/*ADC CM A1*/SPORT1 TX Frame Sync/SPI1 Slave Select 3/Alt Timer CLK 3	C
PH2/*ACM_A0*/TSCLK1/*SPI1_SEL2*/TACI7	I/O	GPIO/*ADC CM A0*/SPORT1 TX Serial CLK/SPI1 Slave Select 2/Alt Capture In 7	C
TWI (2-Wire Interface) Port			
SCL	I/O 5 V	TWI Serial Clock (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	D
SDA	I/O 5 V	TWI Serial Data (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	D
JTAG Port			
TCK	I	JTAG CLK	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$	I	JTAG Reset (This signal should be pulled low if the JTAG port is not used.)	
$\overline{\text{EMU}}$	O	Emulation Output	C
Clock			
CLKIN	I	CLK/Crystal In	
XTAL	O	Crystal Output	
EXTCLK	O	Clock Output	B
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Nonmaskable Interrupt (This signal should be pulled high when not used.)	
BMODE2–0	I	Boot Mode Strap 2-0	
ADSP-BF50x Voltage Regulation I/F			
EXT_WAKE	O	Wake up Indication	C
$\overline{\text{PG}}$	I	Power Good	
Power Supplies		**ALL SUPPLIES MUST BE POWERED** See Operating Conditions on Page 26.	
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Internal Power Supply	
$V_{DDFLASH}$	P	Flash Memory Power Supply	
GND	G	Ground for All Supplies	

ADSP-BF50x Clock Related Operating Conditions

Table 14 describes the core clock timing requirements for the ADSP-BF50x processors. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock (see Table 16). Table 15 describes phase-locked loop operating conditions.

Table 14. Core Clock (CCLK) Requirements—ADSP-BF50x Processors—All Speed Grades

Parameter		Min V_{DDINT}	Nom V_{DDINT}	Max CCLK Frequency	Unit
f_{CCLK}	Core Clock Frequency (All Models)	1.33 V	1.400 V	400	MHz
	Core Clock Frequency (Industrial/Commercial Models)	1.16 V	1.225 V	300	MHz
	Core Clock Frequency (Industrial Models Only)	1.14 V	1.200 V	200	MHz
	Core Clock Frequency (Commercial Models Only)	1.10 V	1.150 V	200	MHz

Table 15. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency (Commercial/Industrial Models)	72	Instruction Rate[1]	MHz
	Voltage Controlled Oscillator (VCO) Frequency (Automotive Models)	84	Instruction Rate[1]	MHz

[1] For more information, see Ordering Guide on Page 81.

Table 16. Maximum SCLK Conditions for ADSP-BF50x Processors

Parameter		V_{DDEXT} = 1.8 V/2.5 V/3.3 V Nominal	Unit
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq 1.16$ V)	100	MHz
	CLKOUT/SCLK Frequency ($V_{DDINT} < 1.16$ V)	80	MHz

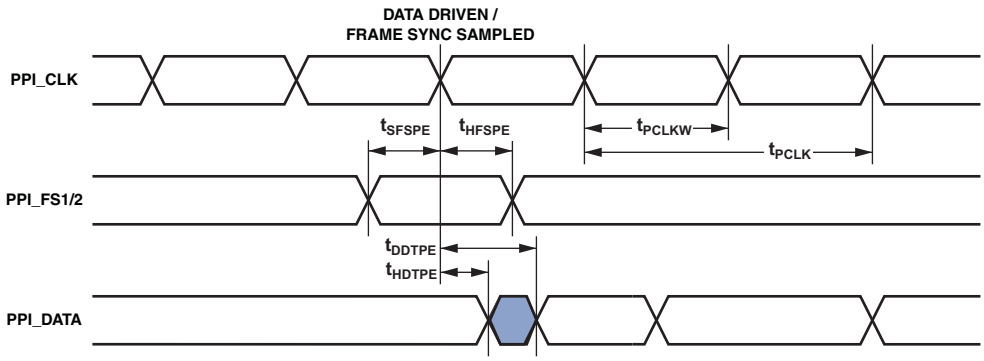


Figure 15. PPI GP Tx Mode with External Frame Sync Timing

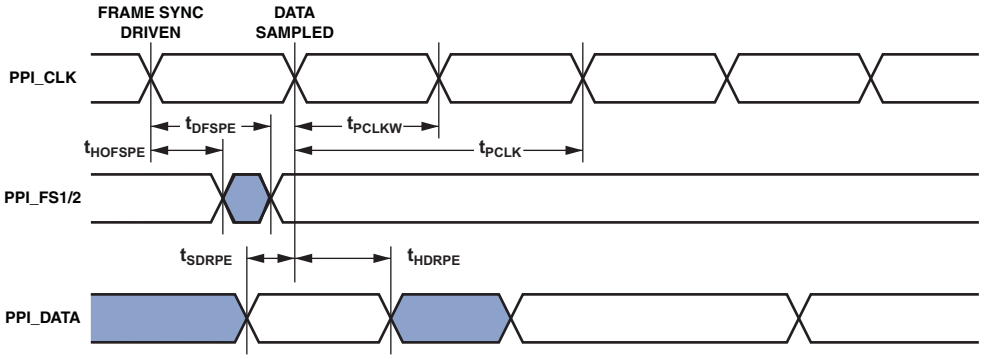


Figure 16. PPI GP Rx Mode with Internal Frame Sync Timing

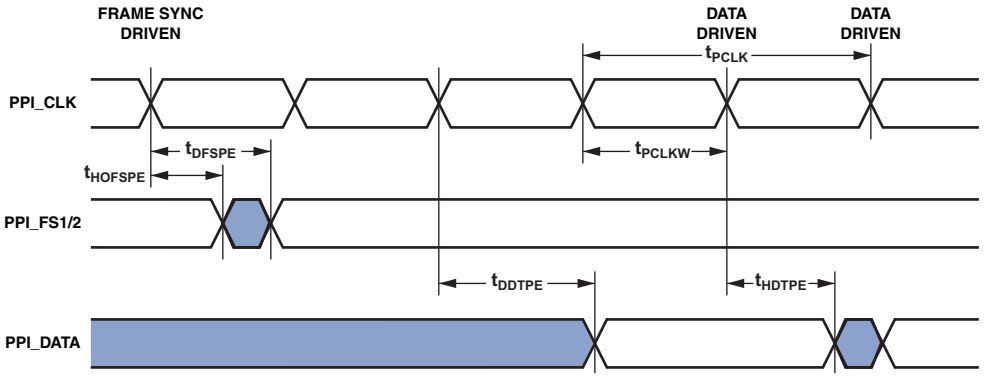


Figure 17. PPI GP Tx Mode with Internal Frame Sync Timing

Serial Peripheral Interface (SPI) Port—Master Timing

Table 34 and Figure 23 describe SPI port master operations.

Table 34. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	11.6		9.6		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPISELx}$ low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 2.0$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)	0	6	0	6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0		–1.0		ns

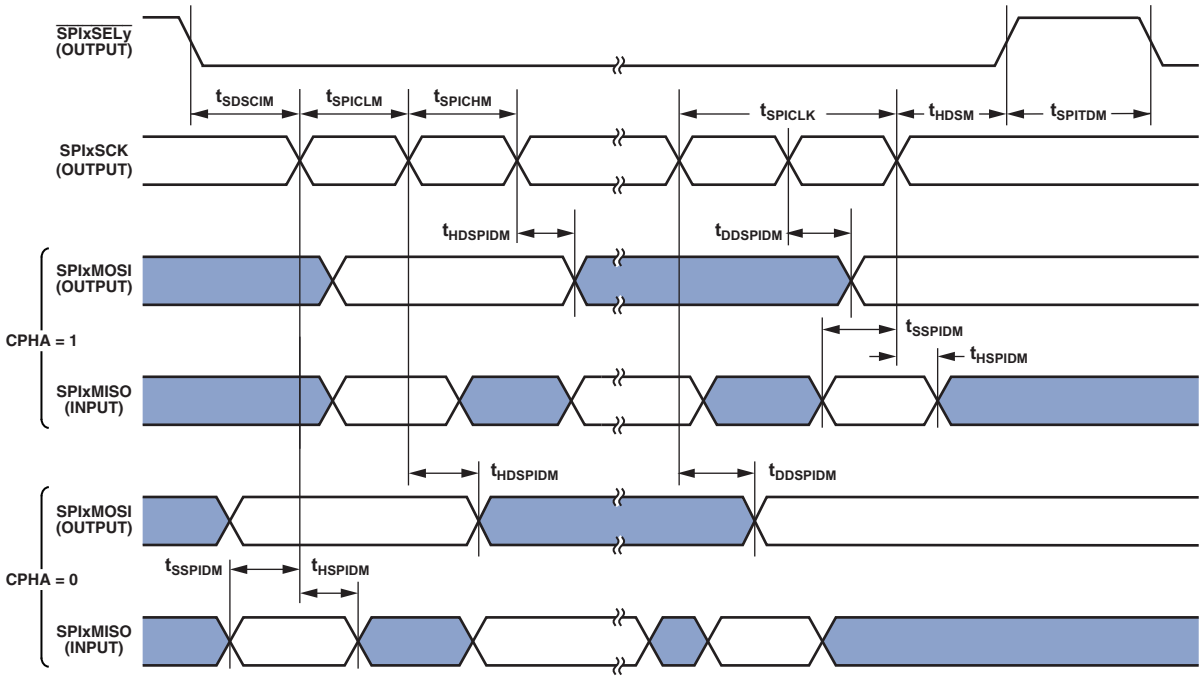


Figure 23. Serial Peripheral Interface (SPI) Port—Master Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the *ADSP-BF50x Hardware Reference Manual*.

General-Purpose Port Timing

Table 36 and Figure 25 describe general-purpose port operations.

Table 36. General-Purpose Port Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirement						
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
Switching Characteristic						
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT High	0	11.0	0	8.9	ns

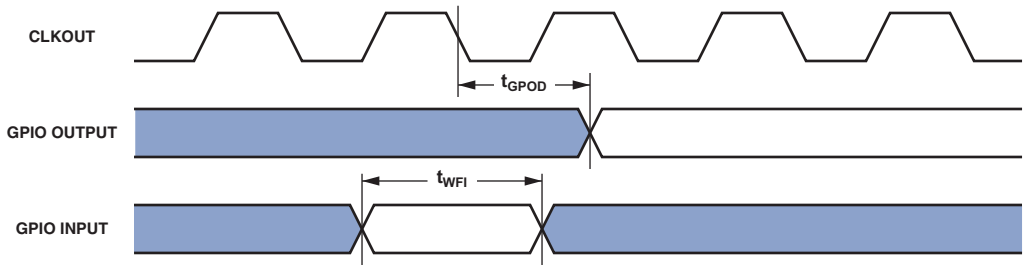


Figure 25. General-Purpose Port Timing

PROCESSOR—OUTPUT DRIVE CURRENTS

Figure 32 through Figure 40 show typical current-voltage characteristics for the output drivers of the ADSP-BF50xF processors.

The curves represent the current drive capability of the output drivers. See Table 11 on Page 22 for information about which driver type corresponds to a particular pin.

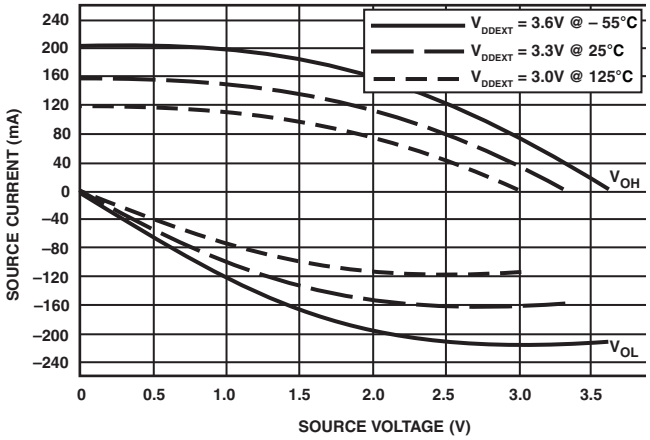


Figure 32. Driver Type B Current (3.3 V V_{DDEXT})

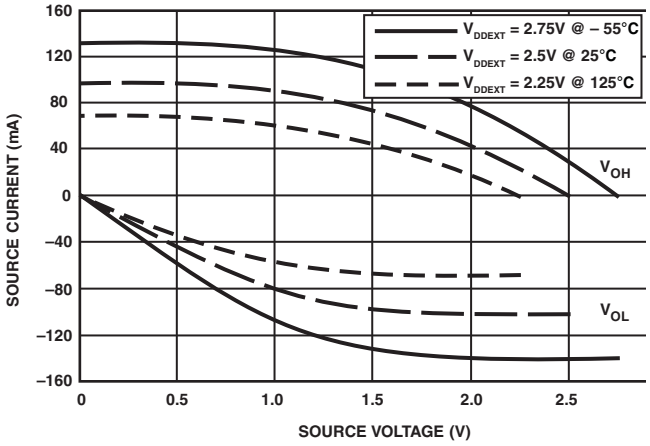


Figure 33. Driver Type B Current (2.5 V V_{DDEXT})

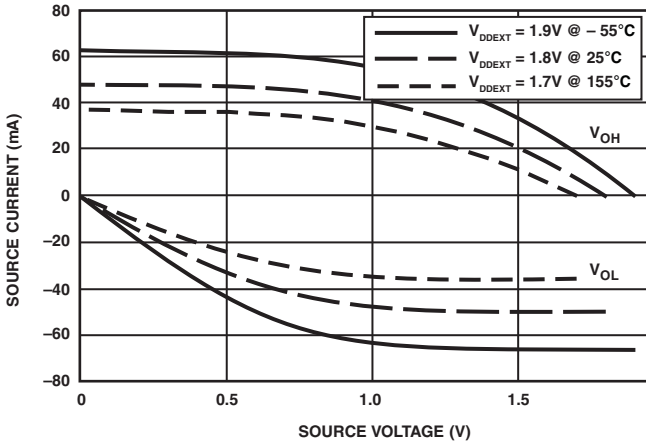


Figure 34. Driver Type B Current (1.8 V V_{DDEXT})

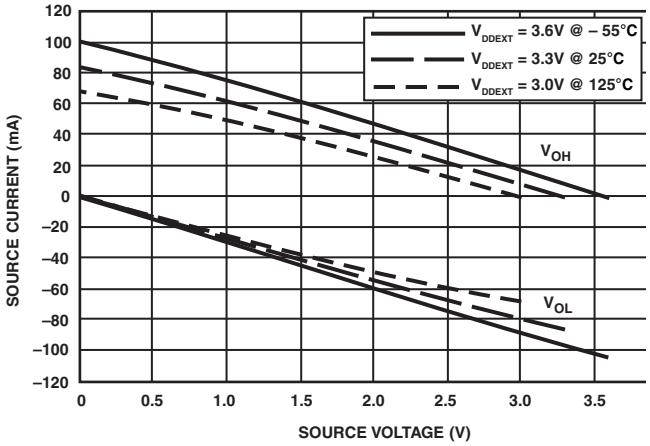


Figure 35. Driver Type C Current (3.3 V V_{DDEXT})

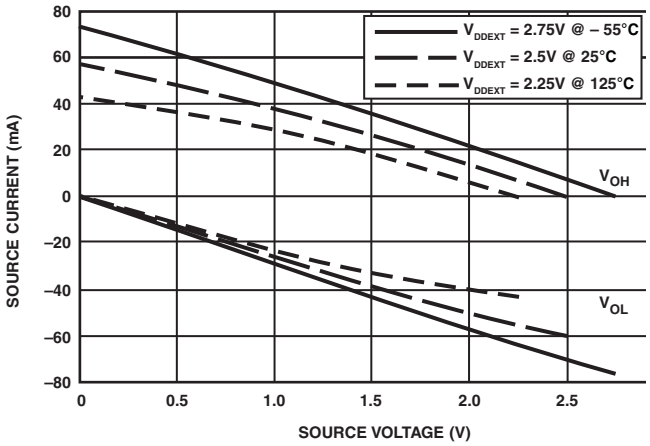


Figure 36. Drive Type C Current (2.5 V V_{DDEXT})

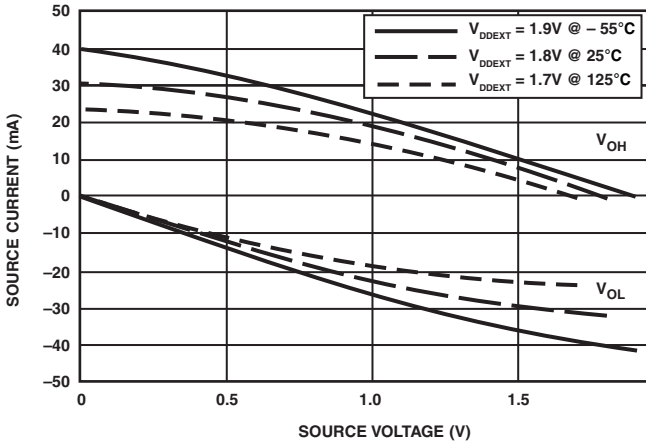


Figure 37. Driver Type C Current (1.8 V V_{DDEXT})

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 42.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.25 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V and 0.15 V for V_{DDEXT} (nominal) = 1.8 V.

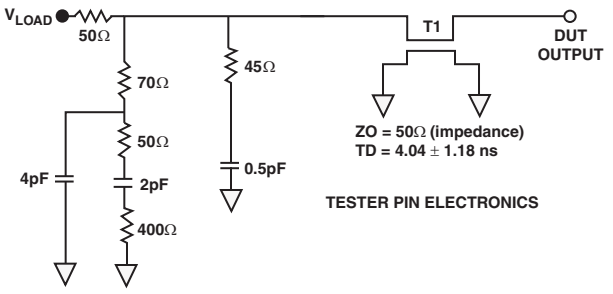
The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Processor—Timing Specifications on Page 33.

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 43). V_{LOAD} is equal to (V_{DDEXT}) /2. The graphs of Figure 44 through Figure 49 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 43. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

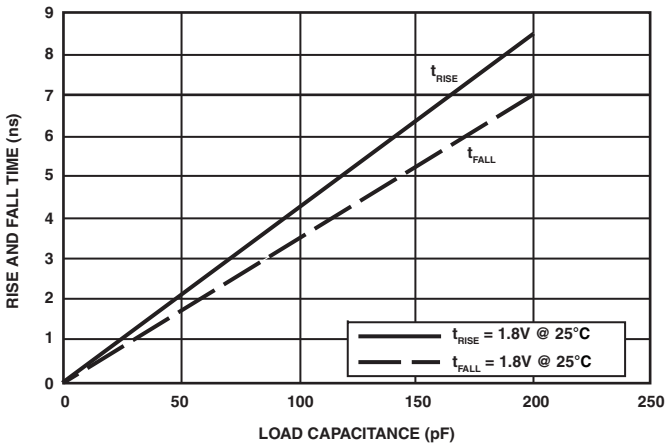


Figure 44. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8 V V_{DDEXT})

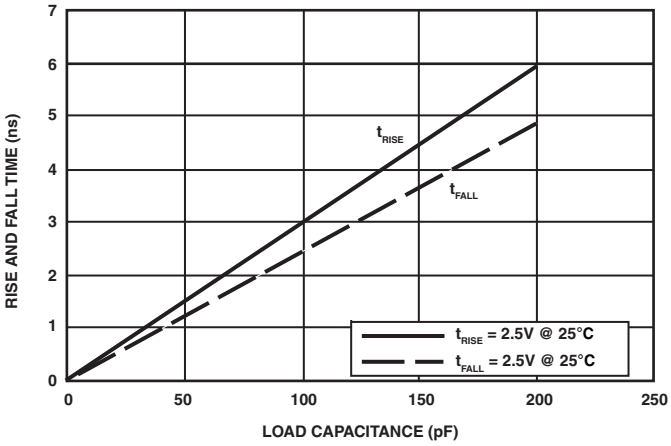


Figure 45. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5 V V_{DDEXT})

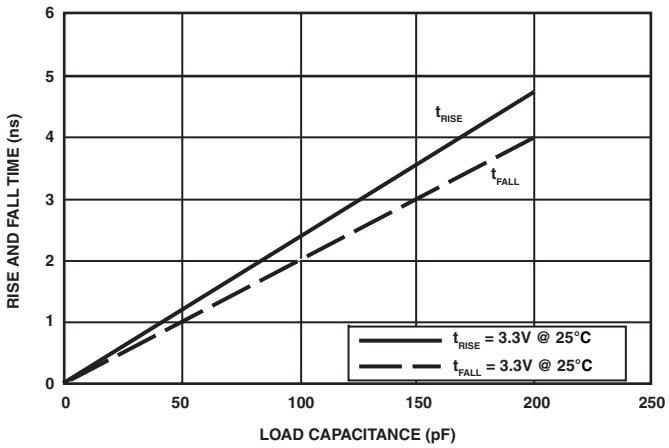


Figure 46. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3 V V_{DDEXT})

ADC—SPECIFICATIONS

Specifications are subject to change without notice.

ADC—OPERATING CONDITIONS

Parameter	Conditions	Min	Nominal	Max	Unit
V_{DD}[1] (AV_{DD}, DV_{DD}, V_{DRIVE})	f_{ADSCLK} = 24 MHz, f_S up to 1.5 MSPS, internal or external reference = 2.5 V ± 1% unless otherwise noted	2.7		3.6	V
	f_{ADSCLK} = 25 MHz, f_S up to 1.56 MSPS, internal or external reference = 2.5 V ± 1% unless otherwise noted	3.0		3.6	V
	f_{ADSCLK} = 32 MHz, f_S up to 2.0 MSPS, internal or external reference = 2.5 V ± 1% unless otherwise noted	4.75 (AV_{DD}, DV_{DD}) 2.7 (V_{DRIVE})		5.25 (AV_{DD}, DV_{DD}) 5.25 (V_{DRIVE})	V V
T_J Junction Temperature	120-Lead LQFP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C

[1] Throughout the ADC sections of this data sheet, V_{DD} refers to both AV_{DD} and DV_{DD}.

Table 47. Operating Conditions (Analog, Voltage Reference, and Logic I/O)

Parameter	Specification	Unit	Test Conditions/Comments
ANALOG INPUT[1]			
Single-Ended Input Range	0 V to V_{REF}	V	RANGE= low
	0 V to 2 × V_{REF}	V	RANGE = high
Pseudo Differential Input Range: V_{IN+} – V_{IN-}[2]	0 V to V_{REF}	V	RANGE = low
	2 × V_{REF}	V	RANGE = high
Fully Differential Input Range: V_{IN+} and V_{IN-}	V_{CM} ± V_{REF}/2	V	V_{CM} = common-mode voltage[3] = V_{REF}/2, RANGE = low
	V_{CM} ± V_{REF}	V	V_{CM} = V_{REF}, RANGE = high
DC Leakage Current	±1	µA max	V_{A1} to V_{A6}, V_{B1} to V_{B6}
Input Capacitance[4]	45	pF typ	When in track
	10	pF typ	When in hold
INTERNAL VOLTAGE REFERENCE (OUTPUT)[5]			
Reference Output Voltage	2.5 ± 0.4%	V	@ 25°C, AV_{DD} = 2.7 V to 5.25 V
Long-Term Stability[4]	150	ppm typ	For 1000 hours
Output Voltage Thermal Hysteresis[6]	50	ppm typ	
D_{CAP}A, D_{CAP}B Output Impedance[4]	10	Ω typ	
Reference Temperature Coefficient[4]	60 max, 20 typ	ppm/°C	
V_{REF} Noise[4]	20	µV rms typ	
EXTERNAL VOLTAGE REFERENCE (INPUT)[5]			
Reference Input Voltage Range[7]	0.1 to AV_{DD}	V	See ADC—Typical Performance Characteristics
DC Leakage Current[7]	±2	µA max	
Input Capacitance[4]	25	pF typ	
DIGITAL LOGIC INPUTS			
Input High Voltage, V_{INH}	2.8	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±15	nA typ	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[4]	5	pF typ	

Table 47. Operating Conditions (Analog, Voltage Reference, and Logic I/O) (Continued)

Parameter	Specification	Unit	Test Conditions/Comments
DIGITAL LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V min	No DC load (I_{OH} = 0 mA)
Output Low Voltage, V_{OL}	0.4	V max	No DC load (I_{OL} = 0 mA)
Floating State Leakage Current	±1	µA max	V_{IN} = 0 V or V_{DRIVE}
Floating State Output Capacitance[4]	7	pF typ	
Output Coding[8]	Straight (natural) binary twos complement		

[1] V_{IN-} or V_{IN+} must remain within GND/V_{DD}.
[2] V_{IN-} = 0 V for specified performance. For full input range on V_{IN-} pin, see Figure 74 and Figure 75.
[3] For full common-mode range, see Figure 70 and Figure 71.
[4] Sample tested during initial release to ensure compliance.
[5] Relates to Pin D_{CAP}A or Pin D_{CAP}B (V_{REF}).
[6] See ADC—Terminology on Page 61.
[7] External voltage reference applied to Pins D_{CAP}A, Pin D_{CAP}B (V_{REF}).
[8] See Table 52 and Table 53.

Table 48. Operating Conditions (ADC Performance/Accuracy)

Parameter	Specification	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal-to-Noise Ratio (SNR)	71	dB min	f_{IN} = 14 kHz sine wave; differential mode
	69	dB min	f_{IN} = 14 kHz sine wave; single-ended and pseudo differential modes
Signal-to-(Noise + Distortion) Ratio (SINAD)[1]	70	dB min	f_{IN} = 14 kHz sine wave; differential mode
	68	dB min	f_{IN} = 14 kHz sine wave; single-ended and pseudo differential modes
Total Harmonic Distortion (THD)[1]	–77	dB max	f_{IN} = 14 kHz sine wave; differential mode
	–73	dB max	f_{IN} = 14 kHz sine wave; single-ended and pseudo differential modes
Spurious-Free Dynamic Range (SFDR)[1]	–75	dB max	f_{IN} = 50 kHz sine wave
Intermodulation Distortion (IMD)[1,2]			f_a = 30 kHz, fb = 50 kHz
Second-Order Terms	–88	dB typ	
Third-Order Terms	–88	dB typ	
Channel-to-Channel Isolation	–88	dB typ	
SAMPLE AND HOLD			
Aperture Delay[2]	11	ns max	
Aperture Jitter[2]	50	ps typ	
Aperture Delay Matching[2]	200	ps max	
Full Power Bandwidth	33/26	MHz typ	@ 3 dB, AV_{DD}, DV_{DD} = 5 V/AV_{DD}, DV_{DD} = 3 V
	3.5/3	MHz typ	@ 0.1 dB, AV_{DD}, DV_{DD} = 5 V/AV_{DD}, DV_{DD} = 3 V

Table 48. Operating Conditions (ADC Performance/Accuracy) (Continued)

Parameter	Specification	Unit	Test Conditions/Comments
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity (INL)[1]	±1	LSB max	±0.7 LSB typ; differential mode
	±1.5	LSB max	±0.9 LSB typ; single-ended and pseudo differential modes
Differential Nonlinearity (DNL)[1, 3]	±0.99	LSB max	Differential mode
	–0.99/+1.5	LSB max	Single-ended and pseudo differential modes
Straight Natural Binary Output Coding			
Offset Error[1,2]	±7	LSB max	
Offset Error Match[1,2]	±2	LSB typ	
Gain Error[1,2]	±2.5	LSB max	
Gain Error Match[1,2]	±0.5	LSB typ	
Twos Complement Output Coding			
Positive Gain Error[1,2]	±2	LSB max	
Positive Gain Error Match[1,2]	±0.5	LSB typ	
Zero Code Error[1,2]	±5	LSB max	
Zero Code Error Match[1,2]	±1	LSB typ	
Negative Gain Error[1,2]	±2	LSB max	
Negative Gain Error Match[1,2]	±0.5	LSB typ	
CONVERSION RATE			
Conversion Time	14	ADSCLK cycles	437.5 ns with ADSCLK = 32 MHz
Track-and-Hold Acquisition Time[2]	90	ns max	Full-scale step input; AV_{DD}, DV_{DD} = 5 V
	110	ns max	Full-scale step input; AV_{DD}, DV_{DD} = 3 V
Throughput Rate	2	MSPS max	

[1] See ADC—Terminology on Page 61.
[2] Sample tested during initial release to ensure compliance.
[3] Guaranteed no missed codes to 12 bits.

Table 49. Operating Conditions (Power[1])

Parameter	Specification	Unit	Test Conditions/Comments
POWER SUPPLY REQUIREMENTS			
V_{DD}	2.7/5.25	V min/V max	
V_{DRIVE}	2.7/5.25	V min/V max	
I_{DD}			Digital Logic Inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	2.3	mA max	V_{DD} = 5.25 V
Operational			
f_S = 2 MSPS	6.4	mA max	V_{DD} = 5.25 V; 5.7 mA typ
f_S = 1.5 MSPS	4	mA max	V_{DD} = 3.6 V; 3.4 mA typ
Partial Power-Down Mode	500	µA max	Static
Full Power-Down Mode (V_{DD})	2.8	µA max	Static
POWER DISSIPATION			
Normal Mode (Operational)	33.6	mW max	V_{DD} = 5.25 V
Partial Power-Down (Static)	2.625	mW max	V_{DD} = 5.25 V
Full Power-Down (Static)	14.7	µW max	V_{DD} = 5.25 V

[1] In this table, V_{DD} refers to both AV_{DD} and DV_{DD}.

ADC—TIMING SPECIFICATIONS

Table 50. Serial Data Interface[1]

Parameter	Specification	Unit	Test Conditions / Comments
f_{ADSCLK}[2]	1/32	MHz min/max	
$t_{CONVERT}$	$14 \times t_{ADSCLK}$	ns max	$t_{ADSCLK} = 1/f_{ADSCLK}$
	437.5	ns max	f_{ADSCLK} = 32 MHz, f_{SAMPLE} = 2 MSPS; AV_{DD}, DV_{DD} = 5 V
	560.0	ns max	f_{ADSCLK} = 25 MHz, f_{SAMPLE} = 1.56 MSPS; AV_{DD}, DV_{DD} = 3 V
	583.3	ns max	f_{ADSCLK} = 24 MHz, f_{SAMPLE} = 1.5 MSPS; AV_{DD}, DV_{DD} = 2.7 V
t_{QUIET}	30	ns min	Minimum time between end of serial read and next falling edge of $\overline{CS}$
t_2	18/23	ns min	$\overline{CS}$ to ADSCLK setup time; V_{DD} = 5 V/3 V
t_3	15	ns max	Delay from $\overline{CS}$ until $D_{OUT}A$ and $D_{OUT}B$ are three-state disabled
t_4[3]	27/36	ns max	Data access time after ADSCLK falling edge, V_{DD} = 5 V/3 V
t_5	0.45 t_{ADSCLK}	ns min	ADSCLK low pulse width
t_6	0.45 t_{ADSCLK}	ns min	ADSCLK high pulse width
t_7	5/10	ns min	ADSCLK to data valid hold time, V_{DD} = 5 V/3 V
t_8	15	ns max	$\overline{CS}$ rising edge to $D_{OUT}A$, $D_{OUT}B$, high impedance
t_9	30	ns min	$\overline{CS}$ rising edge to falling edge pulse width
t_{10}	5/35	ns min/max	ADSCLK falling edge to $D_{OUT}A$, $D_{OUT}B$, high impedance

[1] See Figure 87 on Page 72 and Figure 88 on Page 72.
[2] Minimum ADSCLK for specified performance; with slower ADSCLK frequencies, performance specifications apply typically.
[3] The time required for the output to cross 0.4 V or 2.4 V.

ADC—ABSOLUTE MAXIMUM RATINGS

Stresses above those listed in Table 51 may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 51. Absolute Maximum Ratings

Parameter	Rating
AV_{DD}, DV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to DGND	–0.3 V to +7 V
V_{DRIVE} to DGND	–0.3 V to DV_{DD}
V_{DRIVE} to AGND	–0.3 V to AV_{DD}
AV_{DD} to DV_{DD}	–0.3 V to +0.3 V
AGND to DGND	–0.3 V to +0.3 V
Analog Input Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	–0.3 V to +7 V
Digital Output Voltage to GND	–0.3 V to V_{DRIVE} + 0.3 V
V_{REF} to AGND	–0.3 V to AV_{DD} + 0.3 V
Input Current to Any ADC Pin Except Supplies[1]	±10 mA
Storage Temperature Range	See Table 20 on Page 31
Junction Temperature Under Bias	See Table 20 on Page 31

[1] Transient currents of up to 100 mA will not cause latch up.

When the ADC starts a conversion (see Figure 63 (ADC Conversion Phase)), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} pins must be matched; otherwise, the two inputs will have different settling times, resulting in errors.

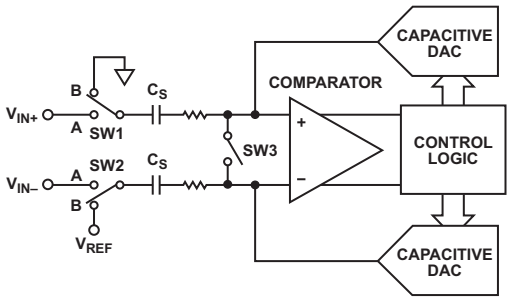


Figure 63. ADC Conversion Phase

Analog Input Structure

Figure 64 (Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed) shows the equivalent circuit of the analog input structure of the ADC in differential/pseudo differential mode. In single-ended mode, V_{IN} is internally tied to AGND. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and starts conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

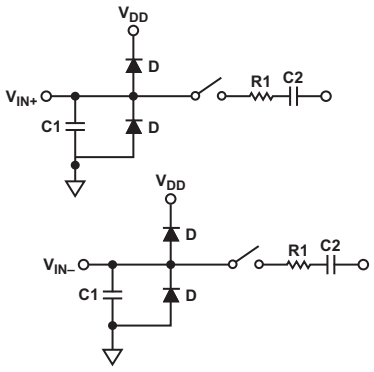


Figure 64. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed

The C1 capacitors in Figure 64 (Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed) are typically 4 pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the ADC's sampling capacitors with a capacitance of 45 pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins with optimum values of 47 Ω and 10 pF. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated.

The THD increases as the source impedance increases and performance degrades. Figure 65 (THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode shows a graph of the THD vs. the analog input signal frequency for different source impedances in single-ended mode, while Figure 66 (THD vs. Analog Input Frequency for Various Source Impedances, Differential Mode) shows the THD vs. the analog input signal frequency for different source impedances in differential mode.

Figure 67 (THD vs. Analog Input Frequency for Various Supply Voltages) shows a graph of the THD vs. the analog input frequency for various supplies while sampling at 2 MSPS. In this case, the source impedance is 47 Ω.

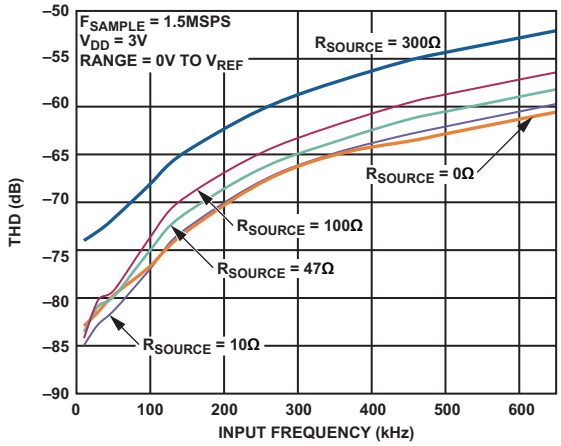


Figure 65. THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode

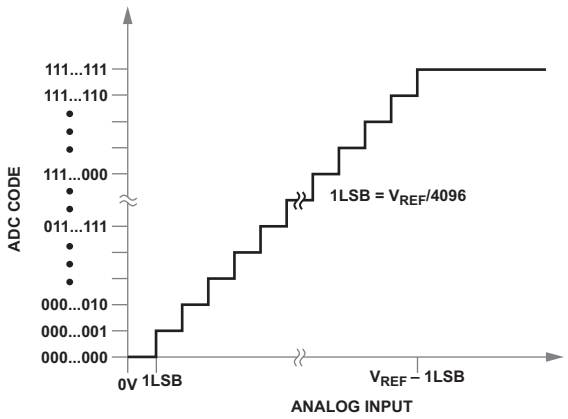


Figure 78. Straight Binary Transfer Characteristic

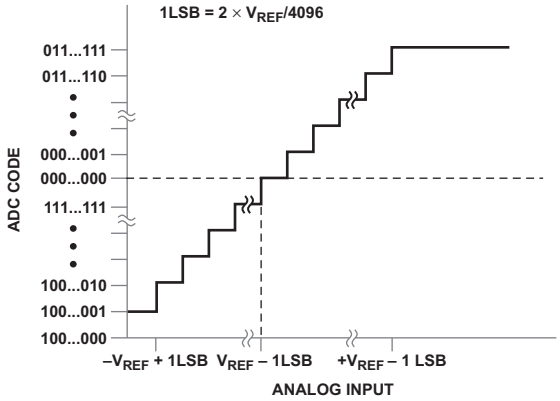


Figure 79. Twos Complement Transfer Characteristic with $V_{REF} \pm V_{REF}$ Input Range

Serial Interface Voltage Drive

The ADC also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the ADC was operated with a AV_{DD}/DV_{DD} of 5 V, the V_{DRIVE} pin could be powered from a 3 V supply, best ADC performance low voltage digital processors. Therefore, the ADC could be used with the $2 \times V_{REF}$ input range, with a AV_{DD}/DV_{DD} of 5 V while still being able to serial interface to 3 V digital I/O parts.

ADC—MODES OF OPERATION

The mode of operation of the ADC is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. After a conversion is initiated, the point at which $\overline{CS}$ is pulled high determines which power-down mode, if any, the device enters. Similarly, if already in a power-down mode, $\overline{CS}$ can control whether the device returns to normal operation or remains in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for applications needing fastest throughput rates because the user does not have to worry about any power-up times with the ADC remaining fully powered at all times. Figure 80 (Normal Mode Operation) shows the general diagram of the operation of the ADC in this mode.

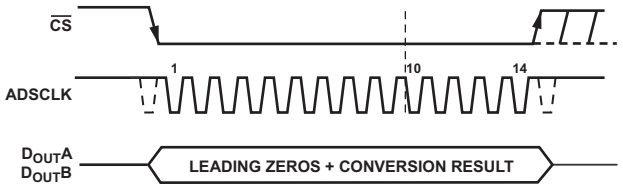


Figure 80. Normal Mode Operation

The conversion is initiated on the falling edge of $\overline{CS}$, as described in the ADC—Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 ADSCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th ADSCLK falling edge but before the 14th ADSCLK falling edge, the part remains powered up, but the conversion is terminated and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. Fourteen serial clock cycles are required to complete the conversion and access the conversion result. The D_{OUT} line does not return to three-state after 14 ADSCLK cycles have elapsed, but instead does so when $\overline{CS}$ is brought high again. If $\overline{CS}$ is left low for another 2 ADSCLK cycles (for example, if only a 16 ADSCLK burst is available), two trailing zeros are clocked out after the data. If $\overline{CS}$ is left low for a further 14 (or16) ADSCLK cycles, the result from the other ADC on board is also accessed on the same D_{OUT} line, as shown in Figure 88 (Reading Data from Both ADCs on One DOUT Line with 32 ADSCLKs). See the ADC—Serial Interface section.

Once 32 ADSCLK cycles have elapsed, the D_{OUT} line returns to three-state on the 32nd ADSCLK falling edge. If $\overline{CS}$ is brought high prior to this, the D_{OUT} line returns to three-state at that point. Therefore, $\overline{CS}$ may idle low after 32 ADSCLK cycles until it is brought high again sometime prior to the next conversion (effectively idling $\overline{CS}$ low), if so desired, because the bus still returns to three-state upon completion of the dual result read.

Once a data transfer is complete and $D_{OUT}A$ and $D_{OUT}B$ have returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again (assuming the required acquisition time is allowed).

Partial Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate, and the ADC is then powered

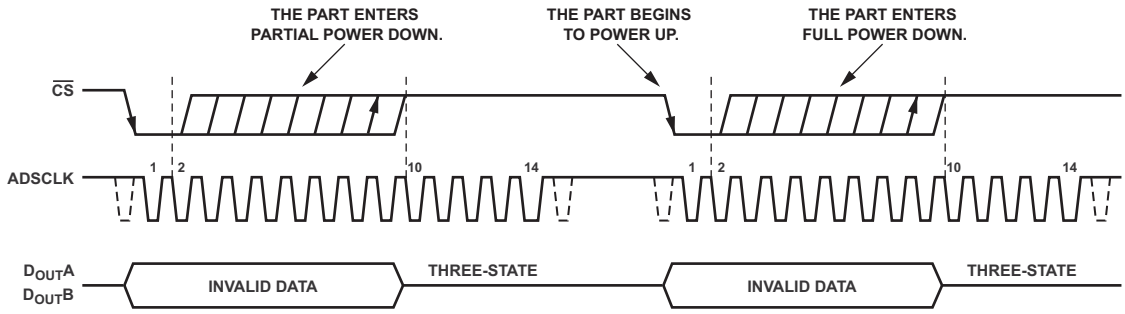


Figure 83. Entering Full Power-Down Mode

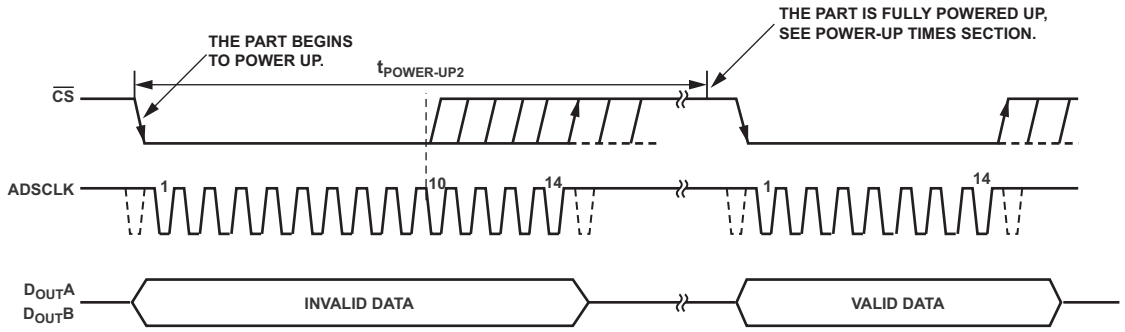


Figure 84. Exiting Full Power-Down Mode

Power-Up Times

As described in detail, the ADC has two power-down modes, partial power-down and full power-down. This section deals with the power-up time required when coming out of either of these modes. It should be noted that the power-up times, as explained in this section, apply with the recommended capacitors in place on the $D_{CAP}A$ and $D_{CAP}B$ pins.

To power up from full power-down, approximately 1.5 ms should be allowed from the falling edge of $\overline{CS}$, shown as $t_{POWER-UP2}$ in Figure 84 (Exiting Full Power-Down Mode). Powering up from partial power-down requires much less time. The power-up time from partial power-down is typically 1 µs; however, if using the internal reference, then the ADC must be in partial power-down for at least 67 µs in order for this power-up time to apply.

When power supplies are first applied to the ADC, the ADC may power up in either of the power-down modes or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the partial power-down mode immediately after the supplies are applied, then two dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th ADSCLK falling edge (see Figure 80 (Normal Mode Operation)); in the second cycle, $\overline{CS}$ must be brought high before the 10th ADSCLK edge but after the second ADSCLK falling edge (see Figure 81 (Entering Partial Power-Down Mode)). Alternatively, if it is intended to place the part in full power-down mode when the supplies are applied, then three dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th ADSCLK falling edge (see Figure 80 (Normal Mode Operation)); the second and third dummy cycles place the part in full power-down (see Figure 83 (Entering Full Power-Down Mode)).

Once supplies are applied to the ADC, enough time must be allowed for any external reference to power up and charge the various reference buffer decoupling capacitors to their final values.

Power vs. Throughput Rate

The power consumption of the ADC varies with the throughput rate. When using very slow throughput rates and as fast an ADSCLK frequency as possible, the various power-down options can be used to make significant power savings. However, the ADC quiescent current is low enough that even without using the power-down options, there is a noticeable variation in power consumption with sampling rate. This is true whether a fixed ADSCLK value is used or if it is scaled with the sampling rate. Figure 85 (Power vs. Throughput in Normal Mode with VDD = 3 V) and Figure 86 (Power vs. Throughput in Normal Mode with VDD = 5 V) show plots of power vs. the throughput rate when operating in normal mode for a fixed

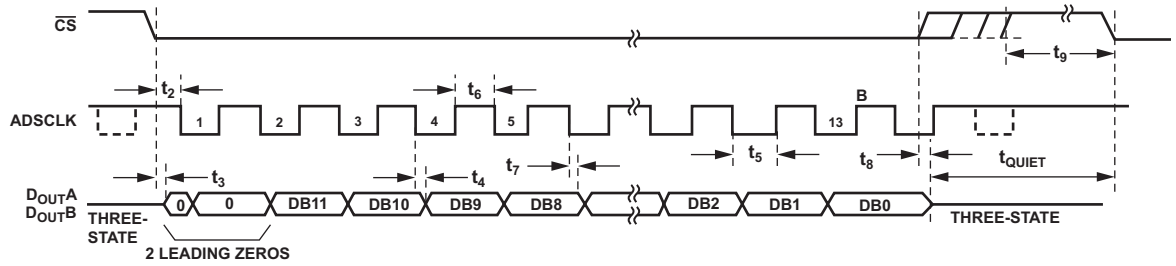


Figure 87. Serial Interface Timing Diagram

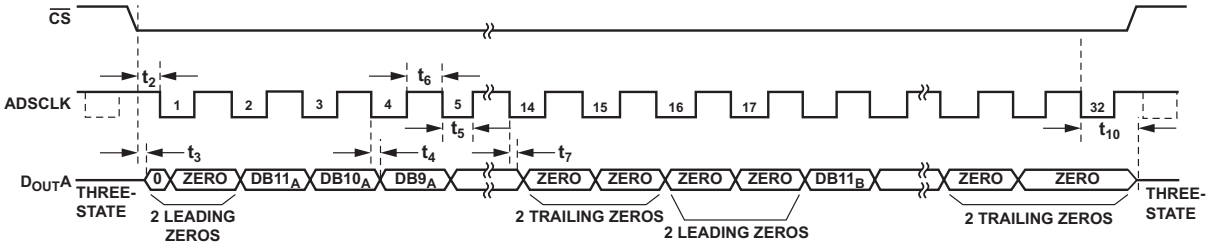


Figure 88. Reading Data from Both ADCs on One D_{OUT} Line with 32 ADSCLKs

Table 55. 120-Lead LQFP Lead Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	V_{DDEXT}	31	PG3	61	V_{DDINT}	91	V_{B2}
2	PF2	32	PG4	62	V_{DDEXT}	92	V_{B1}
3	PF4	33	TDI	63	$V_{DDFLASH}$	93	AGND
4	PF3	34	TCK	64	V_{DDEXT}	94	$D_{CAP}B$
5	PF5	35	TMS	65	V_{DDINT}	95	RANGE
6	V_{DDEXT}	36	TDO	66	V_{DDEXT}	96	SGL/$\overline{DIFF}$
7	PF6	37	$\overline{TRST}$	67	V_{DDEXT}	97	A2
8	PF7	38	PG5	68	$\overline{EMU}$	98	A1
9	PF8	39	PG6	69	$V_{DDFLASH}$	99	AGND
10	PF9	40	PG7	70	EXT_WAKE	100	A0
11	$\overline{NMI}$	41	V_{DDEXT}	71	$\overline{PG}$	101	$\overline{CS}$
12	$\overline{RESET}$	42	V_{DDINT}	72	NC	102	ADSCLK
13	GND	43	PG8	73	AGND	103	$D_{OUT}B$
14	PF10	44	PG9	74	DGND	104	DGND
15	V_{DDEXT}	45	PG10	75	REF_SELECT	105	$D_{OUT}A$
16	PF11	46	PG11	76	AV_{DD}	106	V_{DRIVE}
17	GND	47	PG12	77	$D_{CAP}A$	107	DV_{DD}
18	PF12	48	PG13	78	AGND	108	GND
19	PF13	49	PG14	79	AGND	109	GND
20	V_{DDEXT}	50	PG15	80	V_{A1}	110	CLKIN
21	PF14	51	V_{DDEXT}	81	V_{A2}	111	XTAL
22	PF15	52	V_{DDINT}	82	AGND	112	V_{DDEXT}
23	V_{DDEXT}	53	V_{DDINT}	83	V_{A3}	113	PH0
24	V_{DDINT}	54	SDA	84	V_{A4}	114	PH2
25	$V_{DDFLASH}$	55	SCL	85	V_{A5}	115	PH1
26	V_{DDEXT}	56	BMODE2	86	V_{A6}	116	V_{DDEXT}
27	PG0	57	BMODE1	87	V_{B6}	117	V_{DDINT}
28	PG1	58	BMODE0	88	V_{B5}	118	PF0
29	PG2	59	V_{DDEXT}	89	V_{B4}	119	PF1
30	V_{DDEXT}	60	NC	90	V_{B3}	120	EXTCLK
						121*	GND
						122**	AGND

* Pin no. 121 is the GND supply (see Figure 89 and Figure 90) for the processor (4.6mm × 6.17mm); this pad **must** connect to GND.
** Pin no. 122 is the AGND supply (see Figure 89 and Figure 90) for the ADC (2.81mm × 2.81mm); this pad **must** connect to AGND.

OUTLINE DIMENSIONS

Dimensions in Figure 93 (for the 120-lead LQFP) and in Figure 94 (for the 88-lead LFCSP) are shown in millimeters.

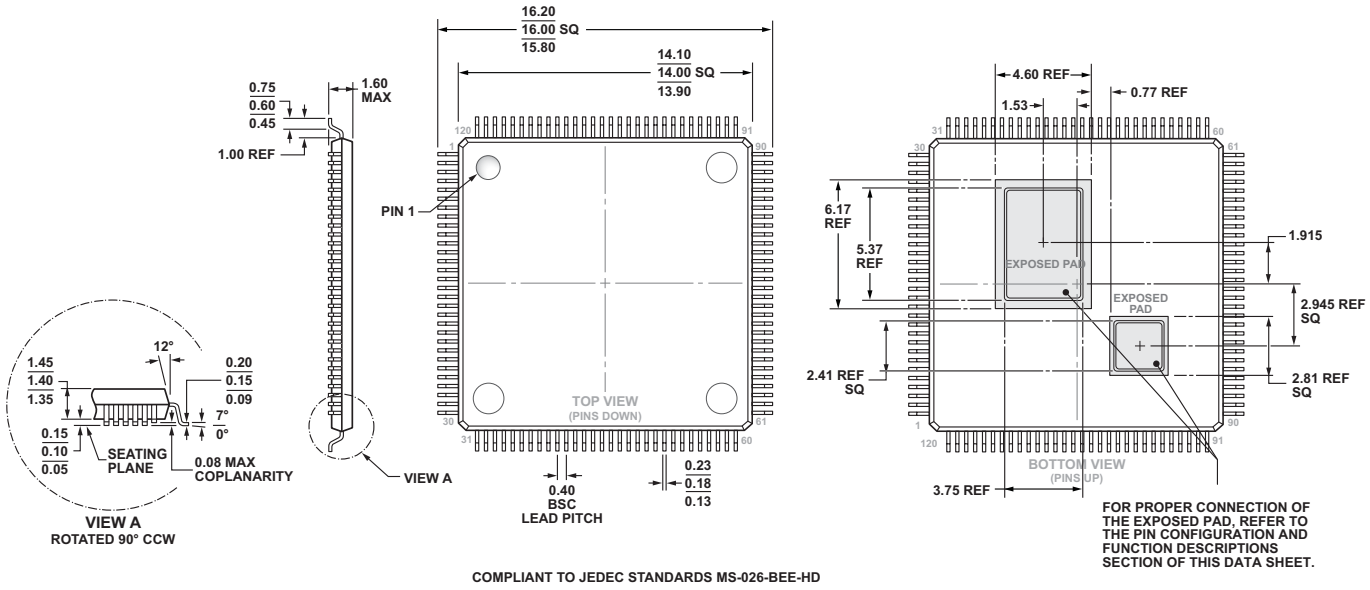


Figure 93. 120-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP][1]
(SW-120-2)
Dimensions shown in millimeters

[1] For information relating to the SW-120-2 package's exposed pad, see the table endnote on Page 74.