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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | - |
| Interface | - |
| Clock Rate | - |
| Non-Volatile Memory | - |
| On-Chip RAM | - |
| Voltage - I/O | - |
| Voltage - Core | - |
| Operating Temperature | - |
| Mounting Type | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-bf506kswz-4f |

# GENERAL DESCRIPTION

The ADSP-BF50x processors are members of the Blackfin® family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF50x processors are completely code compatible with other Blackfin processors. ADSP-BF50x processors offer performance up to 400 MHz and reduced static power consumption. Differences with respect to peripheral combinations are shown in Table 1.

**Table 1. Processor Comparison**

| Feature | | ADSP-BF504 | ADSP-BF504F | ADSP-BF506F |
|---|---|---|---|---|
| Up/Down/Rotary Counters | | 2 | 2 | 2 |
| Timer/Counters with PWM | | 8 | 8 | 8 |
| 3-Phase PWM Units | | 2 | 2 | 2 |
| SPORTs | | 2 | 2 | 2 |
| SPIs | | 2 | 2 | 2 |
| UARTs | | 2 | 2 | 2 |
| Parallel Peripheral Interface | | 1 | 1 | 1 |
| Removable Storage Interface | | 1 | 1 | 1 |
| CAN | | 1 | 1 | 1 |
| TWI | | 1 | 1 | 1 |
| Internal 32M Bit Flash | | – | 1 | 1 |
| ADC Control Module (ACM) | | 1 | 1 | 1 |
| Internal ADC | | – | – | 1 |
| GPIOs | | 35 | 35 | 35 |
| Memory (bytes) | L1 Instruction SRAM | 16K | 16K | 16K |
| | L1 Instruction SRAM/Cache | 16K | 16K | 16K |
| | L1 Data SRAM | 16K | 16K | 16K |
| | L1 Data SRAM/Cache | 16K | 16K | 16K |
| | L1 Scratchpad | 4K | 4K | 4K |
| | L3 Boot ROM | 4K | 4K | 4K |
| Maximum Speed Grade[1] | | 400 MHz | | |
| Maximum System Clock Speed | | 100 MHz | | |
| Package Options | | 88-Lead LFCSP | 88-Lead LFCSP | 120-Lead LQFP |

[1] For valid clock combinations, see Table 14, Table 15, Table 16, and Table 24.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

## PORTABLE LOW-POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which provides the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

## SYSTEM INTEGRATION

The ADSP-BF50x processors are highly integrated system-on-a-chip solutions for the next generation of embedded industrial, instrumentation, and power/motion control applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include a watchdog timer; two 32-bit up/down counters with rotary support; eight 32-bit timers/counters with PWM support; six pairs of 3-phase 16-bit center-based PWM units; two dual-channel, full-duplex synchronous serial ports (SPORTs); two serial peripheral interface (SPI) compatible ports; two UARTs with IrDA® support; a parallel peripheral interface (PPI); a removable storage interface (RSI) controller; an internal ADC with 12 channels, 12 bits, up to 2 MSPS, and ACM controller; a controller area network (CAN) controller; a 2-wire interface (TWI) controller; and an internal 32M bit flash.

## PROCESSOR PERIPHERALS

The ADSP-BF50x processors contain a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). These Blackfin processors contain high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The SPORT, SPI, UART, PPI, and RSI peripherals are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including boot ROM and internal 32M bit synchronous burst flash. Multiple on-chip buses running at up to 100 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF50x processors include an interface to an off-chip voltage regulator in support of the processor's dynamic power management capability.

## BLACKFIN PROCESSOR CORE

As shown in Figure 2, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo $2^{32}$ multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If the second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

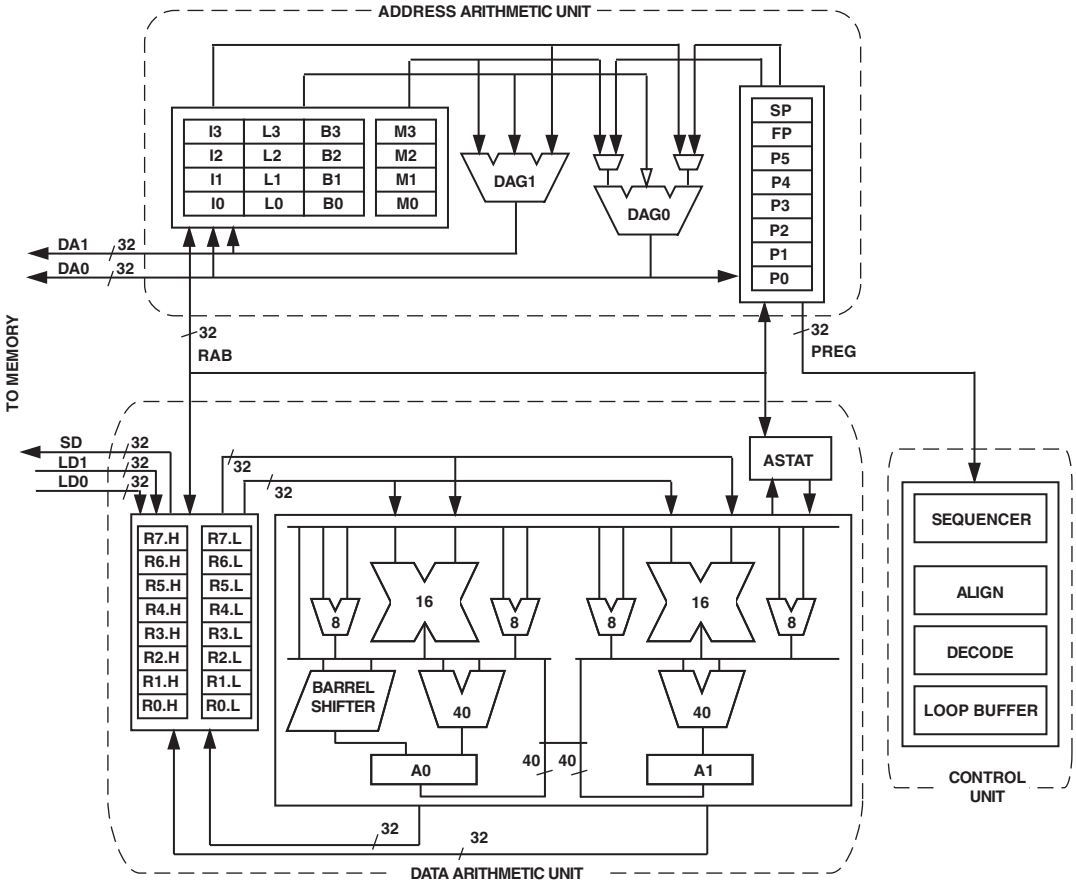


*Figure 2. Blackfin Processor Core*

## FLASH MEMORY

The ADSP-BF504F and ADSP-BF506F processors include an on-chip 32M bit (×16, multiple bank, burst) Flash memory. The features of this memory include:

- Synchronous/asynchronous read
  - Synchronous burst read mode: 50 MHz
  - Asynchronous/synchronous read mode
  - Random access times: 70 ns
- Synchronous burst read suspend
- Memory blocks
  - Multiple bank memory array: 4M bit banks
  - Parameter blocks (top location)
- Dual operations
  - Program erase in one bank while read in others
  - No delay between read and write operations
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked or locked down
- Security
  - 128-bit user programmable OTP cells
  - 64-bit unique device number
- Common Flash interface (CFI)
- 100,000 program/erase cycles per block

Flash memory ships from the factory in an erased state *except* for block 0 of the parameter bank. Block 0 of the Flash memory parameter bank ships from the factory in an unknown state. An erase operation should be performed prior to programming this block.

## DMA CONTROLLERS

The processor has multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interface. DMA-capable peripherals include the SPORTs, SPI ports, UARTs, RSI, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The processor DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the processor DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels, which are provided for transfers between the various memories of the processor system with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

## WATCHDOG TIMER

The processor includes a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a core and system reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine whether the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK) at a maximum frequency of $f_{SCLK}$.

## TIMERS

There are nine general-purpose programmable timer units in the processors. Eight timers have an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF pins, to an external clock input to the PPI_CLK input pin, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

## UP/DOWN COUNTERS AND THUMBWHEEL INTERFACES

Two 32-bit up/down counters are provided that can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. The counters can also operate in general-purpose up/down count modes. Then, count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three pins have a programmable debouncing circuit.

Internal signals forwarded to each timer unit enable these timers to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

## 3-PHASE PWM UNITS

The two/dual 3-phase PWM generation units each feature:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single/double update modes
- Programmable dead time and switching frequency
- Twos-complement implementation which permits smooth transition to full ON and full OFF states
- Possibility to synchronize the PWM generation to either externally-generated or internally-generated synchronization pulses
- Special provisions for BDCM operation (crossover and output enable functions)
- Wide variety of special switched reluctance (SR) operating modes
- Output polarity and clock gating control
- Dedicated asynchronous PWM shutdown signal

Each PWM block integrates a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction motor (ACIM) or permanent magnet synchronous motor (PMSM) control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM) or brushless dc motor (BDCM). Software can enable a special mode for switched reluctance motors (SRM).

The six PWM output signals (per PWM unit) consist of three high-side drive signals (PWMx_AH, PWMx_BH, and PWMx_CH) and three low-side drive signals (PWMx_AL, PWMx_BL, and PWMx_CL). The polarity of the generated PWM signal can be set with software, so that either active HI or active LO PWM patterns can be produced.

The switching frequency of the generated PWM pattern is programmable using the 16-bit PWM_TM register. The PWM generator can operate in single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period, so that the resultant PWM patterns are symmetrical about the midpoint of the PWM period. In the double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

Pulses synchronous to the switching frequency can be generated internally and output on the PWMx_SYNC pin. The PWM unit can also accept externally generated synchronization pulses through PWMx_SYNC.

Each PWM unit features a dedicated asynchronous shutdown pin, $\overline{\text{PWMx\_TRIP}}$, which (when brought low) instantaneously places all six PWM outputs in the OFF state.

## SERIAL PORTS

The processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- $I^2S$ capable operation.
- Bidirectional operation—Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of $I^2S$ stereo audio.
- Buffered (8-deep) transmit and receive ports—Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking—Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from ($f_{SCLK}$/131,070) Hz to ($f_{SCLK}$/2) Hz.
- Word length—Each SPORT supports serial data words from 3 to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing—Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware—Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

### *EZ-KIT Lite Evaluation Board*

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

### *EZ-KIT Lite Evaluation Kits*

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

### *Software Add-Ins for CrossCore Embedded Studio*

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

### *Board Support Packages for Evaluation Hardware*

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

### *Middleware Packages*

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

### *Algorithmic Modules*

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

### *Designing an Emulator-Compatible DSP Board (Target)*

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

## ADC AND ACM INTERFACE

This section describes the ADC and ACM interface. System designers should also consult the *ADSP-BF50x Blackfin Processor Hardware Reference* for additional information.

The ADC control module (ACM) provides an interface that synchronizes the controls between the processor and the internal analog-to-digital converter (ADC) module. The ACM is available on the ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors, and the ADC is available on the ADSP-BF506F processor only. The analog-to-digital conversions are initiated by the processor, based on external or internal events.

The ACM allows for flexible scheduling of sampling instants and provides precise sampling signals to the ADC.

## ADC APPLICATION HINTS

The following sections provide application hints for using the ADC.

### *Grounding and Layout Considerations*

The analog and digital supplies to the ADC are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the ADC should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All AGND pins should be sunk in the AGND plane. Digital and analog ground planes should be joined in only one place. If the ADC is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the ground pins on the ADC.

Avoid running digital lines under the device as this couples noise onto the die. Avoid running digital lines in the area of the AGND pad as this couples noise onto the ADC die and into the AGND plane. The power supply lines to the ADC should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feed through within the board, traces on opposite sides of the board should run at right angles to each other.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

## ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF50x processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF50x Blackfin Processor Hardware Reference* (volumes 1 and 2)
- *Blackfin Processor Programming Reference*
- *ADSP-BF50x Blackfin Processor Anomaly List*

## RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http:\\www.analog.com\signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

# SIGNAL DESCRIPTIONS

Signal definitions for the ADSP-BF50x processors are listed in Table 11. All pins for the ADC (ADSP-BF506F processor only) are listed in Table 12.

In order to maintain maximum function and reduce package size and pin count, some pins have multiple, multiplexed functions. In cases where pin function is reconfigurable, the default state is shown in plain text, while the alternate functions are shown in italics.

During and immediately after reset, all processor signals (not ADC signals) are three-stated with the following exceptions: EXT_WAKE is driven high and XTAL is driven in conjunction with CLKIN to create a crystal oscillator circuit. During hibernate, all signals are three-stated with the following exceptions: EXT_WAKE is driven low and XTAL is driven to a solid logic level.

During and immediately after reset, all I/O pins have their input buffers disabled until enabled by user software with the exception of the pins that need pull-ups or pull-downs, as noted in Table 11.

Adding a parallel termination to CLKOUT may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

**Table 11. Processor—Signal Descriptions**

| Signal Name | Type | Function | Driver Type |
|---|---|---|---|
| Port F: *GPIO and Multiplexed Peripherals* | | | |
| PF0/*TSCLK0/UA0_RX/TMR6/CUD0* | I/O | GPIO/*SPORT0 TX Serial CLK/UART0 RX/Timer6/Count Up Dir 0* | C |
| PF1/*RSCLK0/UA0_TX/TMR5/CDG0* | I/O | GPIO/*SPORT0 RX Serial CLK/UART0 TX/Timer5/Count Down Dir 0* | C |
| PF2/*DT0PRI/PWM0_BH/PPI_D8/CZM0* | I/O | GPIO/*SPORT0 TX Pri Data/PWM0 Drive B Hi/PPI Data 8/Counter Zero Marker 0* | C |
| PF3/*TFS0/PWM0_BL/PPI_D9/CDG0* | I/O | GPIO/*SPORT0 TX Frame Sync/PWM0 Drive B Lo/PPI Data 9/Count Down Dir 0* | C |
| PF4/*RFS0/PWM0_CH/PPI_D10/TACLK0* | I/O | GPIO/*SPORT0 RX Frame Sync/PWM0 Drive C Hi/PPI Data 10/Alt Timer CLK 0* | C |
| PF5/*DR0PRI/PWM0_CL/PPI_D11/TACLK1* | I/O | GPIO/*SPORT0 Pri RX Data/PWM0 Drive C Lo/PPI Data 11/Alt Timer CLK 1* | C |
| PF6/*UA1_TX/$\overline{\text{PWM0\_TRIP}}$/PPI_D12* | I/O | GPIO/*UART1 TX/PWM0 TRIP/PPI Data 12* | C |
| PF7/*UA1_RX/PWM0_SYNC/PPI_D13/TACI3* | I/O | GPIO/*UART1 RX/PWM0 SYNC/PPI Data 13/Alt Capture In 3* | C |
| PF8/*$\overline{\text{UA1\_RTS}}$/DT0SEC/PPI_D7* | I/O | GPIO/*UART1 RTS/SPORT0 TX Sec Data/PPI Data 7* | C |
| PF9/*$\overline{\text{UA1\_CTS}}$/DR0SEC/PPI_D6/CZM0* | I/O | GPIO/*UART1 CTS/SPORT0 Sec RX Data/PPI Data 6/Counter Zero Marker 0* | C |
| PF10/*SPI0_SCK/TMR2/PPI_D5* | I/O | GPIO/*SPI0 SCK/Timer2/PPI Data 5* | C |
| PF11/*SPI0_MISO/$\overline{\text{PWM0\_TRIP}}$/PPI_D4/TACLK2* | I/O | GPIO/*SPI0 MISO/PWM0 TRIP/PPI Data 4/Alt Timer CLK 2* | C |
| PF12/*SPI0_MOSI/PWM0_SYNC/PPI_D3* | I/O | GPIO/*SPI0 MOSI/PWM0 SYNC/PPI Data 3* | C |
| PF13/*$\overline{\text{SPI0\_SEL1}}$/TMR3/PPI_D2/$\overline{\text{SPI0\_SS}}$* | I/O | GPIO/*SPI0 Slave Select 1/Timer3/PPI Data 2/SPI0 Slave Select In* | C |
| PF14/*$\overline{\text{SPI0\_SEL2}}$/PWM0_AH/PPI_D1* | I/O | GPIO/*SPI0 Slave Select 2/PWM0 AH/PPI Data 1* | C |
| PF15/*$\overline{\text{SPI0\_SEL3}}$/PWM0_AL/PPI_D0* | I/O | GPIO/*SPI0 Slave Select 3/PWM0 AL/PPI Data 0* | C |
| Port G: *GPIO and Multiplexed Peripherals* | | | |
| PG0/*$\overline{\text{SPI1\_SEL3}}$/TMRCLK/PPI_CLK/UA1_RX/TACI4* | I/O | GPIO/*SPI1 Slave Select 3/Timer CLK/PPI Clock/UART1 RX/Alt Capture In 4* | C |
| PG1/*$\overline{\text{SPI1\_SEL2}}$/PPI_FS3/CAN_RX/TACI5* | I/O | GPIO/*SPI1 Slave Select 2/PPI FS3/CAN RX/Alt Capture In 5* | C |
| PG2/*$\overline{\text{SPI1\_SEL1}}$/TMR4/CAN_TX/$\overline{\text{SPI1\_SS}}$* | I/O | GPIO/*SPI1 Slave Select 1/Timer4/CAN TX/SPI1 Slave Select In* | C |
| PG3/*HWAIT/SPI1_SCK/DT1SEC/UA1_TX* | I/O | GPIO/*HWAIT/SPI1 SCK/SPORT1 TX Sec Data/UART1 TX* | C |
| PG4/*SPI1_MOSI/DR1SEC/PWM1_SYNC/TACLK6* | I/O | GPIO/*SPI1 MOSI/SPORT1 Sec RX Data/PWM1 SYNC/Alt Timer CLK 6* | C |
| PG5/*SPI1_MISO/TMR7/$\overline{\text{PWM1\_TRIP}}$* | I/O | GPIO/*SPI1 MISO/Timer7/PWM1 TRIP* | C |
| PG6/*ACM_SGLDIFF/SD_D3/PWM1_AH* | I/O | GPIO/*ADC CM SGL DIFF/SD Data 3/PWM1 Drive A Hi* | C |
| PG7/*ACM_RANGE/SD_D2/PWM1_AL* | I/O | GPIO/*ADC CM RANGE/SD Data 2/PWM1 Drive A Lo* | C |
| PG8/*DR1SEC/SD_D1/PWM1_BH* | I/O | GPIO/*SPORT1 Sec RX Data/SD Data 1/PWM1 Drive B Hi* | C |
| PG9/*DR1PRI/SD_D0/PWM1_BL* | I/O | GPIO/*SPORT1 Pri RX Data/SD Data 0/PWM1 Drive B Lo* | C |
| PG10/*RFS1/SD_CMD/PWM1_CH/TACI6* | I/O | GPIO/*SPORT1 RX Frame Sync/SD CMD/PWM1 Drive C Hi/Alt Capture In 6* | C |
| PG11/*RSCLK1/SD_CLK/PWM1_CL/TACLK7* | I/O | GPIO/*SPORT1 RX Serial CLK/SD CLK/PWM1 Drive C Lo/Alt Timer CLK 7* | C |
| PG12/*UA0_RX/SD_D4/PPI_D15/TACI2* | I/O | GPIO/*UART0 RX/SD Data 4/PPI Data 15/Alt Capture In 2* | C |
| PG13/*UA0_TX/SD_D5/PPI_D14/CZM1* | I/O | GPIO/*UART0 TX/SD Data 5/PPI Data 14/Counter Zero Marker 1* | C |

**Table 12. ADC—Signal Descriptions (ADSP-BF506F Processor Only) (Continued)**

| Signal Name | Type | Function |
|---|---|---|
| $D_{OUT}A$, $D_{OUT}B$ | O | Serial Data Outputs. The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the ADSCLK input and 14 ADSCLKs are required to access the data. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data stream consists of two leading zeros followed by the 12 bits of conversion data. The data is provided MSB first. If $\overline{CS}$ is held low for 16 ADSCLK cycles rather than 14, then two trailing zeros will appear after the 12 bits of data. If $\overline{CS}$ is held low for a further 16 ADSCLK cycles on either $D_{OUT}A$ or $D_{OUT}B$, the data from the other ADC follows on the $D_{OUT}$ pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either $D_{OUT}A$ or $D_{OUT}B$ using only one serial port. For more information, see the ADC—Serial Interface section. |
| $V_{DRIVE}$ | P | Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the digital I/O interface operates. This pin should be decoupled to DGND. The voltage at this pin may be different than that at $AV_{DD}$ and $DV_{DD}$ but should never exceed either by more than 0.3 V. |
| $DV_{DD}$ | P | Digital Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for all digital circuitry on the internal ADC. The $DV_{DD}$ and $AV_{DD}$ voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND. |

# SPECIFICATIONS

Specifications are subject to change without notice.

## OPERATING CONDITIONS

| Parameter | | Conditions | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDINT}$ | Internal Supply Voltage | Industrial Models | 1.14 | | 1.47 | V |
| | Internal Supply Voltage | Commercial Models | 1.10 | | 1.47 | V |
| | Internal Supply Voltage | Automotive Models | 1.33 | | 1.47 | V |
| $V_{DDEXT}$[1, 2] | External Supply Voltage | 1.8 V I/O, ADSP-BF504, Nonautomotive and Non Flash Models | 1.7 | 1.8 | 1.9 | V |
| | External Supply Voltage | 2.5 V I/O, ADSP-BF504, Nonautomotive and Non Flash Models | 2.25 | 2.5 | 2.75 | V |
| | External Supply Voltage | 3.3 V I/O, ADSP-BF50x, All Models | 2.7 | 3.3 | 3.6 | V |
| $V_{DDFLASH}$[1, 3] | Flash Memory Supply Voltage | | 1.7 | 1.8 | 2.0 | V |
| $V_{IH}$ | High Level Input Voltage[4, 5] | $V_{DDEXT}$ = 1.90 V | 1.2 | | | V |
| | High Level Input Voltage[4, 6] | $V_{DDEXT}$ = 2.75 V | 1.7 | | | V |
| | High Level Input Voltage[4, 6] | $V_{DDEXT}$ = 3.6 V | 2.0 | | | V |
| $V_{IHTWI}$ | High Level Input Voltage[5] | $V_{DDEXT}$ = 1.90 V/2.75 V/3.6 V | 0.7 × $V_{BUSTWI}$[7, 8] | | $V_{BUSTWI}$[7, 8] | V |
| $V_{IL}$ | Low Level Input Voltage[4, 5] | $V_{DDEXT}$ = 1.7 V | | | 0.6 | V |
| | Low Level Input Voltage[4, 6] | $V_{DDEXT}$ = 2.25 V | | | 0.7 | V |
| | Low Level Input Voltage[4, 6] | $V_{DDEXT}$ = 3.0 V | | | 0.8 | V |
| $V_{ILTWI}$ | Low Level Input Voltage[5] | $V_{DDEXT}$ = minimum | | | 0.3 × $V_{BUSTWI}$[8] | V |
| $T_J$ | Junction Temperature | 88-Lead LFCSP @ $T_{AMBIENT}$ = –40°C to +85°C | –40 | | +105 | °C |
| | Junction Temperature | 88-Lead LFCSP @ $T_{AMBIENT}$ = 0°C to +70°C | 0 | | +90 | °C |
| | Junction Temperature | 120-Lead LQFP @ $T_{AMBIENT}$ = –40°C to +85°C | –40 | | +105 | °C |
| | Junction Temperature | 120-Lead LQFP @ $T_{AMBIENT}$ = 0°C to +70°C | 0 | | +90 | °C |
| | Junction Temperature | 88-Lead LFCSP @ $T_{AMBIENT}$ = –40°C to +105°C | –40 | | +125 | °C |

[1] Must remain powered (even if the associated function is not used).
[2] 1.8 V and 2.5 V I/O are supported only on ADSP-BF504 nonautomotive models. All ADSP-BF50x flash and automotive models support 3.3 V I/O only.
[3] For ADSP-BF504, $V_{DDFLASH}$ pins should be connected to GND.
[4] Parameter value applies to all input and bidirectional pins, except SDA and SCL.
[5] Bidirectional pins (PF15–0, PG15–0, PH15–0) and input pins (TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF50x processors are 2.5 V tolerant (always accept up to 2.7 V maximum $V_{IH}$). Voltage compliance (on outputs, $V_{OH}$) is limited by the $V_{DDEXT}$ supply voltage.
[6] Bidirectional pins (PF15–0, PG15–0, PH2–0) and input pins (TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF50x processors are 3.3 V tolerant (always accept up to 3.6 V maximum $V_{IH}$). Voltage compliance (on outputs, $V_{OH}$) is limited by the $V_{DDEXT}$ supply voltage.
[7] The $V_{IHTWI}$ min and max value vary with the selection in the TWI_DT field of the NONGPIO_DRIVE register. See $V_{BUSTWI}$ min and max values in Table 13.
[8] SDA and SCL are pulled up to $V_{BUSTWI}$. See Table 13.

Table 13 shows settings for TWI_DT in the NONGPIO_DRIVE register. Set this register prior to using the TWI port.

**Table 13. TWI_DT Field Selections and $V_{DDEXT}$/$V_{BUSTWI}$**

| TWI_DT | $V_{DDEXT}$ Nominal | $V_{BUSTWI}$ Minimum | $V_{BUSTWI}$ Nominal | $V_{BUSTWI}$ Maximum | Unit |
|---|---|---|---|---|---|
| 000 (default) | 3.3 | 2.97 | 3.3 | 3.63 | V |
| 001 | 1.8 | 1.7 | 1.8 | 1.98 | V |
| 010 | 2.5 | 2.97 | 3.3 | 3.63 | V |
| 011 | 1.8 | 2.97 | 3.3 | 3.63 | V |
| 100 | 3.3 | 4.5 | 5 | 5.5 | V |
| 101 | 1.8 | 2.25 | 2.5 | 2.75 | V |
| 110 | 2.5 | 2.25 | 2.5 | 2.75 | V |
| 111 (reserved) | — | — | — | — | — |

## PROCESSOR—TIMING SPECIFICATIONS

Specifications subject to change without notice.

### *Clock and Reset Timing*

Table 24 and Figure 10 describe clock and reset operations. Per the CCLK and SCLK timing specifications in Table 14 to Table 16, combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of the processor's speed grade. Table 25 and Figure 11 describe clock out timing.

**Table 24. Clock and Reset Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $f_{CKIN}$ | CLKIN Frequency[1, 2, 3, 4] (Commercial/Industrial Models) | 12 | 50 | MHz |
| | CLKIN Frequency[1, 2, 3, 4] (Automotive Models) | 14 | 50 | MHz |
| $t_{CKINL}$ | CLKIN Low Pulse[1] | 10 | | ns |
| $t_{CKINH}$ | CLKIN High Pulse[1] | 10 | | ns |
| $t_{WRST}$ | $\overline{\text{RESET}}$ Asserted Pulse Width Low[5] | $11 \times t_{CKIN}$ | | ns |
| *Switching Characteristic* | | | | |
| $t_{BUFDLAY}$ | CLKIN to CLKBUF[6] Delay | | 11 | ns |

[1] Applies to PLL bypass mode and PLL non bypass mode.

[2] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed $f_{VCO}$, $f_{CCLK}$, and $f_{SCLK}$ settings discussed in Table 14 on Page 27 through Table 16 on Page 27.

[3] The $t_{CKIN}$ period (see Figure 10) equals $1/f_{CKIN}$.

[4] If the DF bit in the PLL_CTL register is set, the minimum $f_{CKIN}$ specification is 24 MHz for commercial/industrial models and 28 MHz for automotive models.

[5] Applies after power-up sequence is complete. See Table 26 and Figure 12 for power-up reset timing.

[6] The ADSP-BF504/ADSP-BF504F/ADSP-BF506F processor does not have a dedicated CLKBUF pin. Rather, the EXTCLK pin may be programmed to serve as CLKBUF or CLKOUT. This parameter applies when EXTCLK is programmed to output CLKBUF.

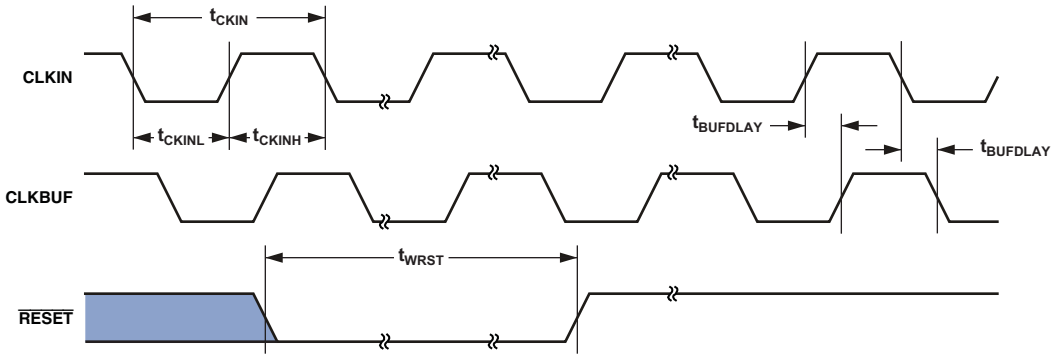


*Figure 10. Clock and Reset Timing*

**Table 33. Serial Ports — External Late Frame Sync**

| Parameter | | $V_{DDEXT}$ = 1.8 V Min | $V_{DDEXT}$ = 1.8 V Max | $V_{DDEXT}$ = 2.5 V/3.3 V Min | $V_{DDEXT}$ = 2.5 V/3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Switching Characteristics* | | | | | | |
| $t_{DDTLFSE}$ | Data Delay from Late External TFSx or External RFSx in Multi-channel Mode With MFD = 0[1, 2] | | 12.0 | | 10.0 | ns |
| $t_{DTENLFSE}$ | Data Enable from External RFSx in Multi-channel Mode With MFD = 0[1, 2] | 0.0 | | 0.0 | | ns |

[1] When in multi-channel mode, TFSx enable and TFSx valid follow $t_{DTENLFSE}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$ then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFSE}$ apply.

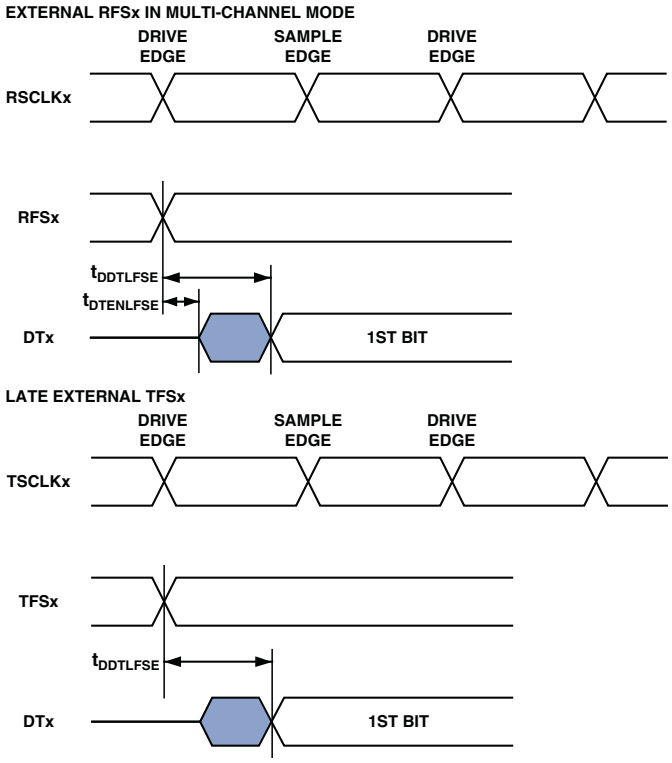


*Figure 22. Serial Ports — External Late Frame Sync*

required acquisition time for the next sampling instant at Point B; therefore, the analog inputs are configured as differential for that conversion.

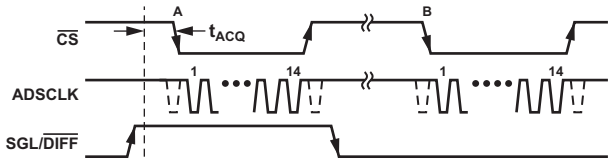


*Figure 77. Selecting Differential or Single-Ended Configuration*

The channels used for simultaneous conversions are selected via the multiplexer address input pins, A0 to A2. The logic states of these pins also need to be established prior to the acquisition time; however, they may change during the conversion time provided the mode is not changed. If the mode is changed from fully differential to pseudo differential, for example, then the acquisition time would start again from this point. The selected input channels are decoded as shown in Table 53 (Analog Input Type and Channel Selection).

The analog input range of the ADC can be selected as 0 V to $V_{REF}$ or 0 V to 2 × $V_{REF}$ via the RANGE pin. This selection is made in a similar fashion to that of the SGL/$\overline{DIFF}$ pin by setting the logic state of the RANGE pin a time $t_{acq}$ prior to the falling edge of $\overline{CS}$. Subsequent to this, the logic level on this pin can be altered after the third falling edge of ADSCLK. If this pin is tied to a logic low, the analog input range selected is 0 V to $V_{REF}$. If this pin is tied to a logic high, the analog input range selected is 0 V to 2 × $V_{REF}$.

### Output Coding

The ADC output coding is set to either twos complement or straight binary, depending on which analog input configuration is selected for a conversion. Table 52 (ADC Output Coding) shows which output coding scheme is used for each possible analog input configuration.

### Transfer Functions

The designed code transitions occur at successive integer LSB values (1 LSB, 2 LSB, and so on). In single-ended mode, the LSB size is $V_{REF}$/4096 when the 0 V to $V_{REF}$ range is used, and the LSB size is 2 × $V_{REF}$/4096 when the 0 V to 2 × $V_{REF}$ range is used. In differential mode, the LSB size is 2 × $V_{REF}$ /4096 when the 0 V to $V_{REF}$ range is used, and the LSB size is 4 × $V_{REF}$/4096 when the 0 V to 2 × $V_{REF}$ range is used. The ideal transfer characteristic for the ADC when straight binary coding is output is shown in Figure 78 (Straight Binary Transfer Characteristic), and the ideal transfer characteristic for the ADC when twos complement coding is output is shown in Figure 79 (Twos Complement Transfer Characteristic with VREF ± VREF Input Range) (this is shown with the 2 × $V_{REF}$ range).

**Table 52. ADC Output Coding**

| SGL/$\overline{DIFF}$ | | RANGE | | Output Coding |
|---|---|---|---|---|
| 0 | (Differential Input) | 0 | (0 V to $V_{REF}$) | Twos complement |
| 0 | (Differential Input) | 1 | (0 V to 2 × $V_{REF}$) | Twos complement |
| 1 | (Single-Ended Input) | 0 | (0 V to $V_{REF}$) | Straight binary |
| 1 | (Single-Ended Input) | 1 | (0 V to2 × $V_{REF}$) | Twos complement |
| 0 | (Pseudo-Differential Input) | 0 | (0 V to $V_{REF}$) | Straight binary |
| 0 | (Pseudo-Differential Input) | 1 | (0 V to 2 × $V_{REF}$) | Twos complement |

**Table 53. Analog Input Type and Channel Selection**

| | | | | ADC A | | ADC B | | |
|---|---|---|---|---|---|---|---|---|
| SGL/$\overline{DIFF}$ | A2 | A1 | A0 | $V_{IN+}$ | $V_{IN-}$ | $V_{IN+}$ | $V_{IN-}$ | Comment |
| 1 | 0 | 0 | 0 | $V_{A1}$ | AGND | $V_{B1}$ | AGND | Single ended |
| 1 | 0 | 0 | 1 | $V_{A2}$ | AGND | $V_{B2}$ | AGND | Single ended |
| 1 | 0 | 1 | 0 | $V_{A3}$ | AGND | $V_{B3}$ | AGND | Single ended |
| 1 | 0 | 1 | 1 | $V_{A4}$ | AGND | $V_{B4}$ | AGND | Single ended |
| 1 | 1 | 0 | 0 | $V_{A5}$ | AGND | $V_{B5}$ | AGND | Single ended |
| 1 | 1 | 0 | 1 | $V_{A6}$ | AGND | $V_{B6}$ | AGND | Single ended |
| 0 | 0 | 0 | 0 | $V_{A1}$ | $V_{A2}$ | $V_{B1}$ | $V_{B2}$ | Fully differential |
| 0 | 0 | 0 | 1 | $V_{A1}$ | $V_{A2}$ | $V_{B1}$ | $V_{B2}$ | Pseudo differential |
| 0 | 0 | 1 | 0 | $V_{A3}$ | $V_{A4}$ | $V_{B3}$ | $V_{B4}$ | Fully differential |
| 0 | 0 | 1 | 1 | $V_{A3}$ | $V_{A4}$ | $V_{B3}$ | $V_{B4}$ | Pseudo differential |
| 0 | 1 | 0 | 0 | $V_{A5}$ | $V_{A6}$ | $V_{B5}$ | $V_{B6}$ | Fully differential |
| 0 | 1 | 0 | 1 | $V_{A5}$ | $V_{A6}$ | $V_{B5}$ | $V_{B6}$ | Pseudo differential |

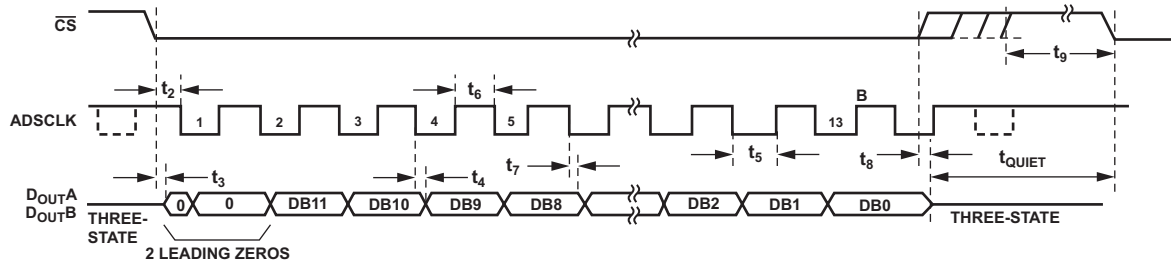


*Figure 87. Serial Interface Timing Diagram*

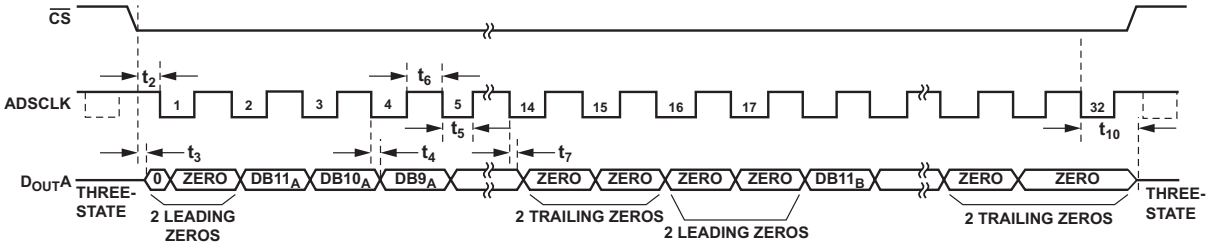


*Figure 88. Reading Data from Both ADCs on One $D_{OUT}$ Line with 32 ADSCLKs*

**Table 55. 120-Lead LQFP Lead Assignment (Numerical by Lead Number)**

| Lead No. | Signal | Lead No. | Signal | Lead No. | Signal | Lead No. | Signal |
|---|---|---|---|---|---|---|---|
| 1 | $V_{DDEXT}$ | 31 | PG3 | 61 | $V_{DDINT}$ | 91 | $V_{B2}$ |
| 2 | PF2 | 32 | PG4 | 62 | $V_{DDEXT}$ | 92 | $V_{B1}$ |
| 3 | PF4 | 33 | TDI | 63 | $V_{DDFLASH}$ | 93 | AGND |
| 4 | PF3 | 34 | TCK | 64 | $V_{DDEXT}$ | 94 | $D_{CAP}B$ |
| 5 | PF5 | 35 | TMS | 65 | $V_{DDINT}$ | 95 | RANGE |
| 6 | $V_{DDEXT}$ | 36 | TDO | 66 | $V_{DDEXT}$ | 96 | SGL/$\overline{DIFF}$ |
| 7 | PF6 | 37 | $\overline{TRST}$ | 67 | $V_{DDEXT}$ | 97 | A2 |
| 8 | PF7 | 38 | PG5 | 68 | $\overline{EMU}$ | 98 | A1 |
| 9 | PF8 | 39 | PG6 | 69 | $V_{DDFLASH}$ | 99 | AGND |
| 10 | PF9 | 40 | PG7 | 70 | EXT_WAKE | 100 | A0 |
| 11 | $\overline{NMI}$ | 41 | $V_{DDEXT}$ | 71 | $\overline{PG}$ | 101 | $\overline{CS}$ |
| 12 | $\overline{RESET}$ | 42 | $V_{DDINT}$ | 72 | NC | 102 | ADSCLK |
| 13 | GND | 43 | PG8 | 73 | AGND | 103 | $D_{OUT}B$ |
| 14 | PF10 | 44 | PG9 | 74 | DGND | 104 | DGND |
| 15 | $V_{DDEXT}$ | 45 | PG10 | 75 | REF_SELECT | 105 | $D_{OUT}A$ |
| 16 | PF11 | 46 | PG11 | 76 | $AV_{DD}$ | 106 | $V_{DRIVE}$ |
| 17 | GND | 47 | PG12 | 77 | $D_{CAP}A$ | 107 | $DV_{DD}$ |
| 18 | PF12 | 48 | PG13 | 78 | AGND | 108 | GND |
| 19 | PF13 | 49 | PG14 | 79 | AGND | 109 | GND |
| 20 | $V_{DDEXT}$ | 50 | PG15 | 80 | $V_{A1}$ | 110 | CLKIN |
| 21 | PF14 | 51 | $V_{DDEXT}$ | 81 | $V_{A2}$ | 111 | XTAL |
| 22 | PF15 | 52 | $V_{DDINT}$ | 82 | AGND | 112 | $V_{DDEXT}$ |
| 23 | $V_{DDEXT}$ | 53 | $V_{DDINT}$ | 83 | $V_{A3}$ | 113 | PH0 |
| 24 | $V_{DDINT}$ | 54 | SDA | 84 | $V_{A4}$ | 114 | PH2 |
| 25 | $V_{DDFLASH}$ | 55 | SCL | 85 | $V_{A5}$ | 115 | PH1 |
| 26 | $V_{DDEXT}$ | 56 | BMODE2 | 86 | $V_{A6}$ | 116 | $V_{DDEXT}$ |
| 27 | PG0 | 57 | BMODE1 | 87 | $V_{B6}$ | 117 | $V_{DDINT}$ |
| 28 | PG1 | 58 | BMODE0 | 88 | $V_{B5}$ | 118 | PF0 |
| 29 | PG2 | 59 | $V_{DDEXT}$ | 89 | $V_{B4}$ | 119 | PF1 |
| 30 | $V_{DDEXT}$ | 60 | NC | 90 | $V_{B3}$ | 120 | EXTCLK |
| | | | | | | 121* | GND |
| | | | | | | 122** | AGND |

* Pin no. 121 is the GND supply (see Figure 89 and Figure 90) for the processor (4.6mm × 6.17mm); this pad **must** connect to GND.
** Pin no. 122 is the AGND supply (see Figure 89 and Figure 90) for the ADC (2.81mm × 2.81mm); this pad **must** connect to AGND.

Figure 89 shows the top view of the 120-lead LQFP package lead configuration.

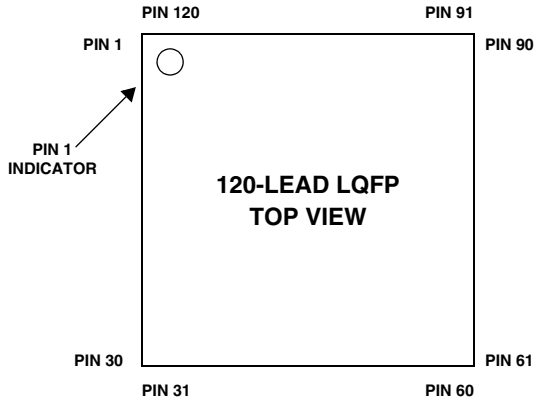


*Figure 89. 120-Lead LQFP Package Lead Configuration (Top View)*

Figure 90 shows the bottom view of the 120-lead LQFP package lead configuration.

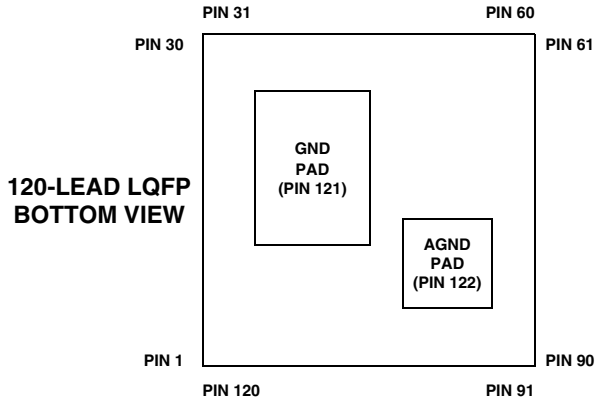


*Figure 90. 120-Lead LQFP Package Lead Configuration (Bottom View)*

# 88-LEAD LFCSP LEAD ASSIGNMENT

Table 56 lists the LFCSP leads by signal mnemonic. Table 57 on Page 77 lists the LFCSP by lead number.

**Table 56. 88-Lead LFCSP Lead Assignment (Alphabetical by Signal)**

| Signal | Lead No. | Signal | Lead No. | Signal | Lead No. | Signal | Lead No. |
|---|---|---|---|---|---|---|---|
| BMODE0 | 51 | PF4 | 82 | PG9 | 34 | $V_{DDEXT}$ | 20 |
| BMODE1 | 50 | PF5 | 83 | PG10 | 35 | $V_{DDEXT}$ | 31 |
| BMODE2 | 49 | PF6 | 85 | PG11 | 36 | $V_{DDEXT}$ | 41 |
| CLKIN | 68 | PF7 | 86 | PG12 | 37 | $V_{DDEXT}$ | 52 |
| $\overline{EMU}$ | 60 | PF8 | 87 | PG13 | 38 | $V_{DDEXT}$ | 54 |
| EXT_WAKE | 62 | PF9 | 88 | PG14 | 39 | $V_{DDEXT}$ | 56 |
| EXTCLK | 78 | PF10 | 4 | PG15 | 40 | $V_{DDEXT}$ | 58 |
| GND | 3 | PF11 | 6 | PH0 | 71 | $V_{DDEXT}$ | 59 |
| GND | 7 | PF12 | 8 | PH1 | 72 | $V_{DDEXT}$ | 70 |
| GND | 67 | PF13 | 9 | PH2 | 73 | $V_{DDEXT}$ | 74 |
| NC | 45 | PF14 | 11 | $\overline{RESET}$ | 2 | $V_{DDEXT}$ | 79 |
| NC | 46 | PF15 | 12 | SCL | 44 | $V_{DDEXT}$ | 84 |
| NC | 47 | $\overline{PG}$ | 63 | SDA | 43 | $V_{DDFLASH}$ | 15 |
| NC | 48 | PG0 | 17 | TCK | 24 | $V_{DDFLASH}$ | 55 |
| NC | 64 | PG1 | 18 | TDI | 23 | $V_{DDFLASH}$ | 61 |
| NC | 65 | PG2 | 19 | TDO | 27 | $V_{DDINT}$ | 14 |
| NC | 66 | PG3 | 21 | TMS | 25 | $V_{DDINT}$ | 32 |
| $\overline{NMI}$ | 1 | PG4 | 22 | $\overline{TRST}$ | 26 | $V_{DDINT}$ | 42 |
| PF0 | 76 | PG5 | 28 | $V_{DDEXT}$ | 5 | $V_{DDINT}$ | 53 |
| PF1 | 77 | PG6 | 29 | $V_{DDEXT}$ | 10 | $V_{DDINT}$ | 57 |
| PF2 | 80 | PG7 | 30 | $V_{DDEXT}$ | 13 | $V_{DDINT}$ | 75 |
| PF3 | 81 | PG8 | 33 | $V_{DDEXT}$ | 16 | XTAL | 69 |
| | | | | | | GND | 89* |

* Pin no. 89 is the GND supply (see Figure 92) for the processor; this pad **must** connect to GND.

# OUTLINE DIMENSIONS

Dimensions in Figure 93 (for the 120-lead LQFP) and in Figure 94 (for the 88-lead LFCSP) are shown in millimeters.

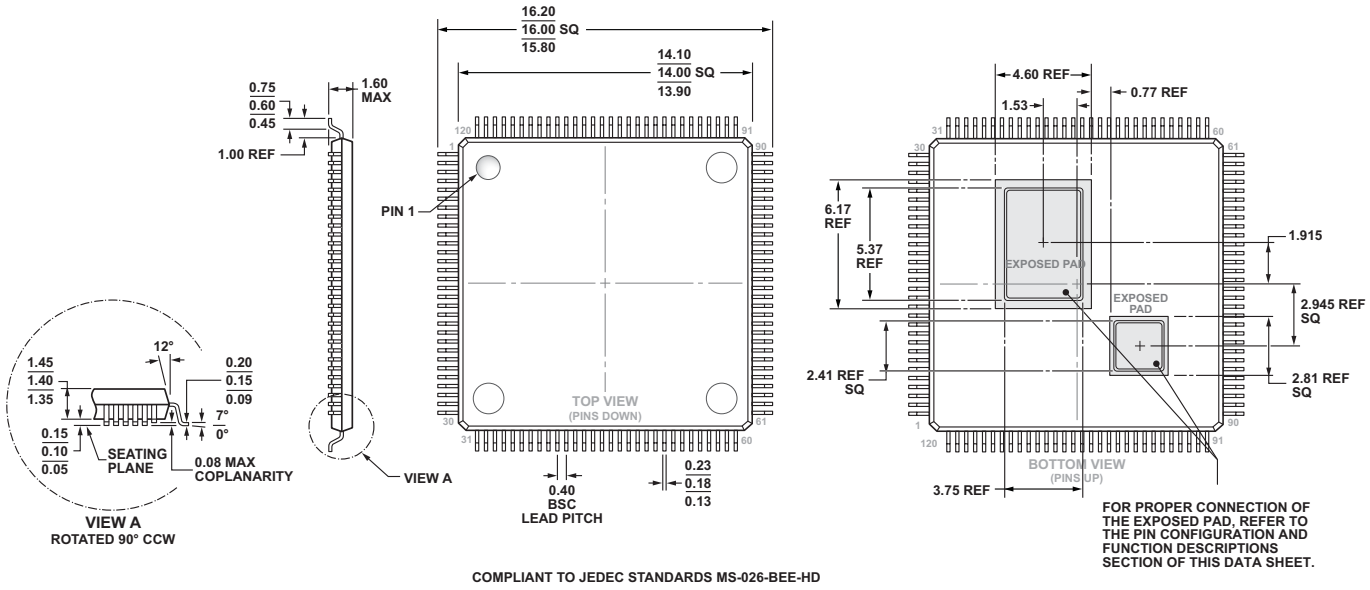


*Figure 93. 120-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP][1]*
*(SW-120-2)*
*Dimensions shown in millimeters*

[1] For information relating to the SW-120-2 package's exposed pad, see the table endnote on Page 74.

## AUTOMOTIVE PRODUCTS

The ADBF504W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 58 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

**Table 58. Automotive Products**

| Automotive Models[1,2] | Temperature Range[3] | Processor Instruction Rate (Maximum) | Flash Memory | Package Description | Package Option |
|---|---|---|---|---|---|
| ADBF504WYCPZ4XX | –40°C to +105°C | 400 MHz | N/A | 88-Lead LFCSP_VQ | CP-88-5 |

[1] Z = RoHS compliant part.
[2] The use of xx designates silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 26 for junction temperature ($T_J$) specification which is the only temperature specification.

## ORDERING GUIDE

| Model[1,2] | Temperature Range[3,4] | Processor Instruction Rate (Maximum) | Flash Memory | Package Description | Package Option |
|---|---|---|---|---|---|
| ADSP-BF504BCPZ-3F | –40°C to +85°C | 300 MHz | 32M bit | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-BF504BCPZ-4 | –40°C to +85°C | 400 MHz | N/A | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-BF504BCPZ-4F | –40°C to +85°C | 400 MHz | 32M bit | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-BF504KCPZ-3F | 0°C to +70°C | 300 MHz | 32M bit | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-BF504KCPZ-4 | 0°C to +70°C | 400 MHz | N/A | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-BF504KCPZ-4F | 0°C to +70°C | 400 MHz | 32M bit | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-BF506BSWZ-3F | –40°C to +85°C | 300 MHz | 32M bit | 120-Lead LQFP_EP | SW-120-2 |
| ADSP-BF506BSWZ-4F | –40°C to +85°C | 400 MHz | 32M bit | 120-Lead LQFP_EP | SW-120-2 |
| ADSP-BF506KSWZ-3F | 0°C to +70°C | 300 MHz | 32M bit | 120-Lead LQFP_EP | SW-120-2 |
| ADSP-BF506KSWZ-4F | 0°C to +70°C | 400 MHz | 32M bit | 120-Lead LQFP_EP | SW-120-2 |

[1] Z = RoHS compliant part.
[2] For feature comparison between ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors, see the Processor Comparison in Table 1 on Page 3.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 26 for junction temperature ($T_J$) specification which is the only temperature specification.
[4] Temperature range 0°C to +70°C is classified as commercial, and temperature range –40°C to +85°C is classified as industrial.

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