Infineon Technologies - MB96F693ABPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

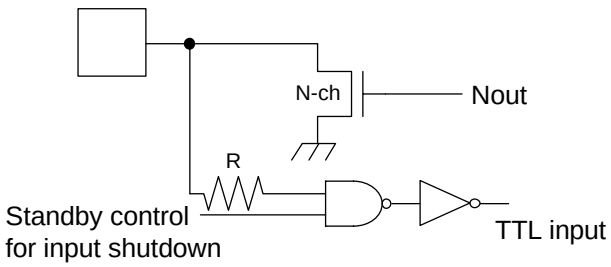
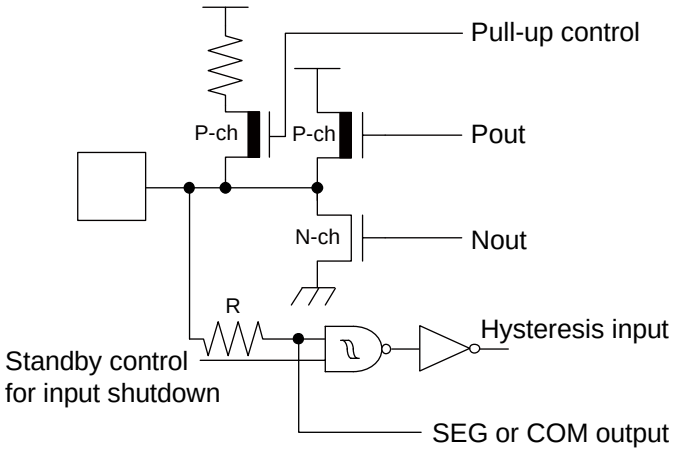
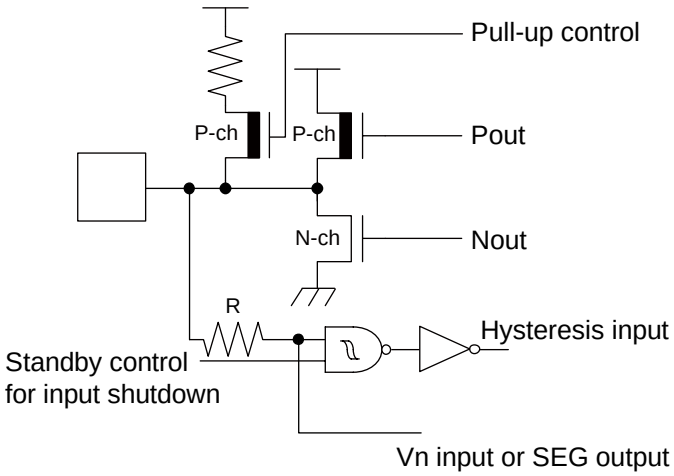
Applications of "Embedded - Microcontrollers"

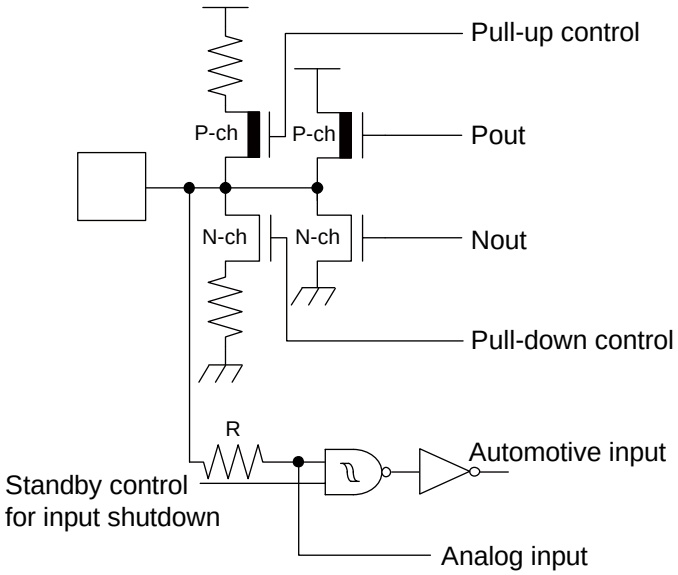
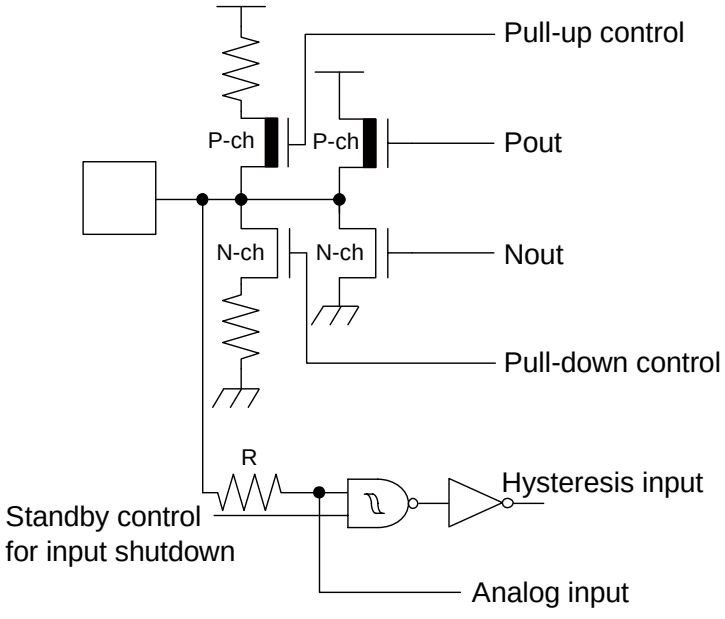
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	77
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f693abpmc-gse1

Contents

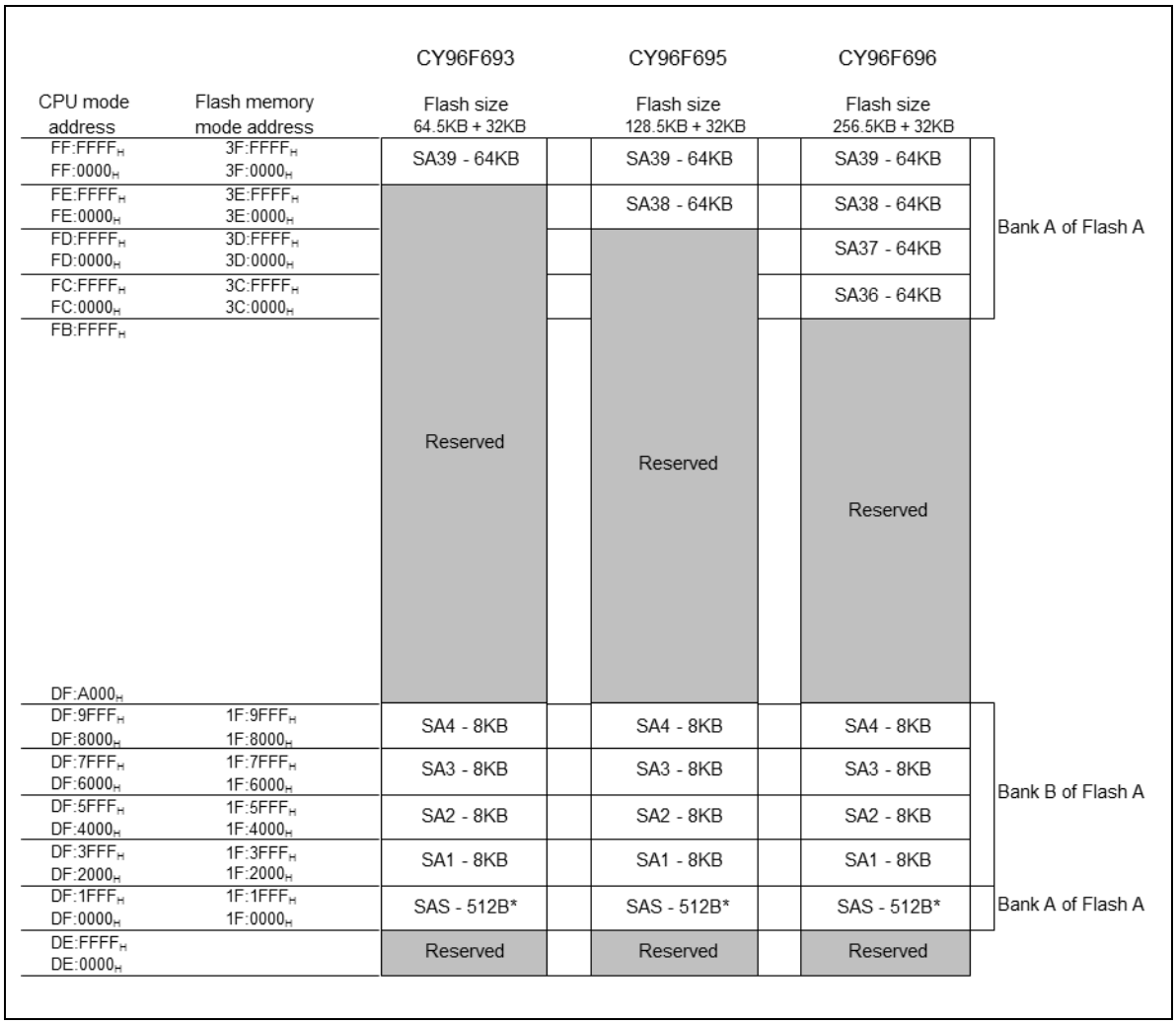
5. Pin Circuit Type

Pin No.	I/O Circuit Type*	Pin Name
1	Supply	Vss
2	F	C
3	P	P03_7 / INT1 / SIN1 / SEG40
4	J	P13_0 / INT2 / SOT1 / SEG41
5	P	P13_1 / INT3 / SCK1 / SEG42
6	J	P13_2 / PPG0 / TIN0 / FRCK1 / SEG43
7	J	P13_3 / PPG1 / TOT0 / WOT / SEG44
8	P	P13_4 / SIN0 / INT6 / SEG45
9	H	P13_5 / SOT0 / ADTG / INT7
10	M	P13_6 / SCK0 / CKOTX0
11	N	P04_4 / PPG3 / SDA0
12	N	P04_5 / PPG4 / SCL0
13	I	P06_2 / AN2 / INT5 / SIN5
14	K	P06_3 / AN3 / FRCK0
15	K	P06_4 / AN4 / IN0 / TTG0 / TTG4
16	K	P06_6 / AN6 / TIN1 / IN4_R
17	K	P06_7 / AN7 / TOT1 / IN5_R
18	Supply	AVcc
19	G	AVRH
20	G	AVRL
21	Supply	AVss
22	K	P05_0 / AN8
23	K	P05_2 / AN10 / OUT2 / SGO1
24	K	P05_3 / AN11 / OUT3 / SGA1
25	Supply	Vcc
26	Supply	Vss
27	K	P05_4 / AN12 / INT2_R / WOT_R
28	K	P05_6 / AN14 / TIN2 / SGO1_R
29	K	P05_7 / AN15 / TOT2 / SGA1_R
30	R	P08_0 / PWM1P0 / AN16
31	R	P08_1 / PWM1M0 / AN17
32	R	P08_2 / PWM2P0 / AN18
33	R	P08_3 / PWM2M0 / AN19
34	R	P08_4 / PWM1P1 / AN20
35	Supply	DVcc
36	Supply	DVss
37	R	P08_5 / PWM1M1 / AN21
38	R	P08_6 / PWM2P1 / AN22 / PPG6_B

Type	Circuit	Remarks
O		■ Open-drain I/O ■ Output 25mA, Vcc = 2.7V ■ TTL input
P		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis inputs with input shutdown function ■ Programmable pull-up resistor ■ SEG or COM output
Q		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis inputs with input shutdown function ■ Programmable pull-up resistor ■ Vn input or SEG output

Type	Circuit	Remarks
R		■ CMOS level output (programmable I_{OL} = 4mA, I_{OH} = -4mA and I_{OL} = 30mA, I_{OH} = -30mA) ■ Automotive input with input shutdown function ■ Programmable pull-up / pull-down resistor ■ Analog input
S		■ CMOS level output (programmable I_{OL} = 4mA, I_{OH} = -4mA and I_{OL} = 30mA, I_{OH} = -30mA) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up / pull-down resistor ■ Analog input

9. User ROM Memory Map for Flash Devices



CPU mode address	Flash memory mode address	CY96F693 Flash size 64.5KB + 32KB	CY96F695 Flash size 128.5KB + 32KB	CY96F696 Flash size 256.5KB + 32KB	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	Reserved	SA38 - 64KB	SA38 - 64KB	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$		Reserved	SA37 - 64KB	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$			SA36 - 64KB	
FB:FFFF$_H$				Reserved	
DF:A000$_H$					
DF:9FFF$_H$ DF:8000$_H$	1F:9FFF$_H$ 1F:8000$_H$	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SAS - 512B*	SAS - 512B*	SAS - 512B*	Bank A of Flash A
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	Reserved	

*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS cannot be used for E^{2}PROM emulation.

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
40	$35C_H$	PPG2	Yes	40	Programmable Pulse Generator 2
41	358_H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354_H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350_H	PPG5	Yes	43	Programmable Pulse Generator 5
44	$34C_H$	PPG6	Yes	44	Programmable Pulse Generator 6
45	348_H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344_H	-	-	46	Reserved
47	340_H	-	-	47	Reserved
48	$33C_H$	-	-	48	Reserved
49	338_H	-	-	49	Reserved
50	334_H	-	-	50	Reserved
51	330_H	-	-	51	Reserved
52	$32C_H$	PPG14	Yes	52	Programmable Pulse Generator 14
53	328_H	PPG15	Yes	53	Programmable Pulse Generator 15
54	324_H	-	-	54	Reserved
55	320_H	-	-	55	Reserved
56	$31C_H$	-	-	56	Reserved
57	318_H	-	-	57	Reserved
58	314_H	RLT0	Yes	58	Reload Timer 0
59	310_H	RLT1	Yes	59	Reload Timer 1
60	$30C_H$	RLT2	Yes	60	Reload Timer 2
61	308_H	RLT3	Yes	61	Reload Timer 3
62	304_H	-	-	62	Reserved
63	300_H	-	-	63	Reserved
64	$2FC_H$	RLT6	Yes	64	Reload Timer 6
65	$2F8_H$	ICU0	Yes	65	Input Capture Unit 0
66	$2F4_H$	ICU1	Yes	66	Input Capture Unit 1
67	$2F0_H$	-	-	67	Reserved
68	$2EC_H$	-	-	68	Reserved
69	$2E8_H$	ICU4	Yes	69	Input Capture Unit 4
70	$2E4_H$	ICU5	Yes	70	Input Capture Unit 5
71	$2E0_H$	ICU6	Yes	71	Input Capture Unit 6
72	$2DC_H$	ICU7	Yes	72	Input Capture Unit 7
73	$2D8_H$	-	-	73	Reserved
74	$2D4_H$	-	-	74	Reserved
75	$2D0_H$	-	-	75	Reserved
76	$2CC_H$	-	-	76	Reserved
77	$2C8_H$	OCU0	Yes	77	Output Compare Unit 0
78	$2C4_H$	OCU1	Yes	78	Output Compare Unit 1
79	$2C0_H$	OCU2	Yes	79	Output Compare Unit 2
80	$2BC_H$	OCU3	Yes	80	Output Compare Unit 3
81	$2B8_H$	-	-	81	Reserved

■ Lead-Free Packaging

CAUTION:

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

12.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

CAUTION:

Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} . Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.8 Pin Handling when not using the A/D Converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

13.10 Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

13.11 SMC Power Supply Pins

All DVcc /DVss pins must be set to the same level as the Vcc /Vss pins.

Note that the SMC I/O pin state is undefined if DV_{CC} is powered on and V_{CC} is below 3V. To avoid this, V_{CC} must always be powered on before DV_{CC}.

DV_{CC}/DV_{SS} must be applied when using SMC I/O pin as GPIO.

13.12 Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to V_{cc} or V_{ss} pin and provide a low-impedance connection.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage[1]	V_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	
Analog power supply voltage[1]	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$[2]
Analog reference voltage[1]	AVRH, AVRL	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL ≥ AV_{SS}
SMC Power supply[1]	DV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC} = DV_{CC}$[2]
LCD power supply voltage[1]	V0 to V3	-	V_{SS} - 0.3	V_{SS} + 6.0	V	V0 to V3 must not exceed V_{CC}
Input voltage[1]	V_I	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq (D)V_{CC} + 0.3V$[3]
Output voltage[1]	V_O	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq (D)V_{CC} + 0.3V$[3]
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins [4]
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	-	-	25	mA	Applicable to general purpose I/O pins [4]
"L" level maximum output current	I_{OL}	-	-	15	mA	Normal port
	I_{OLSMC}	T_A= -40°C	-	52	mA	High current port
		T_A= +25°C	-	39	mA	
		T_A= +85°C	-	32	mA	
		T_A= +105°C	-	30	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	Normal port
	$I_{OLAVSMC}$	T_A= -40°C	-	40	mA	High current port
		T_A= +25°C	-	30	mA	
		T_A= +85°C	-	25	mA	
		T_A= +105°C	-	23	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	50	mA	Normal port
	ΣI_{OLSMC}	-	-	260	mA	High current port
"L" level average overall output current	ΣI_{OLAV}	-	-	25	mA	Normal port
	$\Sigma I_{OLAVSMC}$	-	-	170	mA	High current port

14.3 DC Characteristics

14.3.1 *Current Rating*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[1]	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	28	-	mA	T_A = +25°C
				-	-	38	mA	T_A = +105°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	8	mA	T_A = +105°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.8	-	mA	T_A = +25°C
				-	-	6	mA	T_A = +105°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.16	-	mA	T_A = +25°C
				-	-	3.5	mA	T_A = +105°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3.3	mA	T_A = +105°C

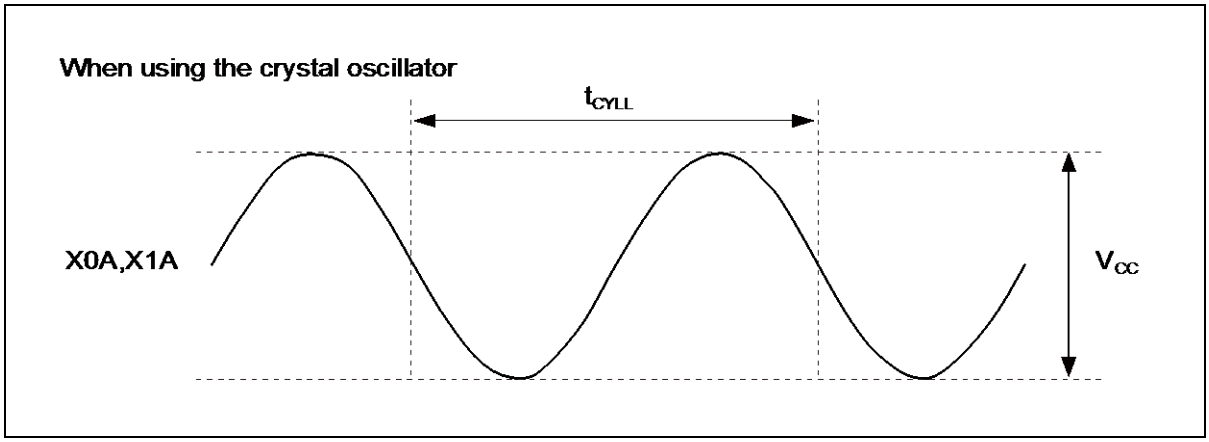
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Sleep modes[1]	I_{CCSPLL}	Vcc	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	9.5	-	mA	T_A = +25°C
				-	-	15	mA	T_A = +105°C
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	1.1	-	mA	T_A = +25°C
				-	-	4.7	mA	T_A = +105°C
	I_{CCSRCH}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped)	-	0.6	-	mA	T_A = +25°C
				-	-	4.1	mA	T_A = +105°C
	I_{CCSRCL}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped)	-	0.07	-	mA	T_A = +25°C
				-	-	2.9	mA	T_A = +105°C
	I_{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.04	-	mA	T_A = +25°C
				-	-	2.7	mA	T_A = +105°C
Power supply current in Timer modes[2]	I_{CCTPLL}	Vcc	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2250	µA	T_A = +25°C
				-	-	3220	µA	T_A = +105°C
	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	330	µA	T_A = +25°C
				-	-	1200	µA	T_A = +105°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	215	µA	T_A = +25°C
				-	-	1110	µA	T_A = +105°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz, (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	µA	T_A = +25°C
				-	-	910	µA	T_A = +105°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	µA	T_A = +25°C
				-	-	885	µA	T_A = +105°C

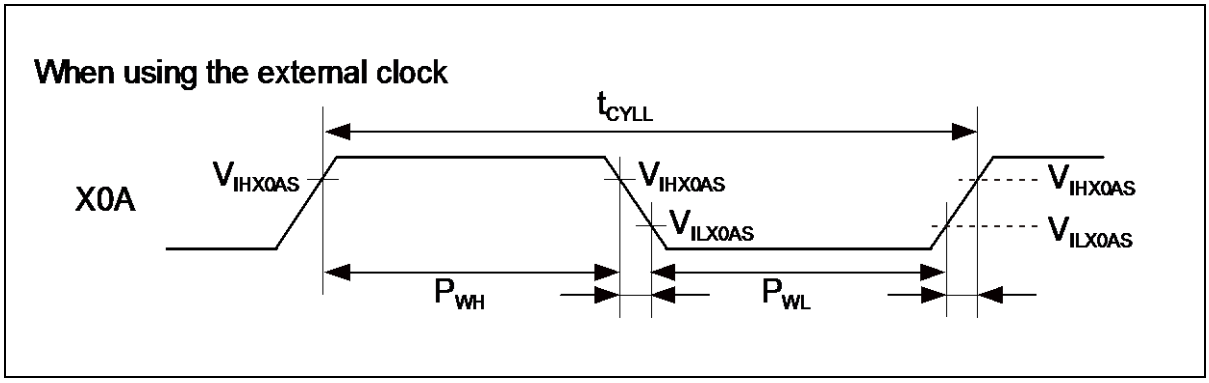
Parameters	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL4}	4mA type	4.5V ≤ (D)V_{CC} ≤ 5.5V I_{OL} = +4mA	-	-	0.4	V	
			2.7V ≤ (D)V_{CC} < 4.5V I_{OL} = +1.7mA					
	V_{OL30}	High Drive type*	4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +52mA	-	-	0.5	V	T_A = -40°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +22mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +39mA					T_A = +25°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +18mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +32mA					T_A = +85°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +14mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +30mA					T_A = +105°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +13.5mA					
	V_{OL3}	3mA type	2.7V ≤ V_{CC} < 5.5V I_{OL} = +3mA	-	-	0.4	V	
	V_{OLD}	DEBUG I/F	V_{CC} = 2.7V I_{OL} = +25mA	0	-	0.25	V	
Input leak current	I_{IL}	Pnn_m	V_{SS} < V_I < V_{CC} AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 1	-	+ 1	µA	Single port pin except high current output I/O for SMC
		P08_m, P09_m, P10_m	DV_{SS} < V_I < DV_{CC} AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 3	-	+ 3	µA	
Total LCD leak current	$\Sigma\|I_{ILCD}\|$	All SEG/ COM pin	V_{CC} = 5.0V	-	0.5	10	µA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V2, V2 and V1, V1 and V0	V_{CC} = 5.0V	6.25	12.5	25	kΩ	

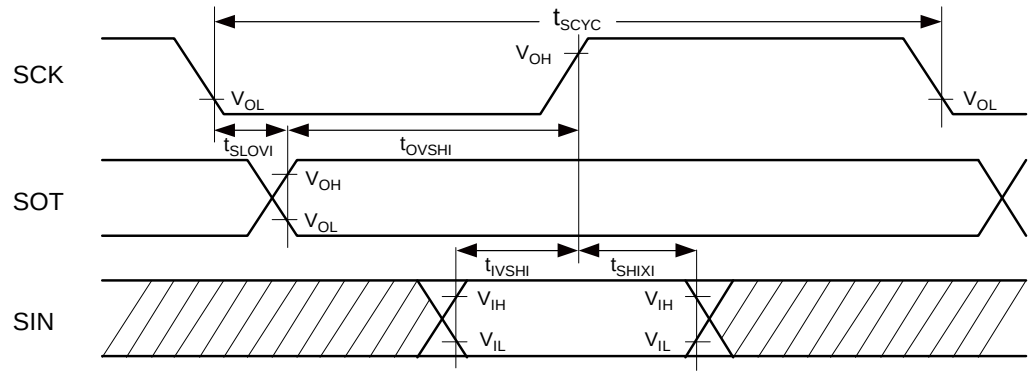
14.4.2 *Sub Clock Input Characteristics*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

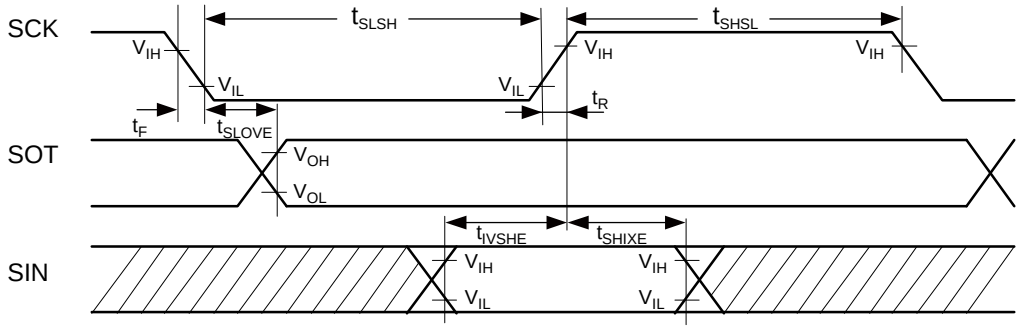
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	







Internal shift clock mode



External shift clock mode

14.5 A/D Converter

14.5.1 *Electrical Characteristics for the A/D Converter*

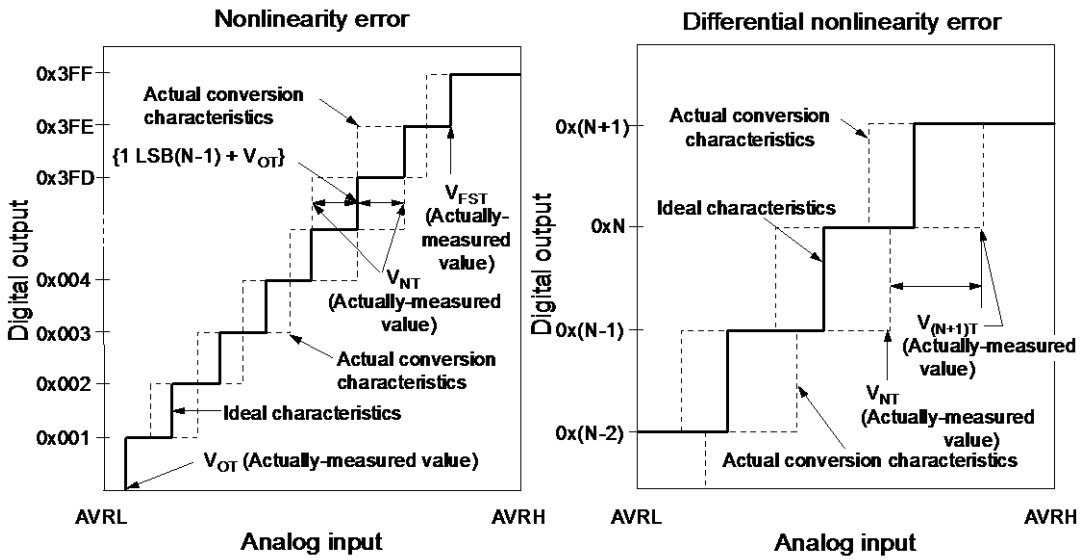
(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	AVRL+ 0.5LSB	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	AVRH- 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} < 4.5V
Sampling time*	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} < 4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH and AVRL)	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	AN2 to 4, 6 to 8, 10 to 12, 14, 15	-	-	16.0	pF	Normal outputs
		AN16 to 31	-	-	17.8	pF	High current outputs
Analog impedance	R_{VIN}	ANn	-	-	2050	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
			-	-	3600	Ω	2.7V ≤ AV_{CC} < 4.5V
Analog port input current (during conversion)	I_{AIN}	AN2 to 4, 6 to 8, 10 to 12, 14, 15	- 0.3	-	+ 0.3	µA	AV_{SS} , AVRL < V_{AIN} < AV_{CC}, AVRH
		AN16 to 31	- 3.0	-	+ 3.0	µA	
Analog input voltage	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC} - 0.1	-	AV_{CC}	V	
	-	AVRL	AV_{SS}	-	AV_{SS}+ 0.1	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

14.5.3 *Definition of A/D Converter Terms*

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

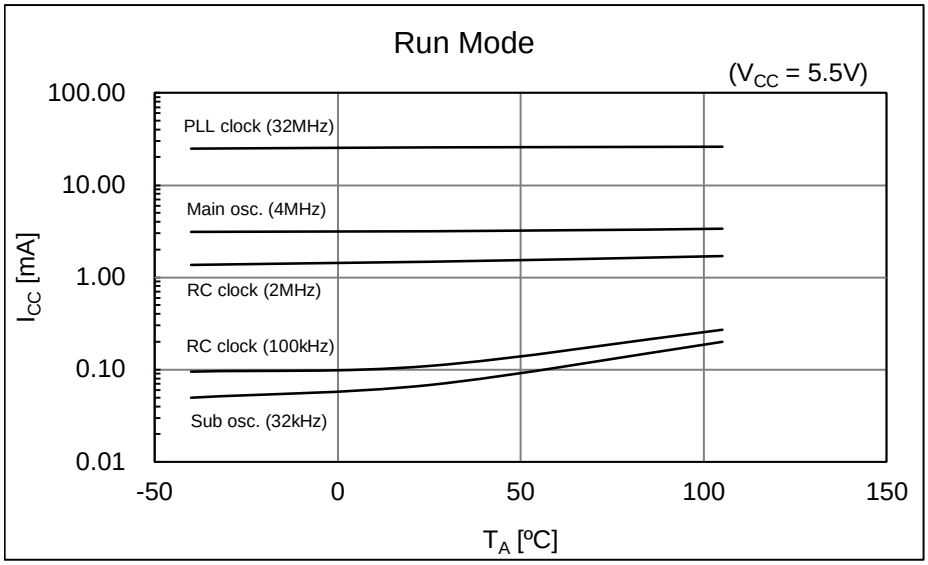
$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

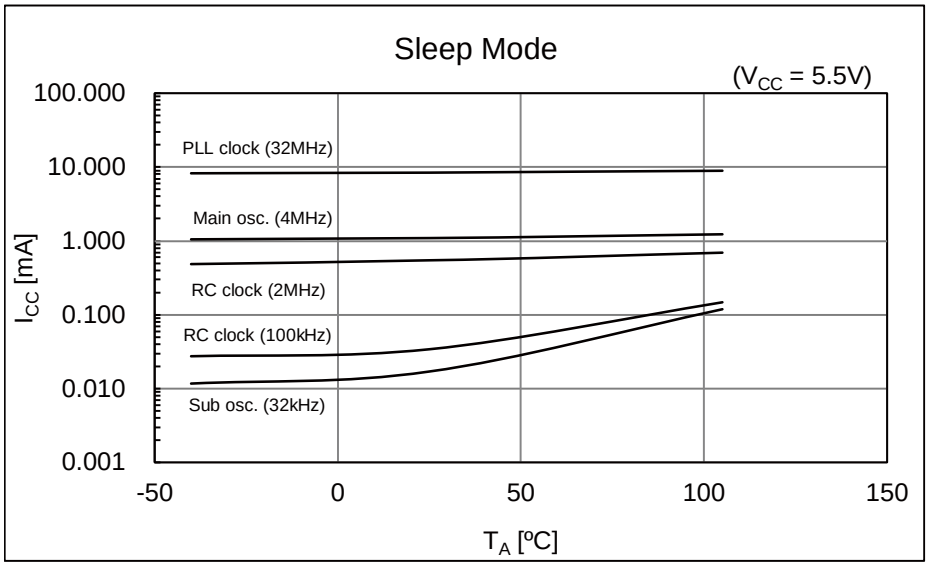
N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

15. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

■ CY96F696





Page	Section	Change Results
		Added Remarks to “PLL oscillation clock frequency”
		Added “ PLL phase jitter” and the figure
	4. AC Characteristics (6) Reset Input	Added the figure for reset input time (t_{RSTL})
51	4. AC Characteristics (8) USART Timing	Changed the condition (V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C) (V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C, C_L = 50pF)
		Changed the HARDWARE MANUAL “MB96690 series HARDWARE MANUAL” “MB96600 series HARDWARE MANUAL”
52		Changed the figure for “Internal shift clock mode”
54	4. AC Characteristics (10) I^2C timing	Added parameter, “Noise filter” and an annotation *5 for it
		Added t_{SP} to the figure
55	5. A/D Converter (1) Electrical Characteristics for the A/D Converter	Added “Analog impedance”
		Added “Variation between channels”
		Added the annotation
56	5. A/D Converter (2) Accuracy and Setting of the A/D Converter Sampling Time	Deleted the unit “[Min]” from approximation formula of Sampling time
57	5. A/D Converter (3) Definition of A/D Converter Terms	Changed the Description and the figure “Linearity” → “Nonlinearity” “Differential linearity error” “Differential nonlinearity error”
		Changed the Description Linearity error: Deviation of the line between the zero-transition point (0b0000000000←→0b0000000001) and the full-scale transition point (0b1111111110←→0b1111111111) from the actual conversion characteristics. Nonlinearity error: Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ←→ 0b0000000001) to the full-scale transition point (0b1111111110 ←→ 0b1111111111).
		Added the Description “Zero transition voltage” “Full scale transition voltage”
59	6. High Current Output Slew Rate	Changed the condition (V_{CC} = AV_{CC} = 2.7V to 5.5V, DV_{CC} = 4.5V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C) (V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)
		Changed the Symbol and figure t_{R2}, t_{F2}, V_{OL2} t_{R30}, t_{F30}, V_{OL30}
59	7. Low Voltage Detection Function Characteristics	Added the Value of “ Power supply voltage change rate” Max: +0.004 V/µs
		Added “Hysteresis width” (V_{HYS})
		Added “Stabilization time” ($T_{LVDSTAB}$)
		Added “Detection delay time” (t_d)
		Deleted the Remarks
		Added the annotation *1, *2
59	7. Low Voltage Detection Function Characteristics	Added the figure for “Hysteresis width”
		Added the figure for “Stabilization time”

Page	Section	Change Results
61	8. Flash Memory Write/Erase Characteristics	Changed the Value of “Sector erase time”
		Added “Security Sector” to “Sector erase time”
		Changed the Parameter “Half word (16 bit) write time” “Word (16-bit) write time”
		Changed the Value of “Chip erase time”
		Changed the Remarks of “Sector erase time” Excludes write time prior to internal erase Includes write time prior to internal erase
		Added the Note and annotation *1
		Deleted “(targeted value)” from title “ Write/Erase cycles and data hold time”
62 to 63	■EXAMPLE CHARACTERISTICS	Added a section
65	■ORDERING INFORMATION	Changed part number MCU with CAN controller MB96F696RAPMC-GSE1* → MB96F696RBPMC-GSE1 MB96F696RAPMC-GSE2* → MB96F696RBPMC-GSE2
		Added part number MCU with CAN controller MB96F693RBPMC-GSE1 MB96F693RBPMC-GSE2 MB96F695RBPMC-GSE1 MB96F695RBPMC-GSE2 MCU without CAN controller MB96F693ABPMC-GSE1 MB96F693ABPMC-GSE2 MB96F695ABPMC-GSE1 MB96F695ABPMC-GSE2
Revision 1.1		
-	-	Company name and layout design change

NOTE: Please see “Document History” about later revised information.

Page	Section	Change Results
Rev.*B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
7, 9, 66,67	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-100P-M20 → LQI100