Infineon Technologies - MB96F693RBPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	77
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f693rbpmc-gse1

- Extended support for LIN-Protocol (with 16-byte FIFO for selected channels) to reduce interrupt load.

I²C

- Up to 400kbps
- Master and Slave functionality, 7-bit and 10-bit addressing

A/D Converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function
- Scan disable Function
- ADC Pulse Detection Function

Source Clock Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

Hardware Watchdog Timer

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free-Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
- Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with Free-running Timer occurs
- A pair of compare registers can be used to generate an output signal

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as 2 ×8-bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture
- Start delay

Stepping Motor Controller

- Stepping Motor Controller with integrated high current output drivers
- Four high current outputs for each channel
- Two synchronized 8/10-bit PWMs per channel
- Internal prescaling for PWM clock: 1, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/16 of peripheral clock
- Dedicated power supply for high current output drivers

LCD Controller

- LCD controller with up to 4COM ×36SEG
- Internal or external voltage generation
- Duty cycle: Selectable from options: 1/2, 1/3 and 1/4
- Fixed 1/3 bias
- Programmable frame period
- Clock source selectable from four options (main clock, peripheral clock, subclock or RC oscillator clock)
- Internal divider resistors or external divider resistors
- On-chip data memory for display
- LCD display can be operated in Timer Mode
- Blank display: selectable
- All SEG, COM and V pins can be switched between general and specialized purposes

Sound Generator

- 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter
- PWM clock by internal prescaler: 1, 1/2, 1/4, 1/8 of peripheral clock

Real Time Clock

- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day

Contents

1. Product Lineup

Features		CY96690	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
64.5KB + 32KB	8KB	CY96F693R, CY96F693A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB	8KB	CY96F695R, CY96F695A	
256.5KB + 32KB	16KB	CY96F696R	
Package		LQFP-100 LQI100	
DMA		4ch	
USART		5ch	LIN-USART 0 to 2/4/5
	with automatic LIN-Header transmission/reception	2ch	LIN-USART 0/1
	with 16 byte RX- and TX-FIFO		
I^2C		1ch	I^2C 0
8/10-bit A/D Converter		27ch	AN 2 to 4/6 to 8/10 to 12/ 14 to 31
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	Yes	
	with ADC Pulse Detection	Yes	
16-bit Reload Timer (RLT)		5ch	RLT 0 to 3/6
16-bit Free-Running Timer (FRT)		2ch	FRT 0/1
16-bit Input Capture Unit (ICU)		6ch (5 channels for LIN-USART)	ICU 0/1/4 to 7 (ICU 0/1/4 to 6 for LIN-USART)
16-bit Output Compare Unit (OCU)		4ch	OCU 0 to 3
8/16-bit Programmable Pulse Generator (PPG)		10ch (16-bit) / 14ch (8-bit)	PPG 0 to 7/14/15
	with Timing point capture	Yes	
	with Start delay	Yes	
	with Ramp	No	
CAN Interface		1ch	CAN 0 32 Message Buffers
Stepping Motor Controller (SMC)		4ch	SMC 0 to 2/4
External Interrupts (INT)		16ch	INT 0 to 15
Non-Maskable Interrupt (NMI)		1ch	
Sound Generator (SG)		2ch	SG 0/1
LCD Controller		4COM × 36SEG	COM 0 to 3 SEG 0 to 4/7/ 11 to 28/30/33/36 to 45
Real Time Clock (RTC)		1ch	
I/O Ports		75 (Dual clock mode) 77 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

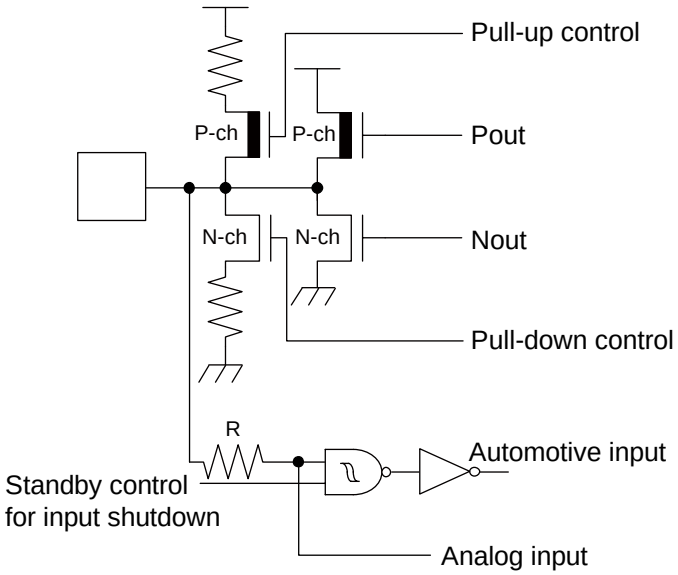
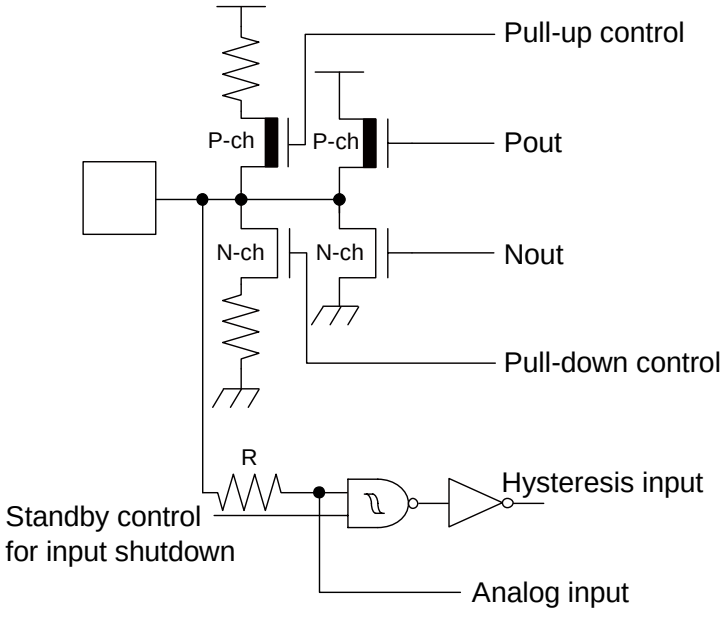
Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.*

4. Pin Description

Pin Name	Feature	Description
ADTG	ADC	A/D converter trigger input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVRL	ADC	A/D converter low reference voltage input pin
AV_{SS}	Supply	Analog circuits power supply pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
CKOTXn_R	Clock Output function	Relocated Clock Output function n inverted output pin
COMn	LCD	LCD Common driver pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
DV_{CC}	Supply	SMC pins power supply
DV_{SS}	Supply	SMC pins power supply
FRCKn	Free-Running Timer	Free-Running Timer n input pin
FRCKn_R	Free-Running Timer	Relocated Free-Running Timer n input pin
INn	ICU	Input Capture Unit n input pin
INn_R	ICU	Relocated Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
OUTn	OCU	Output Compare Unit n waveform output pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_R	PPG	Relocated Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PWMn	SMC	SMC PWM high current output pin
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SCLn	I^2C	I^2C interface n clock I/O input/output pin
SDAn	I^2C	I^2C interface n serial data I/O input/output pin
SEGn	LCD	LCD Segment driver pin
SGAn	Sound Generator	Sound Generator amplitude output pin
SGAn_R	Sound Generator	Relocated Sound Generator amplitude output pin
SGOn	Sound Generator	Sound Generator sound/tone output pin

Pin Name	Feature	Description
SGOn_R	Sound Generator	Relocated Sound Generator sound/tone output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vn	LCD	LCD voltage reference pin
V_{cc}	Supply	Power supply pin
V_{ss}	Supply	Power supply pin
WOT	RTC	Real Time clock output pin
WOT_R	RTC	Relocated Real Time clock output pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin

Type	Circuit	Remarks
R		■ CMOS level output (programmable I_{OL} = 4mA, I_{OH} = -4mA and I_{OL} = 30mA, I_{OH} = -30mA) ■ Automotive input with input shutdown function ■ Programmable pull-up / pull-down resistor ■ Analog input
S		■ CMOS level output (programmable I_{OL} = 4mA, I_{OH} = -4mA and I_{OL} = 30mA, I_{OH} = -30mA) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up / pull-down resistor ■ Analog input

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

CY96690		
Pin Number	**USART Number**	**Normal Function**
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
46	USART2	SIN2
47		SOT2
48		SCK2
86	USART4	SIN4
87		SOT4
88		SCK4

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

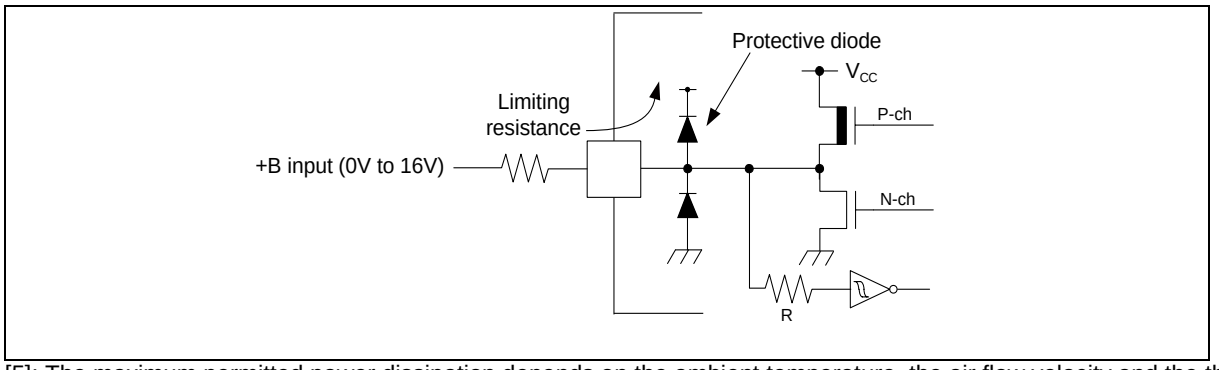
You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage[1]	V_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	
Analog power supply voltage[1]	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$[2]
Analog reference voltage[1]	AVRH, AVRL	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL ≥ AV_{SS}
SMC Power supply[1]	DV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC} = DV_{CC}$[2]
LCD power supply voltage[1]	V0 to V3	-	V_{SS} - 0.3	V_{SS} + 6.0	V	V0 to V3 must not exceed V_{CC}
Input voltage[1]	V_I	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq (D)V_{CC} + 0.3V$[3]
Output voltage[1]	V_O	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq (D)V_{CC} + 0.3V$[3]
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins [4]
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	-	-	25	mA	Applicable to general purpose I/O pins [4]
"L" level maximum output current	I_{OL}	-	-	15	mA	Normal port
	I_{OLSMC}	T_A= -40°C	-	52	mA	High current port
		T_A= +25°C	-	39	mA	
		T_A= +85°C	-	32	mA	
		T_A= +105°C	-	30	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	Normal port
	$I_{OLAVSMC}$	T_A= -40°C	-	40	mA	High current port
		T_A= +25°C	-	30	mA	
		T_A= +85°C	-	25	mA	
		T_A= +105°C	-	23	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	50	mA	Normal port
	ΣI_{OLSMC}	-	-	260	mA	High current port
"L" level average overall output current	ΣI_{OLAV}	-	-	25	mA	Normal port
	$\Sigma I_{OLAVSMC}$	-	-	170	mA	High current port

Sample recommended circuits:



[5]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

[6]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

WARNING:

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}, DV_{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C_S	0.5	1.0 to 3.9	4.7	µF	1.0µF (Allowance within ± 50%) 3.9µF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than C_S.

WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

14.3 DC Characteristics

14.3.1 *Current Rating*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[1]	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	28	-	mA	T_A = +25°C
				-	-	38	mA	T_A = +105°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	8	mA	T_A = +105°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.8	-	mA	T_A = +25°C
				-	-	6	mA	T_A = +105°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.16	-	mA	T_A = +25°C
				-	-	3.5	mA	T_A = +105°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3.3	mA	T_A = +105°C

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode[3]	I_{CCH}	Vcc	-	-	20	60	µA	T_A = +25°C
				-	-	880	µA	T_A = +105°C
Flash Power Down current	$I_{CCFLASHPD}$		-	-	36	70	µA	
Power supply current for active Low Voltage detector[4]	I_{CCLVD}		Low voltage detector enabled	-	5	-	µA	T_A = +25°C
				-	-	12.5	µA	T_A = +105°C
Flash Write/ Erase current[5]	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +105°C

[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

[2]: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32 kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

[3]: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

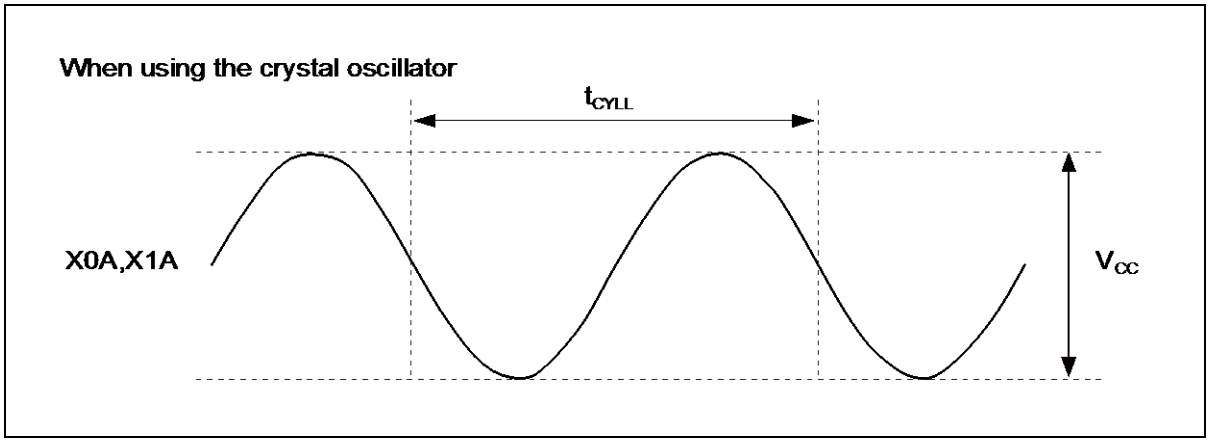
[4]: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

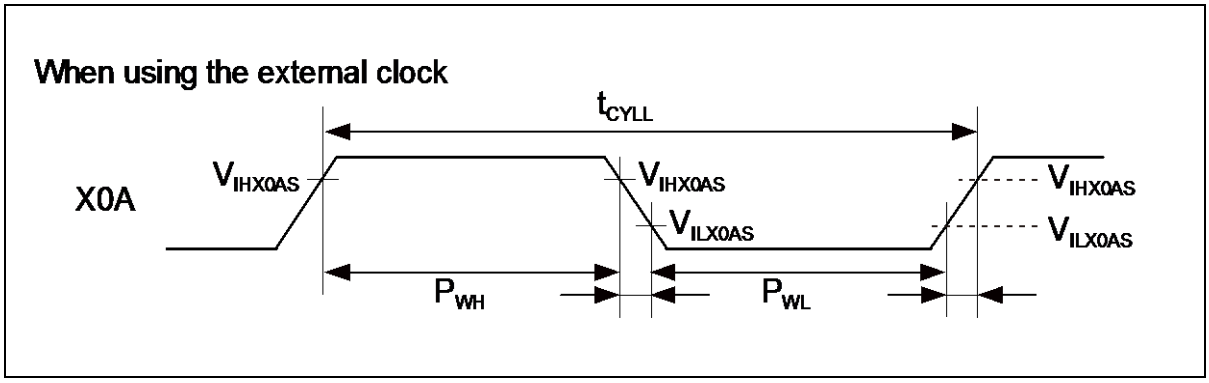
[5]: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

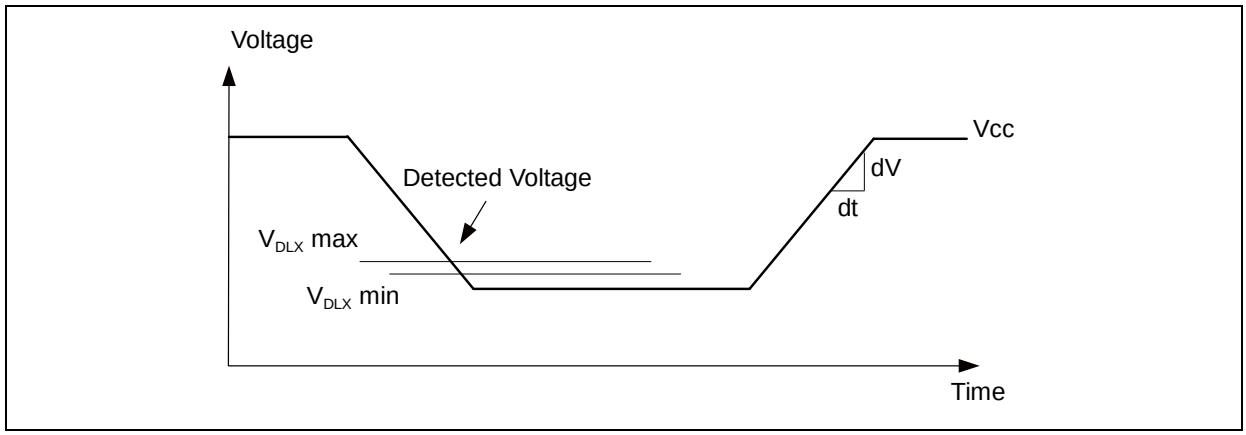
14.4.2 *Sub Clock Input Characteristics*

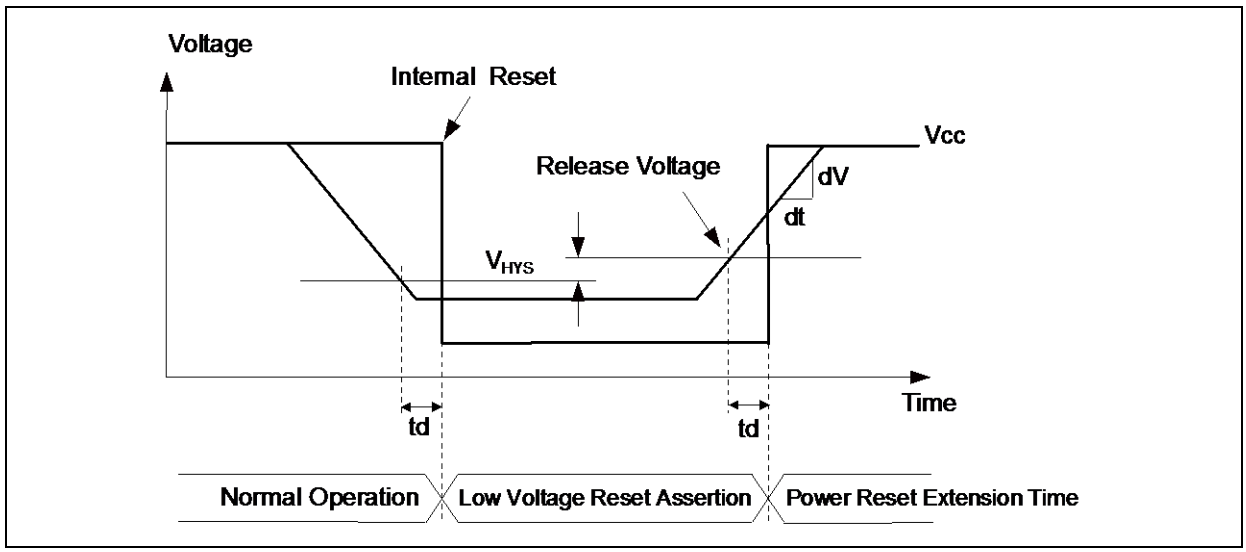
(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

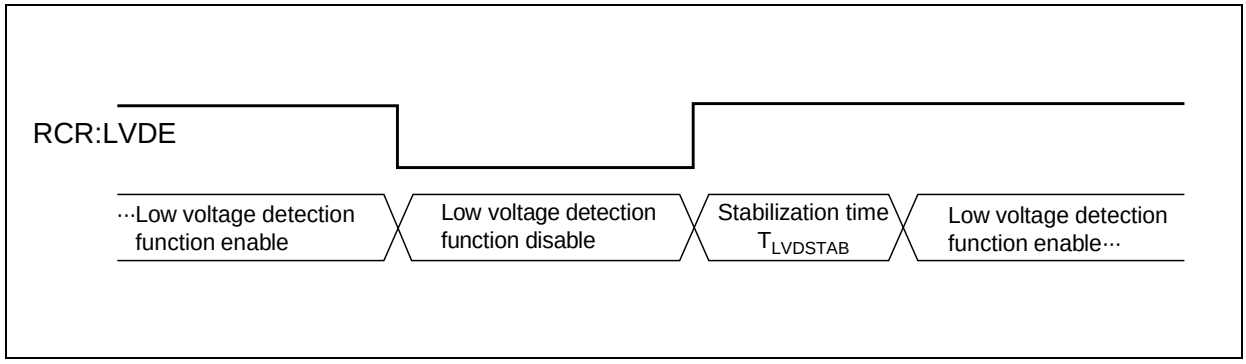
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	






Voltage
Vcc
dV
dt
Detected Voltage
V_{DLX} max
V_{DLX} min
Time


Voltage
Internal Reset
Vcc
Release Voltage
dV
dt
V_{HYS}
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time


RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time $T_{LVDSTAB}$
Low voltage detection function enable···

14.8 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	-	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time		-	-	25	400	µs	Not including system-level overhead time.
Chip erase time		-	-	8.31	40.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[1].

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20 [2]
10,000	10 [2]
100,000	5 [2]

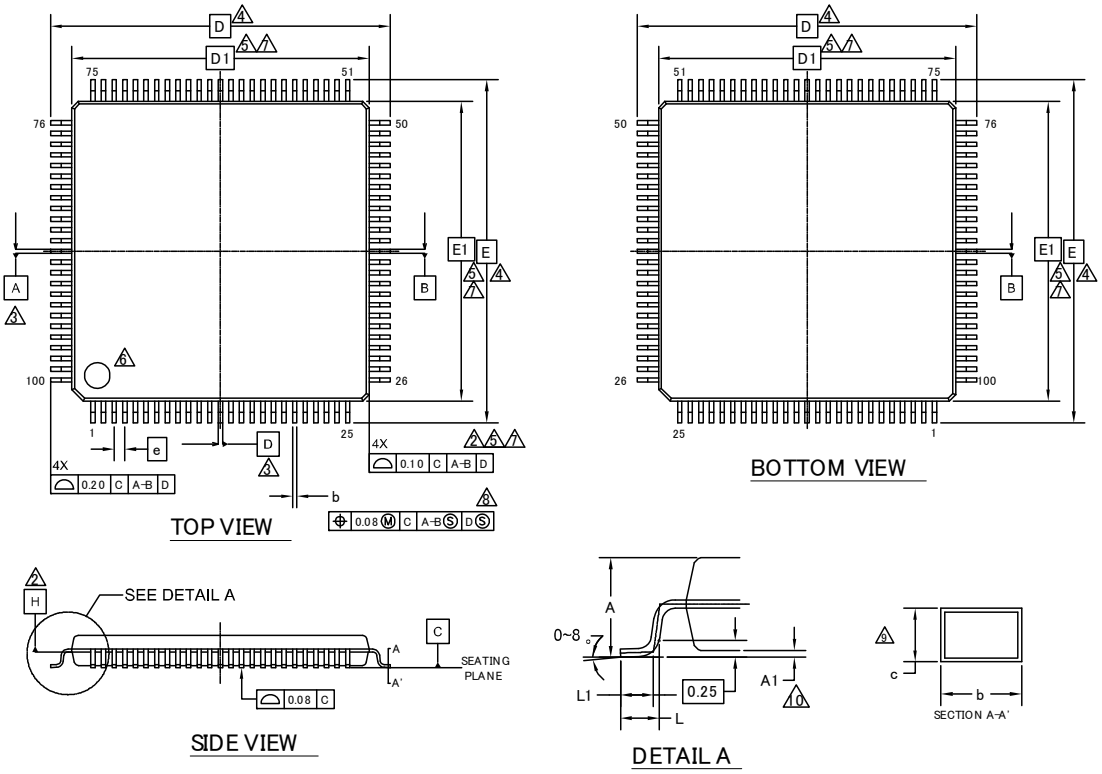
[1]: See "14.7 Low Voltage Detection Function Characteristics".

[2]: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

■ Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

17. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D		16.00 BSC	
D1		14.00 BSC	
e		0.50 BSC	
E		16.00 BSC	
E1		14.00 BSC	
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11500 *A

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

18. Major Changes

Spansion Publication Number: MB96F696-DS704-00011

Page	Section	Change Results
Revision 1.0		
-	-	PRELIMINARY → Data sheet
1	■FEATURES	Changed the description of “System clock” Up to 16 MHz external clock for devices with fast clock input feature Up to 8 MHz external clock for devices with fast clock input feature
2		Changed the description of “Free-Running Timers” Signals an interrupt on overflow Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
2		Changed the description of “LCD Controller” On-chip drivers for internal divider resistors or external divider resistors Internal divider resistors or external divider resistors
3		Changed the description of “External Interrupts” Interrupt mask and pending bit per channel Interrupt mask bit per channel
3		Changed the description of “Built-in On Chip Debugger” - Event sequencer: 2 levels - Event sequencer: 2 levels + reset
6	■PRODUCT LINEUP	Added the Product
		Changed the Remark of RLT RLT 0/1/2/3/6 Only RLT6 can be used as PPG clock source RLT 0 to 3/6
		Changed number of the I/O Ports 77 (Dual clock mode) 79 (Single clock mode) 75 (Dual clock mode) 77 (Single clock mode)
7	■BLOCK DIAGRAM	Deleted the block of RLT6 from PPG block
		Changed the RLT block 4ch 0/1/2/3/6 5ch
9	■PIN DESCRIPTION	Changed the Description of PPGn_B Programmable Pulse Generator n output (8bit) Programmable Pulse Generator n output (16bit/8bit)
13	■PIN CIRCUIT TYPE	Changed the I/O circuit type of Pin no.96 P Q
14	■I/O CIRCUIT TYPE	Changed the figure of type B
		Changed the Remarks of type B (CMOS hysteresis input with input shutdown function, I_{OL} = 4mA, I_{OH} = -4mA, Programmable pull-up resister) (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)
16		Changed the figure of type G
19		Added the Type Q
21	■MEMORY MAP	Changed the START addresses of Boot-ROM 0F:$E000_H$ 0F:$C000_H$
23	■USER ROM MEMORY MAP FOR FLASH DEVICES	Changed the annotation Others (from DF:0200_H to DF:$1FFF_H$) are all mirror area of SAS-512B. Others (from DF:0200_H to DF:$1FFF_H$) is mirror area of SAS-512B.
25	■INTERRUPT VECTOR TABLE	Changed the Description of CALLV0 to CALLV7 Reserved CALLV instruction

Page	Section	Change Results
		Changed the Description of RESET Reserved Reset vector
		Changed the Description of INT9 Reserved INT9 instruction
		Changed the Description of EXCEPTION Reserved Undefined instruction execution
26		Changed the Vector name of Vector number 64 PPGRLT RLT6
		Changed the Description of Vector number 64 Reload Timer 6 can be used as PPG clock source Reload Timer 6
29 to 32	■HANDLING PRECAUTIONS	Added a section
33	■HANDLING DEVICES	Added the description to “3. External clock usage” (3) Opposite phase external clock
35		Changed the description in “7. Turn on sequence of power supply to A/D converter and analog inputs” In this case, the voltage must not exceed AVRH or AV_{CC} In this case, AVRH must not exceed AV_{CC}. Input voltage for ports shared with analog input ports also must not exceed AV_{CC}
35		Changed the description in “11. SMC power supply pins” To avoid this, V_{CC} must always be powered on before DV_{CC}. To avoid this, V_{CC} must always be powered on before DV_{CC}. DVcc/DVss must be applied when using SMC I/O pin as GPIO.
		Added the description “13. Mode Pin (MD)”
36	■ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Changed the Symbol of “"L" level average overall output current” $\Sigma I_{OLSMCAV}$ $\Sigma I_{OLAVSMC}$
		Changed the Symbol of “"H" level average overall output current” $\Sigma I_{OHSMCAV}$ $\Sigma I_{OHAVSMC}$
37		Changed the annotation *2 It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on. It is required that AV_{CC} does not exceed V_{CC}, DV_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.
		Changed the annotation *3 Input/Output voltages of standard ports depend on V_{CC}. Input/Output voltages of high current ports depend on DV_{CC}. Input/Output voltages of standard ports depend on V_{CC}.
		Changed the annotation *4 Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode). Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
		Added the annotation *4 The DEBUG I/F pin has only a protective diode against V_{SS}. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.
38	2. Recommended Operating Conditions	Added the Value and Remarks to “Power supply voltage” Min: 2.0V Typ: - Max: 5.5V Remarks: Maintains RAM data in stop mode

Page	Section	Change Results
		Added Remarks to “PLL oscillation clock frequency”
		Added “ PLL phase jitter” and the figure
	4. AC Characteristics (6) Reset Input	Added the figure for reset input time (t_{RSTL})
51	4. AC Characteristics (8) USART Timing	Changed the condition (V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C) (V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C, C_L = 50pF)
		Changed the HARDWARE MANUAL “MB96690 series HARDWARE MANUAL” “MB96600 series HARDWARE MANUAL”
52		Changed the figure for “Internal shift clock mode”
54	4. AC Characteristics (10) I^2C timing	Added parameter, “Noise filter” and an annotation *5 for it
		Added t_{SP} to the figure
55	5. A/D Converter (1) Electrical Characteristics for the A/D Converter	Added “Analog impedance”
		Added “Variation between channels”
		Added the annotation
56	5. A/D Converter (2) Accuracy and Setting of the A/D Converter Sampling Time	Deleted the unit “[Min]” from approximation formula of Sampling time
57	5. A/D Converter (3) Definition of A/D Converter Terms	Changed the Description and the figure “Linearity” → “Nonlinearity” “Differential linearity error” “Differential nonlinearity error”
		Changed the Description Linearity error: Deviation of the line between the zero-transition point (0b0000000000←→0b0000000001) and the full-scale transition point (0b1111111110←→0b1111111111) from the actual conversion characteristics. Nonlinearity error: Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ←→ 0b0000000001) to the full-scale transition point (0b1111111110 ←→ 0b1111111111).
		Added the Description “Zero transition voltage” “Full scale transition voltage”
59	6. High Current Output Slew Rate	Changed the condition (V_{CC} = AV_{CC} = 2.7V to 5.5V, DV_{CC} = 4.5V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C) (V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)
		Changed the Symbol and figure t_{R2}, t_{F2}, V_{OL2} t_{R30}, t_{F30}, V_{OL30}
59	7. Low Voltage Detection Function Characteristics	Added the Value of “ Power supply voltage change rate” Max: +0.004 V/µs
		Added “Hysteresis width” (V_{HYS})
		Added “Stabilization time” ($T_{LVDSTAB}$)
		Added “Detection delay time” (t_d)
		Deleted the Remarks
		Added the annotation *1, *2
59	7. Low Voltage Detection Function Characteristics	Added the figure for “Hysteresis width”
		Added the figure for “Stabilization time”