Infineon Technologies - MB96F693RBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	77
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f693rbpmc-gse2

Contents

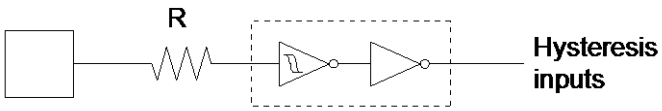
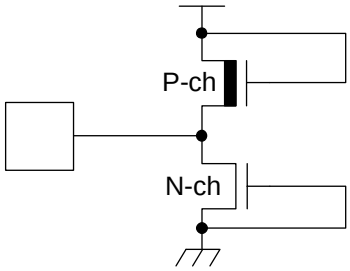
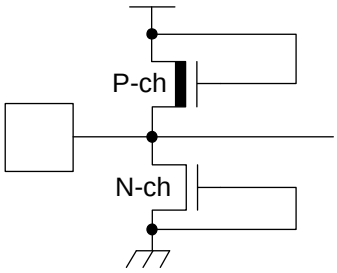
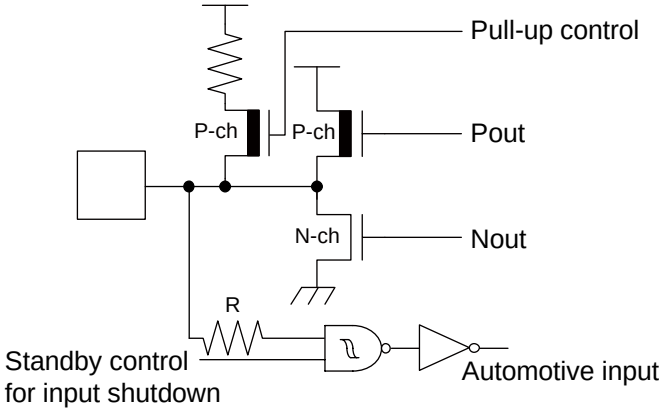
1. Product Lineup

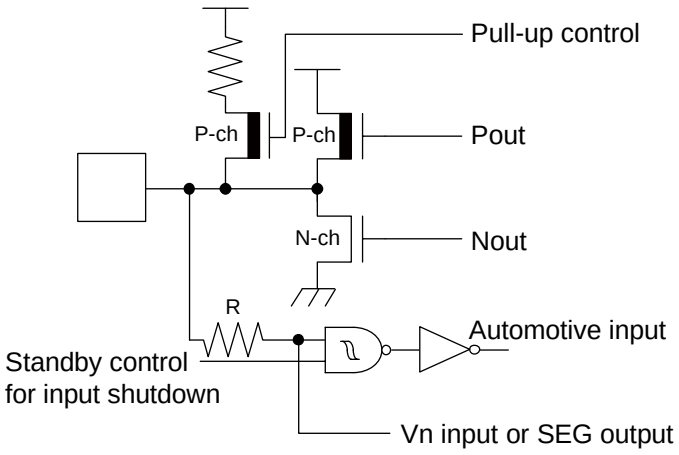
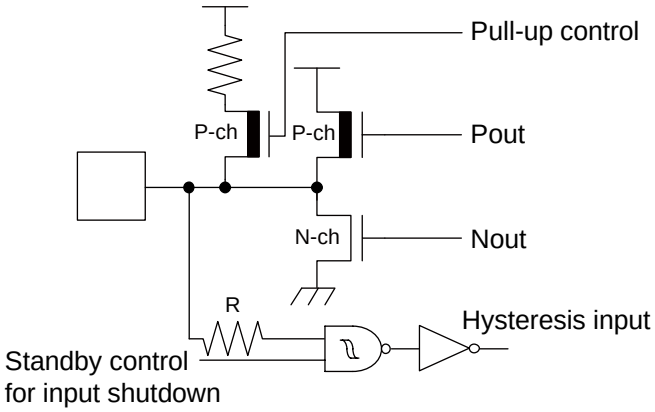
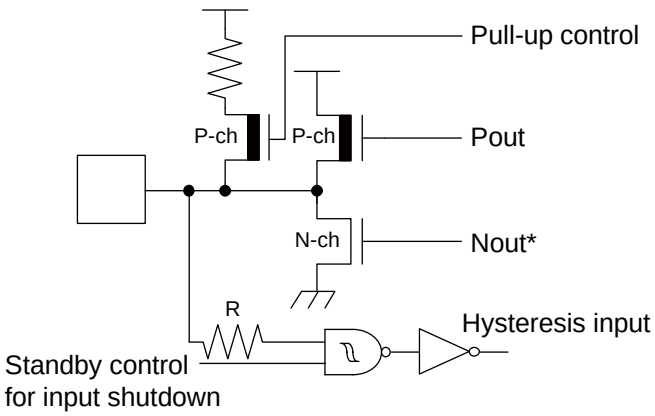
Features		CY96690	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
64.5KB + 32KB	8KB	CY96F693R, CY96F693A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB	8KB	CY96F695R, CY96F695A	
256.5KB + 32KB	16KB	CY96F696R	
Package		LQFP-100 LQI100	
DMA		4ch	
USART		5ch	LIN-USART 0 to 2/4/5
	with automatic LIN-Header transmission/reception	2ch	LIN-USART 0/1
	with 16 byte RX- and TX-FIFO		
I^2C		1ch	I^2C 0
8/10-bit A/D Converter		27ch	AN 2 to 4/6 to 8/10 to 12/ 14 to 31
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	Yes	
	with ADC Pulse Detection	Yes	
16-bit Reload Timer (RLT)		5ch	RLT 0 to 3/6
16-bit Free-Running Timer (FRT)		2ch	FRT 0/1
16-bit Input Capture Unit (ICU)		6ch (5 channels for LIN-USART)	ICU 0/1/4 to 7 (ICU 0/1/4 to 6 for LIN-USART)
16-bit Output Compare Unit (OCU)		4ch	OCU 0 to 3
8/16-bit Programmable Pulse Generator (PPG)		10ch (16-bit) / 14ch (8-bit)	PPG 0 to 7/14/15
	with Timing point capture	Yes	
	with Start delay	Yes	
	with Ramp	No	
CAN Interface		1ch	CAN 0 32 Message Buffers
Stepping Motor Controller (SMC)		4ch	SMC 0 to 2/4
External Interrupts (INT)		16ch	INT 0 to 15
Non-Maskable Interrupt (NMI)		1ch	
Sound Generator (SG)		2ch	SG 0/1
LCD Controller		4COM × 36SEG	COM 0 to 3 SEG 0 to 4/7/ 11 to 28/30/33/36 to 45
Real Time Clock (RTC)		1ch	
I/O Ports		75 (Dual clock mode) 77 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

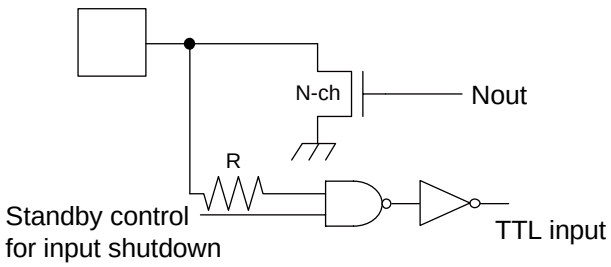
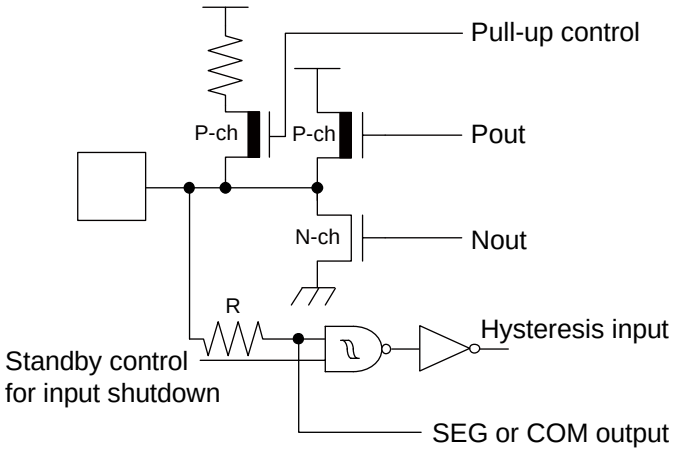
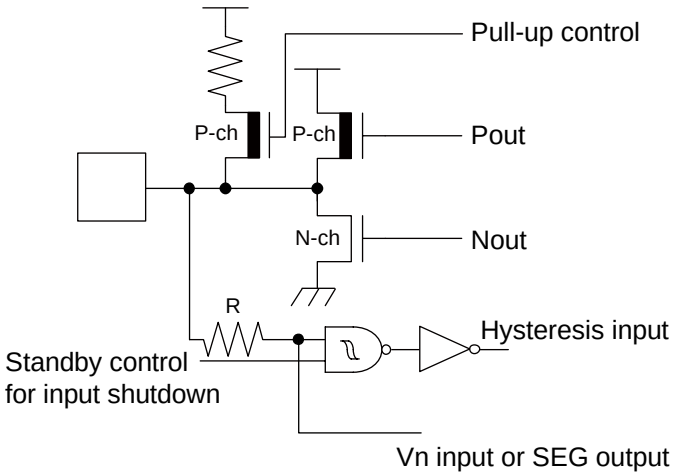
Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.*

Pin No.	I/O Circuit Type*	Pin Name
39	R	P08_7 / PWM2M1 / AN23 / PPG7_B
40	R	P09_0 / PWM1P2 / AN24
41	R	P09_1 / PWM1M2 / AN25
42	R	P09_2 / PWM2P2 / AN26
43	R	P09_3 / PWM2M2 / AN27
44	Supply	DV_{cc}
45	Supply	DV_{ss}
46	S	P10_0 / PWM1P4 / SIN2 / TIN3 / INT11 / AN28
47	R	P10_1 / PWM1M4 / SOT2 / TOT3 / AN29
48	S	P10_2 / PWM2P4 / SCK2 / PPG6 / AN30
49	R	P10_3 / PWM2M4 / PPG7 / AN31
50	Supply	Vcc
51	Supply	V_{ss}
52	O	DEBUG I/F
53	H	P17_0
54	C	MD
55	A	X0
56	A	X1
57	Supply	V_{ss}
58	B	P04_0 / X0A
59	B	P04_1 / X1A
60	C	RSTX
61	J	P11_0 / COM0
62	J	P11_1 / COM1 / PPG0_R
63	J	P11_2 / COM2 / PPG1_R
64	J	P11_3 / COM3 / PPG2_R
65	J	P11_4 / SEG0 / PPG3_R
66	J	P11_5 / SEG1 / PPG4_R
67	J	P11_6 / SEG2 / FRCK0_R
68	J	P11_7 / SEG3 / IN0_R
69	J	P12_0 / SEG4 / IN1_R
70	J	P12_3 / SEG7 / OUT2_R
71	J	P12_7 / SEG11 / INT1_R
72	J	P00_0 / SEG12 / INT3_R
73	J	P00_1 / SEG13 / INT4_R
74	J	P00_2 / SEG14 / INT5_R
75	Supply	V_{cc}
76	Supply	V_{ss}
77	J	P00_3 / SEG15 / INT6_R

Type	Circuit	Remarks
C		CMOS hysteresis input pin
F		Power supply input protection circuit
G		■ A/D converter ref+ (AVRH)/ ref- (AVRL) power supply input pin with protection circuit ■ Without protection circuit against V_{CC} for pins AVRH/AVRL
H		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ Automotive input with input shutdown function ■ Programmable pull-up resistor

Type	Circuit	Remarks
L		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ Automotive input with input shutdown function ■ Programmable pull-up resistor ■ Vn input or SEG output
M		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor
N		■ CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor *: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.

Type	Circuit	Remarks
O		■ Open-drain I/O ■ Output 25mA, Vcc = 2.7V ■ TTL input
P		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis inputs with input shutdown function ■ Programmable pull-up resistor ■ SEG or COM output
Q		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis inputs with input shutdown function ■ Programmable pull-up resistor ■ Vn input or SEG output

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

CY96690		
Pin Number	**USART Number**	**Normal Function**
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
46	USART2	SIN2
47		SOT2
48		SCK2
86	USART4	SIN4
87		SOT4
88		SCK4

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
40	$35C_H$	PPG2	Yes	40	Programmable Pulse Generator 2
41	358_H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354_H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350_H	PPG5	Yes	43	Programmable Pulse Generator 5
44	$34C_H$	PPG6	Yes	44	Programmable Pulse Generator 6
45	348_H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344_H	-	-	46	Reserved
47	340_H	-	-	47	Reserved
48	$33C_H$	-	-	48	Reserved
49	338_H	-	-	49	Reserved
50	334_H	-	-	50	Reserved
51	330_H	-	-	51	Reserved
52	$32C_H$	PPG14	Yes	52	Programmable Pulse Generator 14
53	328_H	PPG15	Yes	53	Programmable Pulse Generator 15
54	324_H	-	-	54	Reserved
55	320_H	-	-	55	Reserved
56	$31C_H$	-	-	56	Reserved
57	318_H	-	-	57	Reserved
58	314_H	RLT0	Yes	58	Reload Timer 0
59	310_H	RLT1	Yes	59	Reload Timer 1
60	$30C_H$	RLT2	Yes	60	Reload Timer 2
61	308_H	RLT3	Yes	61	Reload Timer 3
62	304_H	-	-	62	Reserved
63	300_H	-	-	63	Reserved
64	$2FC_H$	RLT6	Yes	64	Reload Timer 6
65	$2F8_H$	ICU0	Yes	65	Input Capture Unit 0
66	$2F4_H$	ICU1	Yes	66	Input Capture Unit 1
67	$2F0_H$	-	-	67	Reserved
68	$2EC_H$	-	-	68	Reserved
69	$2E8_H$	ICU4	Yes	69	Input Capture Unit 4
70	$2E4_H$	ICU5	Yes	70	Input Capture Unit 5
71	$2E0_H$	ICU6	Yes	71	Input Capture Unit 6
72	$2DC_H$	ICU7	Yes	72	Input Capture Unit 7
73	$2D8_H$	-	-	73	Reserved
74	$2D4_H$	-	-	74	Reserved
75	$2D0_H$	-	-	75	Reserved
76	$2CC_H$	-	-	76	Reserved
77	$2C8_H$	OCU0	Yes	77	Output Compare Unit 0
78	$2C4_H$	OCU1	Yes	78	Output Compare Unit 1
79	$2C0_H$	OCU2	Yes	79	Output Compare Unit 2
80	$2BC_H$	OCU3	Yes	80	Output Compare Unit 3
81	$2B8_H$	-	-	81	Reserved

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
124	$20C_H$	-	-	124	Reserved
125	208_H	-	-	125	Reserved
126	204_H	-	-	126	Reserved
127	200_H	-	-	127	Reserved
128	$1FC_H$	-	-	128	Reserved
129	$1F8_H$	-	-	129	Reserved
130	$1F4_H$	-	-	130	Reserved
131	$1F0_H$	-	-	131	Reserved
132	$1EC_H$	-	-	132	Reserved
133	$1E8_H$	FLASHA	Yes	133	Flash memory A interrupt
134	$1E4_H$	-	-	134	Reserved
135	$1E0_H$	-	-	135	Reserved
136	$1DC_H$	-	-	136	Reserved
137	$1D8_H$	-	-	137	Reserved
138	$1D4_H$	-	-	138	Reserved
139	$1D0_H$	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	$1CC_H$	ADCPD0	No	140	A/D Converter 0 - Pulse detection
141	$1C8_H$	-	-	141	Reserved
142	$1C4_H$	-	-	142	Reserved
143	$1C0_H$	-	-	143	Reserved

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} . Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.8 Pin Handling when not using the A/D Converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

13.10 Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

13.11 SMC Power Supply Pins

All DVcc /DVss pins must be set to the same level as the Vcc /Vss pins.

Note that the SMC I/O pin state is undefined if DV_{CC} is powered on and V_{CC} is below 3V. To avoid this, V_{CC} must always be powered on before DV_{CC}.

DV_{CC}/DV_{SS} must be applied when using SMC I/O pin as GPIO.

13.12 Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to V_{cc} or V_{ss} pin and provide a low-impedance connection.

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode[3]	I_{CCH}	Vcc	-	-	20	60	µA	T_A = +25°C
				-	-	880	µA	T_A = +105°C
Flash Power Down current	$I_{CCFLASHPD}$		-	-	36	70	µA	
Power supply current for active Low Voltage detector[4]	I_{CCLVD}		Low voltage detector enabled	-	5	-	µA	T_A = +25°C
				-	-	12.5	µA	T_A = +105°C
Flash Write/ Erase current[5]	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +105°C

[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

[2]: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32 kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

[3]: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

[4]: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

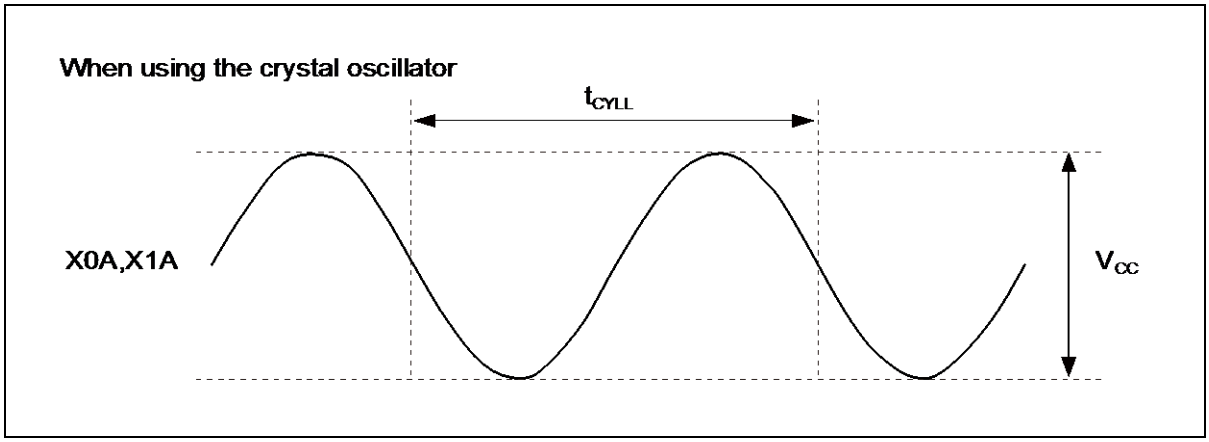
[5]: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

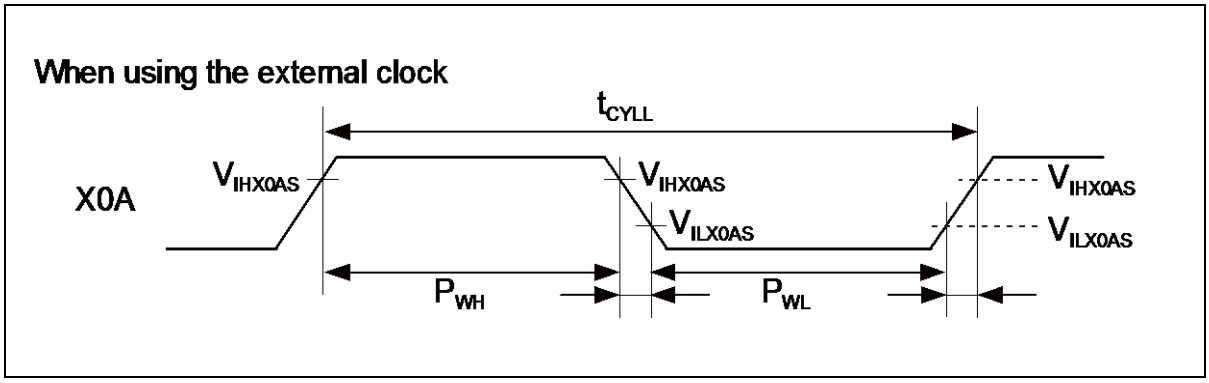
Parameters	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH4}	4mA type	$4.5V \le (D)V_{CC} \le 5.5V$ I_{OH} = -4mA	$(D)V_{CC}$- 0.5	-	$(D)V_{CC}$	V	
			$2.7V \le (D)V_{CC} < 4.5V$ I_{OH} = -1.5mA					
	V_{OH30}	High Drive type*	$4.5V \le DV_{CC} \le 5.5V$ I_{OH} = -52mA	DV_{CC}- 0.5	-	DV_{CC}	V	T_A = -40°C
			$2.7V \le DV_{CC} < 4.5V$ I_{OH} = -18mA					
			$4.5V \le DV_{CC} \le 5.5V$ I_{OH} = -39mA					T_A = +25°C
			$2.7V \le DV_{CC} < 4.5V$ I_{OH} = -16mA					
			$4.5V \le DV_{CC} \le 5.5V$ I_{OH} = -32mA					T_A = +85°C
			$2.7V \le DV_{CC} < 4.5V$ I_{OH} = -14.5mA					
			$4.5V \le DV_{CC} \le 5.5V$ I_{OH} = -30mA					T_A = +105°C
			$2.7V \le DV_{CC} < 4.5V$ I_{OH} = -14mA					
	V_{OH3}	3mA type	$4.5V \le V_{CC} \le 5.5V$ I_{OH} = -3mA	V_{CC}- 0.5	-	V_{CC}	V	
			$2.7V \le V_{CC} < 4.5V$ I_{OH} = -1.5mA					

14.4.2 *Sub Clock Input Characteristics*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	

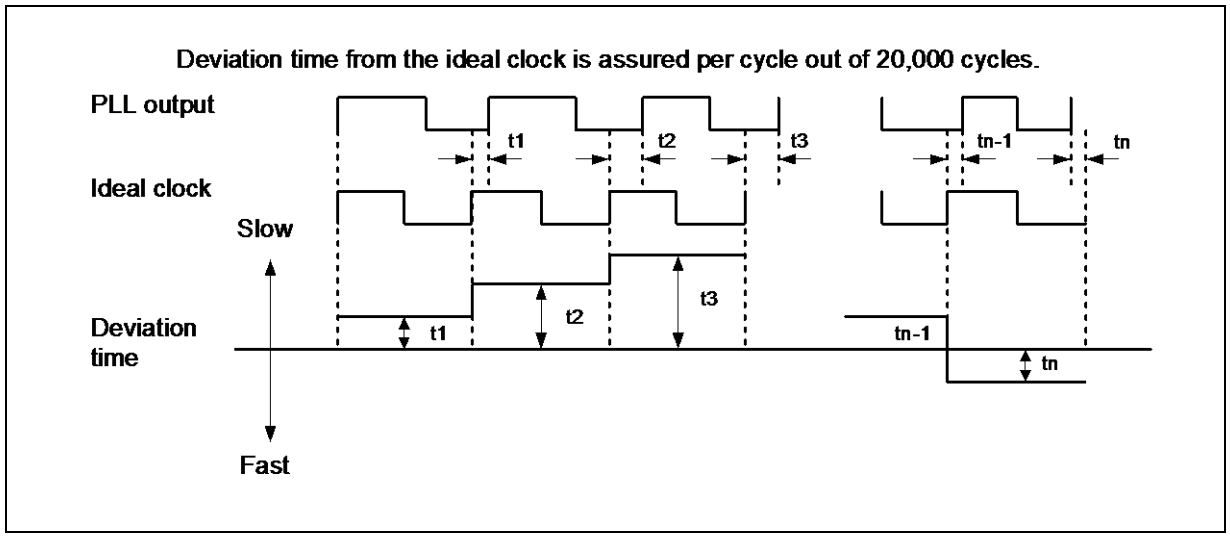




14.4.5 *Operating Conditions of PLL*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

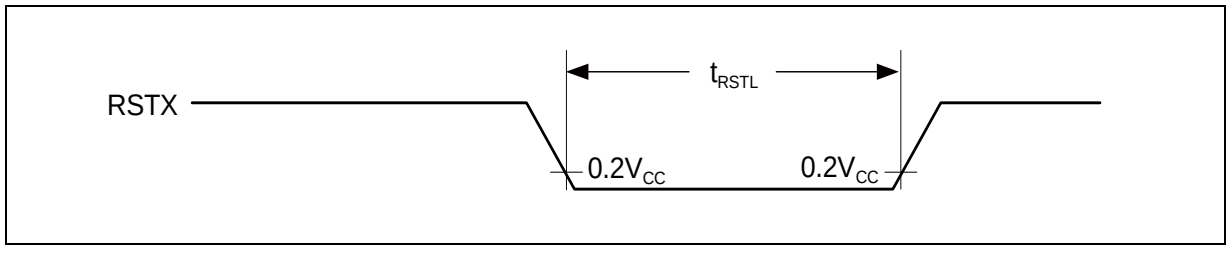
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz



14.4.6 *Reset Input*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs



14.4.8 *USART Timing*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C, C_L=50pF)

Parameter	Symbol	Pin Name	Conditions	4.5V ≤ V_{CC} < 5.5V		2.7V ≤ V_{CC} < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode	$4t_{CLKP1}$	-	$4t_{CLKP1}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N \times t_{CLKP1} - 20^*$	-	$N \times t_{CLKP1} - 30^*$	-	ns
SIN →SCK ↑setup time	t_{IVSHI}	SCKn, SINn		t_{CLKP1}+ 45	-	t_{CLKP1}+ 55	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn	External shift clock mode	t_{CLKP1}+ 10	-	t_{CLKP1}+ 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn		t_{CLKP1}+ 10	-	t_{CLKP1}+ 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2t_{CLKP1}$+ 45	-	$2t_{CLKP1}$+ 55	ns
SIN →SCK ↑setup time	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2+ 10	-	t_{CLKP1}/2+ 10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1}+ 10	-	t_{CLKP1}+ 10	-	ns
SCK fall time	t_F	SCKn		-	20	-	20	ns
SCK rise time	t_R	SCKn		-	20	-	20	ns

Notes:

- *AC characteristic in CLK synchronized mode.*
- *C_L is the load capacity value of pins when testing.*
- *Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "CY96600 series HARDWARE MANUAL".*
- *t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns*
- *These characteristics only guarantee the same relocate port number.*

For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on t_{SCYC} and can be calculated as follows:

- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then N = k, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then N = k + 1, where k is an integer > 1

Examples:

t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}$, $6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}$, $8 \times t_{CLKP1}$	4

14.4.10 *I²C Timing*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Typical Mode		High-Speed Mode[4]		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	C_L = 50pF, R = (Vp/I_{OL})[1]	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45[2]	0	0.9[3]	µs
Data setup time SDA ↓ ↑ →SCL ↑	t_{SUDAT}		250	-	100	-	ns
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs
Bus free time between "STOP condition" and "START condition"	t_{BUS}		4.7	-	1.3	-	µs
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	-	0	(1-1.5) ×t_{CLKP1}[5]	0	(1-1.5) ×t_{CLKP1}[5]	ns

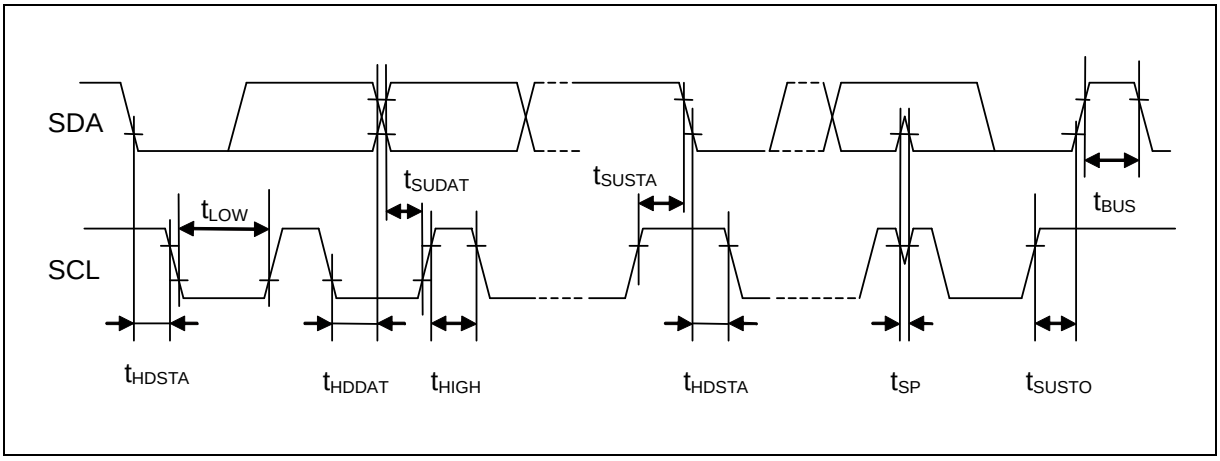
[1]: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

[2]: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

[3]: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250ns".

[4]: For use at over 100 kHz, set the peripheral clock1 (CLKP1) to at least 6 MHz.

[5]: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time.



14.5 A/D Converter

14.5.1 *Electrical Characteristics for the A/D Converter*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

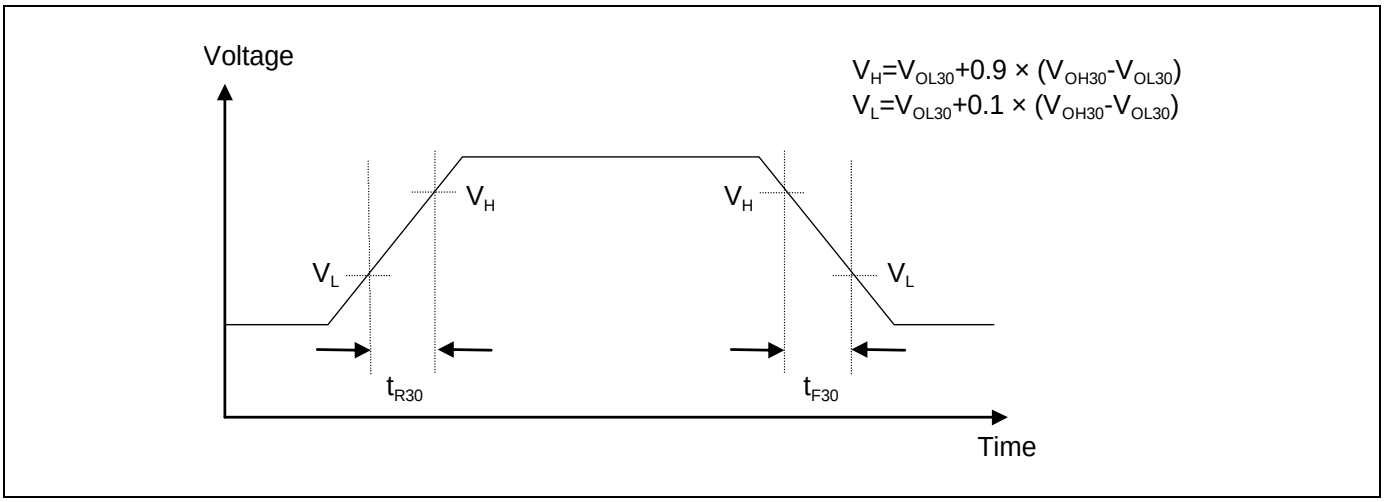
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	AVRL+ 0.5LSB	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	AVRH- 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} < 4.5V
Sampling time*	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} < 4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH and AVRL)	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	AN2 to 4, 6 to 8, 10 to 12, 14, 15	-	-	16.0	pF	Normal outputs
		AN16 to 31	-	-	17.8	pF	High current outputs
Analog impedance	R_{VIN}	ANn	-	-	2050	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
			-	-	3600	Ω	2.7V ≤ AV_{CC} < 4.5V
Analog port input current (during conversion)	I_{AIN}	AN2 to 4, 6 to 8, 10 to 12, 14, 15	- 0.3	-	+ 0.3	µA	AV_{SS} , AVRL < V_{AIN} < AV_{CC}, AVRH
		AN16 to 31	- 3.0	-	+ 3.0	µA	
Analog input voltage	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC} - 0.1	-	AV_{CC}	V	
	-	AVRL	AV_{SS}	-	AV_{SS}+ 0.1	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

14.6 High Current Output Slew Rate

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise/fall time	t_{R30}, t_{F30}	P08_m, P09_m, P10_m	Outputs driving strength set to "30mA"	15	-	75	ns	C_L=85pF



14.7 Low Voltage Detection Function Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage[1]	V_{DL0}	CILCR:LVL = 0000_B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001_B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010_B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011_B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100_B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111_B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001_B	3.91	4.20	4.49	V
Power supply voltage change rate[2]	dV/dt	-	- 0.004	-	+ 0.004	V/µs
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	µs
Detection delay time	t_d	-	-	-	30	µs

[1]: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

[2]: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.

14.8 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	-	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time		-	-	25	400	µs	Not including system-level overhead time.
Chip erase time		-	-	8.31	40.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[1].

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20 [2]
10,000	10 [2]
100,000	5 [2]

[1]: See "14.7 Low Voltage Detection Function Characteristics".

[2]: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

Page	Section	Change Results
66	16. Ordering Information	Revised Marketing Part Numbers as follows: Before) **MCU with CAN controller** MB96F693RBPMC-GSE1 MB96F693RBPMC-GSE2 MB96F695RBPMC-GSE1 MB96F695RBPMC-GSE2 MB96F696RBPMC-GSE1 MB96F696RBPMC-GSE2 **MCU without CAN controller** MB96F693ABPMC-GSE1 MB96F693ABPMC-GSE2 MB96F695ABPMC-GSE1 MB96F695ABPMC-GSE2 After) **MCU with CAN controller** CY96F693RBPMC-GS-UJE1 CY96F696RBPMC-GS-UJE1 CY96F696RBPMC-GS-UJE2 **MCU without CAN controller** CY96F693ABPMC-GS-UJE1 CY96F693ABPMC-GS-UJE2