Infineon Technologies - MB96F695RBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	77
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f695rbpmc-gse2

- Extended support for LIN-Protocol (with 16-byte FIFO for selected channels) to reduce interrupt load.

I²C

- Up to 400kbps
- Master and Slave functionality, 7-bit and 10-bit addressing

A/D Converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function
- Scan disable Function
- ADC Pulse Detection Function

Source Clock Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

Hardware Watchdog Timer

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free-Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
- Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with Free-running Timer occurs
- A pair of compare registers can be used to generate an output signal

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as 2 ×8-bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture
- Start delay

Stepping Motor Controller

- Stepping Motor Controller with integrated high current output drivers
- Four high current outputs for each channel
- Two synchronized 8/10-bit PWMs per channel
- Internal prescaling for PWM clock: 1, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/16 of peripheral clock
- Dedicated power supply for high current output drivers

LCD Controller

- LCD controller with up to 4COM ×36SEG
- Internal or external voltage generation
- Duty cycle: Selectable from options: 1/2, 1/3 and 1/4
- Fixed 1/3 bias
- Programmable frame period
- Clock source selectable from four options (main clock, peripheral clock, subclock or RC oscillator clock)
- Internal divider resistors or external divider resistors
- On-chip data memory for display
- LCD display can be operated in Timer Mode
- Blank display: selectable
- All SEG, COM and V pins can be switched between general and specialized purposes

Sound Generator

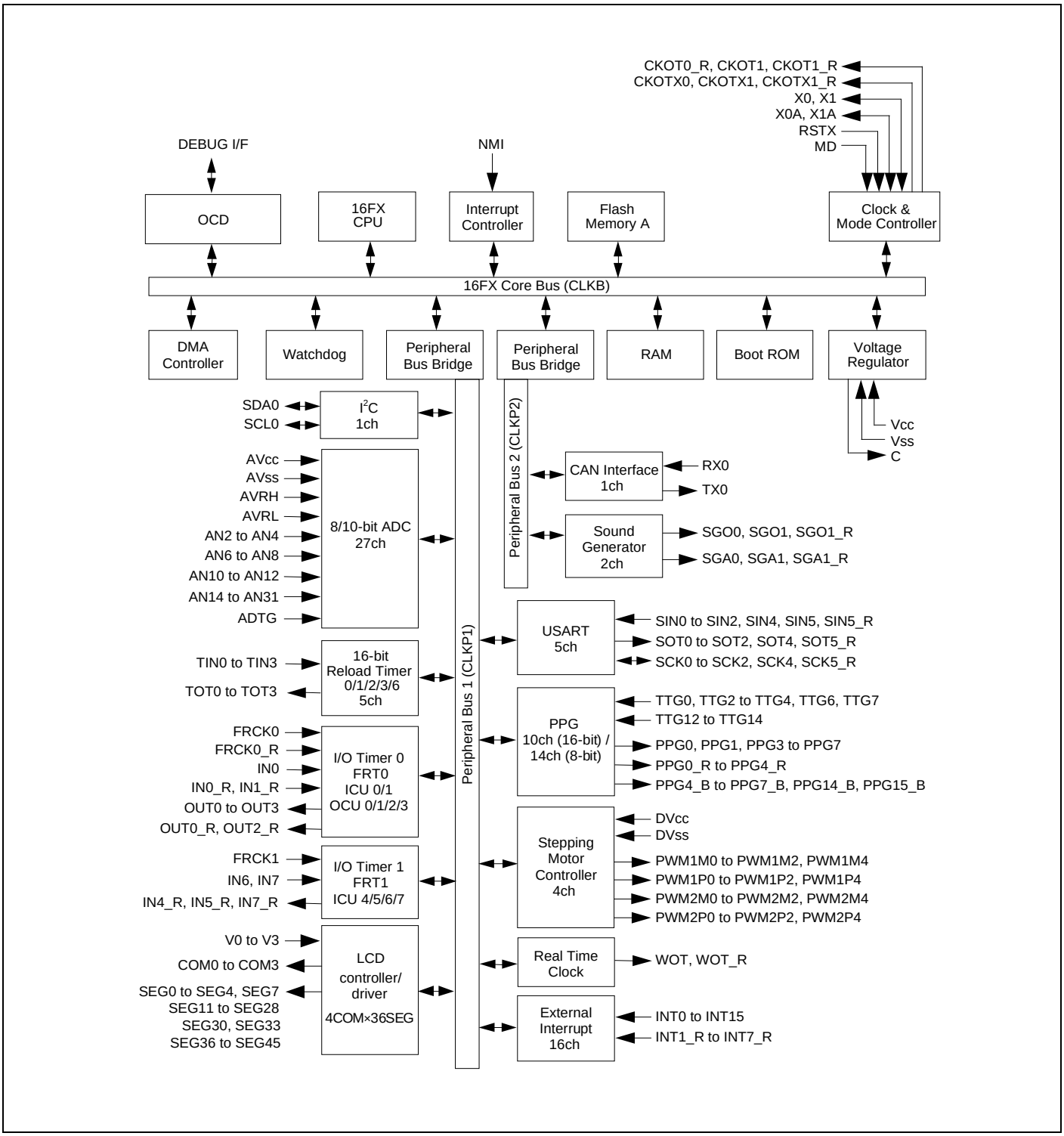
- 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter
- PWM clock by internal prescaler: 1, 1/2, 1/4, 1/8 of peripheral clock

Real Time Clock

- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day

Contents

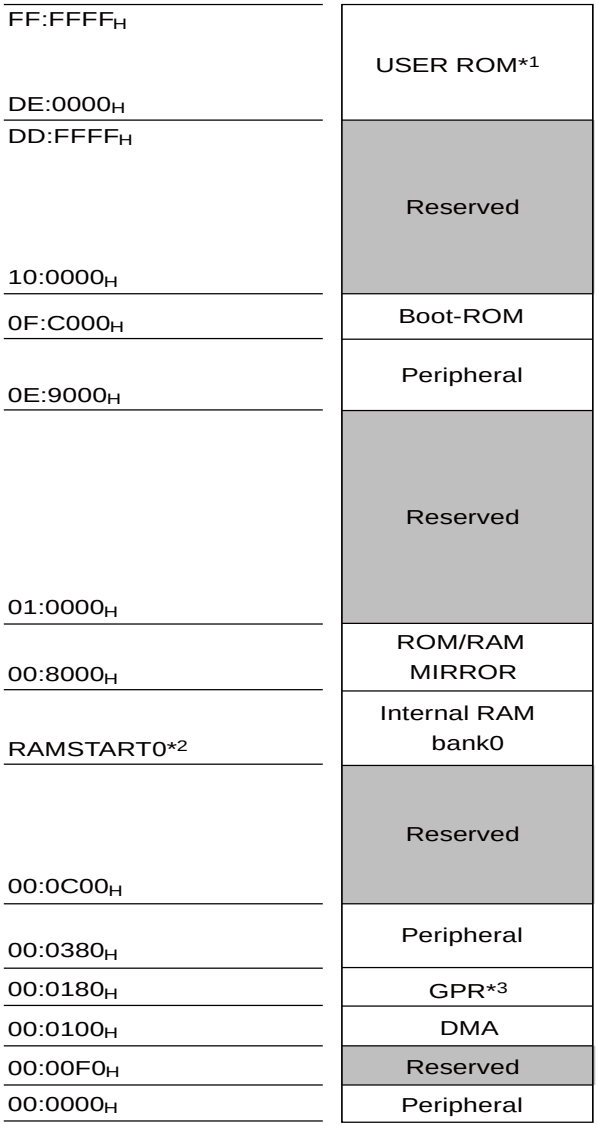
2. Block Diagram



Pin Name	Feature	Description
SGOn_R	Sound Generator	Relocated Sound Generator sound/tone output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vn	LCD	LCD voltage reference pin
V_{cc}	Supply	Power supply pin
V_{ss}	Supply	Power supply pin
WOT	RTC	Real Time clock output pin
WOT_R	RTC	Relocated Real Time clock output pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin

Pin No.	I/O Circuit Type*	Pin Name
39	R	P08_7 / PWM2M1 / AN23 / PPG7_B
40	R	P09_0 / PWM1P2 / AN24
41	R	P09_1 / PWM1M2 / AN25
42	R	P09_2 / PWM2P2 / AN26
43	R	P09_3 / PWM2M2 / AN27
44	Supply	DV_{cc}
45	Supply	DV_{ss}
46	S	P10_0 / PWM1P4 / SIN2 / TIN3 / INT11 / AN28
47	R	P10_1 / PWM1M4 / SOT2 / TOT3 / AN29
48	S	P10_2 / PWM2P4 / SCK2 / PPG6 / AN30
49	R	P10_3 / PWM2M4 / PPG7 / AN31
50	Supply	Vcc
51	Supply	V_{ss}
52	O	DEBUG I/F
53	H	P17_0
54	C	MD
55	A	X0
56	A	X1
57	Supply	V_{ss}
58	B	P04_0 / X0A
59	B	P04_1 / X1A
60	C	RSTX
61	J	P11_0 / COM0
62	J	P11_1 / COM1 / PPG0_R
63	J	P11_2 / COM2 / PPG1_R
64	J	P11_3 / COM3 / PPG2_R
65	J	P11_4 / SEG0 / PPG3_R
66	J	P11_5 / SEG1 / PPG4_R
67	J	P11_6 / SEG2 / FRCK0_R
68	J	P11_7 / SEG3 / IN0_R
69	J	P12_0 / SEG4 / IN1_R
70	J	P12_3 / SEG7 / OUT2_R
71	J	P12_7 / SEG11 / INT1_R
72	J	P00_0 / SEG12 / INT3_R
73	J	P00_1 / SEG13 / INT4_R
74	J	P00_2 / SEG14 / INT5_R
75	Supply	V_{cc}
76	Supply	V_{ss}
77	J	P00_3 / SEG15 / INT6_R

7. Memory Map



*1: For details about USER ROM area, see "User ROM Memory Map for Flash Devices" on the following pages.

*2: For RAMSTART addresses, see the table on the next page.

*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

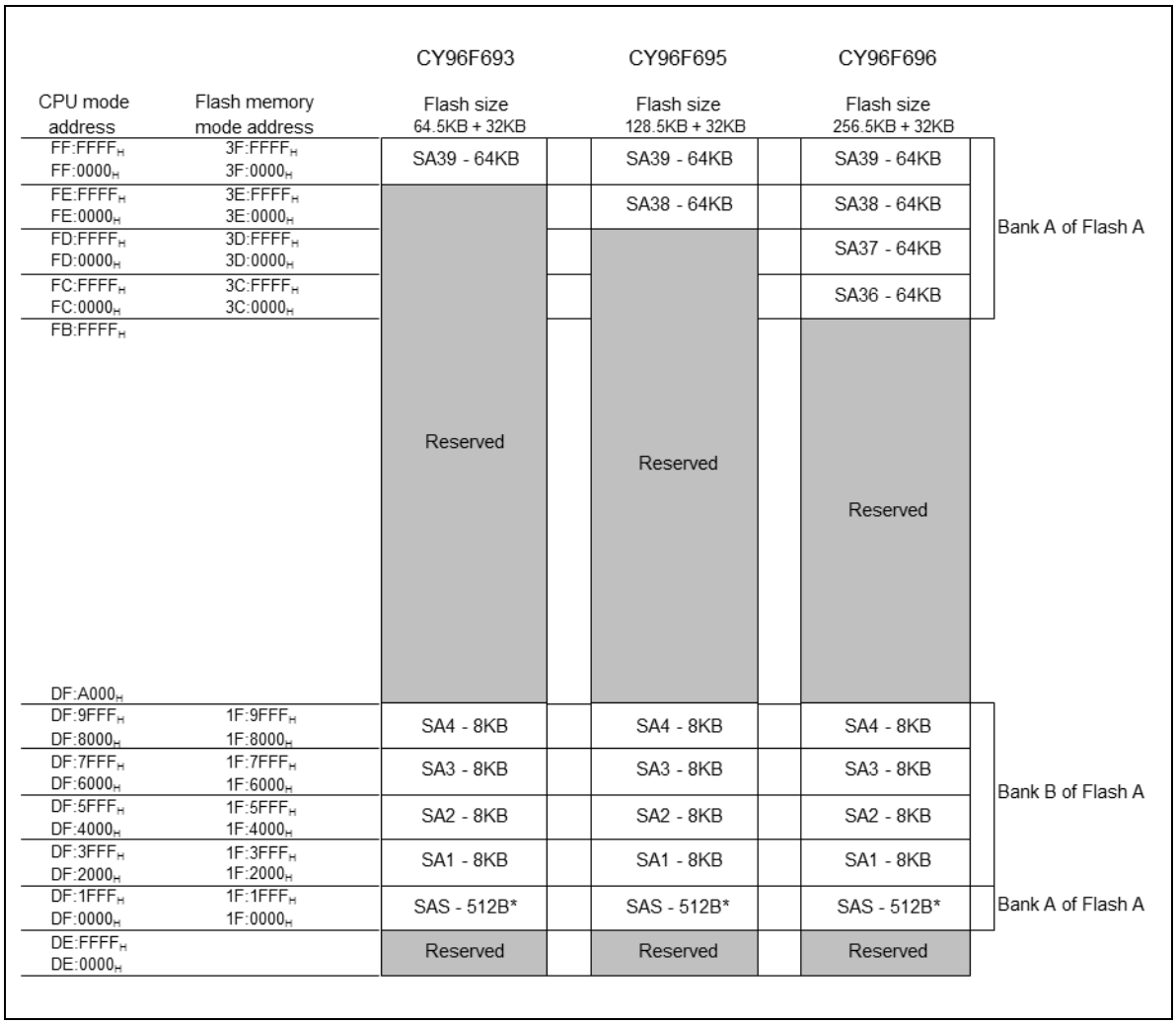
The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

8. RAM Start Addresses

Devices	Bank 0 RAM Size	RAMSTART0
CY96F693 CY96F695	8KB	$00:6200_H$
CY96F696	16KB	$00:4200_H$

9. User ROM Memory Map for Flash Devices



CPU mode address	Flash memory mode address	CY96F693 Flash size 64.5KB + 32KB	CY96F695 Flash size 128.5KB + 32KB	CY96F696 Flash size 256.5KB + 32KB	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	Reserved	SA38 - 64KB	SA38 - 64KB	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$		Reserved	SA37 - 64KB	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$			SA36 - 64KB	
FB:FFFF$_H$				Reserved	
DF:A000$_H$					
DF:9FFF$_H$ DF:8000$_H$	1F:9FFF$_H$ 1F:8000$_H$	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SAS - 512B*	SAS - 512B*	SAS - 512B*	Bank A of Flash A
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	Reserved	

*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS cannot be used for E^{2}PROM emulation.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

CY96690		
Pin Number	**USART Number**	**Normal Function**
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
46	USART2	SIN2
47		SOT2
48		SCK2
86	USART4	SIN4
87		SOT4
88		SCK4

13. Handling Devices

Special Care is Required for the following when Handling the Device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (Vcc/Vss)
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication
- Mode Pin (MD)

13.1 Latch-Up Prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between Vcc pins and Vss pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

13.2 Unused Pins Handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register

PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent

damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than 2kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with

either input disabled or external pull-up/pull-down resistor as described above.

13.3 External Clock Usage

The permitted frequency range of an external clock depends on the oscillator type and configuration.

See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

13.3.1 *Single Phase External Clock for Main Oscillator*

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open.
And supply 1.8V power to the external clock.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} . Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.8 Pin Handling when not using the A/D Converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

13.10 Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

13.11 SMC Power Supply Pins

All DVcc /DVss pins must be set to the same level as the Vcc /Vss pins.

Note that the SMC I/O pin state is undefined if DV_{CC} is powered on and V_{CC} is below 3V. To avoid this, V_{CC} must always be powered on before DV_{CC}.

DV_{CC}/DV_{SS} must be applied when using SMC I/O pin as GPIO.

13.12 Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to V_{cc} or V_{ss} pin and provide a low-impedance connection.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage[1]	V_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	
Analog power supply voltage[1]	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$[2]
Analog reference voltage[1]	AVRH, AVRL	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL ≥ AV_{SS}
SMC Power supply[1]	DV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC} = DV_{CC}$[2]
LCD power supply voltage[1]	V0 to V3	-	V_{SS} - 0.3	V_{SS} + 6.0	V	V0 to V3 must not exceed V_{CC}
Input voltage[1]	V_I	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq (D)V_{CC} + 0.3V$[3]
Output voltage[1]	V_O	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq (D)V_{CC} + 0.3V$[3]
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins [4]
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	-	-	25	mA	Applicable to general purpose I/O pins [4]
"L" level maximum output current	I_{OL}	-	-	15	mA	Normal port
	I_{OLSMC}	T_A= -40°C	-	52	mA	High current port
		T_A= +25°C	-	39	mA	
		T_A= +85°C	-	32	mA	
		T_A= +105°C	-	30	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	Normal port
	$I_{OLAVSMC}$	T_A= -40°C	-	40	mA	High current port
		T_A= +25°C	-	30	mA	
		T_A= +85°C	-	25	mA	
		T_A= +105°C	-	23	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	50	mA	Normal port
	ΣI_{OLSMC}	-	-	260	mA	High current port
"L" level average overall output current	ΣI_{OLAV}	-	-	25	mA	Normal port
	$\Sigma I_{OLAVSMC}$	-	-	170	mA	High current port

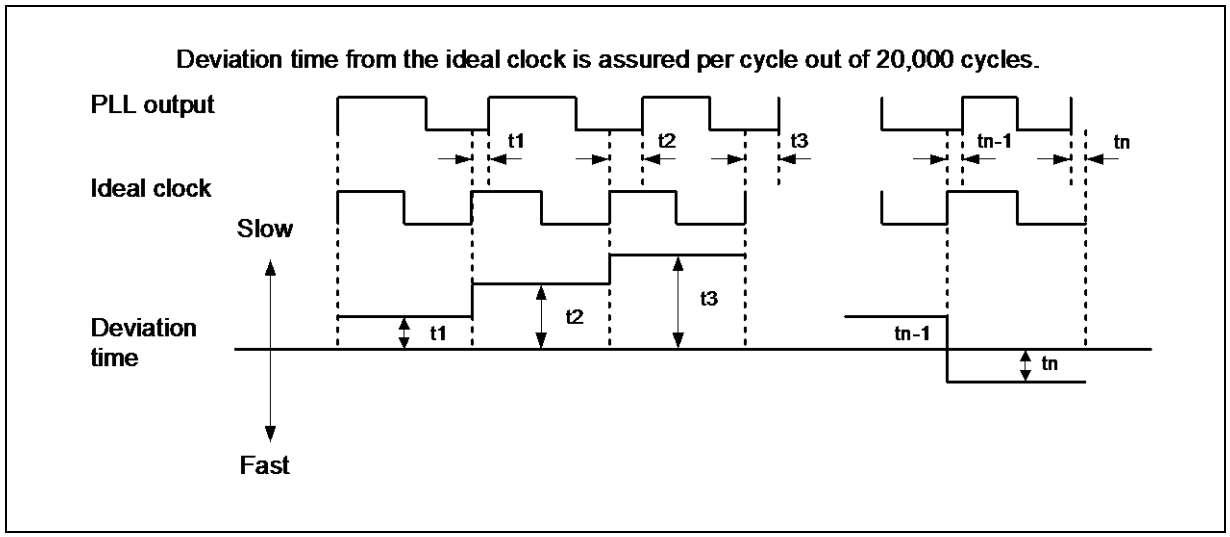
Parameters	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH4}	4mA type	$4.5V \le (D)V_{CC} \le 5.5V$ I_{OH} = -4mA	$(D)V_{CC}$- 0.5	-	$(D)V_{CC}$	V	
			$2.7V \le (D)V_{CC} < 4.5V$ I_{OH} = -1.5mA					
	V_{OH30}	High Drive type*	$4.5V \le DV_{CC} \le 5.5V$ I_{OH} = -52mA	DV_{CC}- 0.5	-	DV_{CC}	V	T_A = -40°C
			$2.7V \le DV_{CC} < 4.5V$ I_{OH} = -18mA					
			$4.5V \le DV_{CC} \le 5.5V$ I_{OH} = -39mA					T_A = +25°C
			$2.7V \le DV_{CC} < 4.5V$ I_{OH} = -16mA					
			$4.5V \le DV_{CC} \le 5.5V$ I_{OH} = -32mA					T_A = +85°C
			$2.7V \le DV_{CC} < 4.5V$ I_{OH} = -14.5mA					
			$4.5V \le DV_{CC} \le 5.5V$ I_{OH} = -30mA					T_A = +105°C
			$2.7V \le DV_{CC} < 4.5V$ I_{OH} = -14mA					
	V_{OH3}	3mA type	$4.5V \le V_{CC} \le 5.5V$ I_{OH} = -3mA	V_{CC}- 0.5	-	V_{CC}	V	
			$2.7V \le V_{CC} < 4.5V$ I_{OH} = -1.5mA					

Parameters	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL4}	4mA type	4.5V ≤ (D)V_{CC} ≤ 5.5V I_{OL} = +4mA	-	-	0.4	V	
			2.7V ≤ (D)V_{CC} < 4.5V I_{OL} = +1.7mA					
	V_{OL30}	High Drive type*	4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +52mA	-	-	0.5	V	T_A = -40°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +22mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +39mA					T_A = +25°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +18mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +32mA					T_A = +85°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +14mA					
			4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +30mA					T_A = +105°C
			2.7V ≤ DV_{CC} < 4.5V I_{OL} = +13.5mA					
	V_{OL3}	3mA type	2.7V ≤ V_{CC} < 5.5V I_{OL} = +3mA	-	-	0.4	V	
	V_{OLD}	DEBUG I/F	V_{CC} = 2.7V I_{OL} = +25mA	0	-	0.25	V	
Input leak current	I_{IL}	Pnn_m	V_{SS} < V_I < V_{CC} AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 1	-	+ 1	µA	Single port pin except high current output I/O for SMC
		P08_m, P09_m, P10_m	DV_{SS} < V_I < DV_{CC} AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 3	-	+ 3	µA	
Total LCD leak current	$\Sigma\|I_{ILCD}\|$	All SEG/ COM pin	V_{CC} = 5.0V	-	0.5	10	µA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V2, V2 and V1, V1 and V0	V_{CC} = 5.0V	6.25	12.5	25	kΩ	

14.4.5 *Operating Conditions of PLL*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

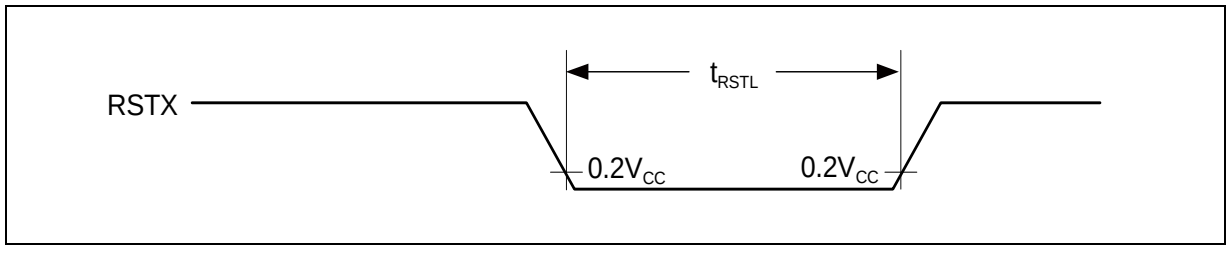
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz



14.4.6 *Reset Input*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

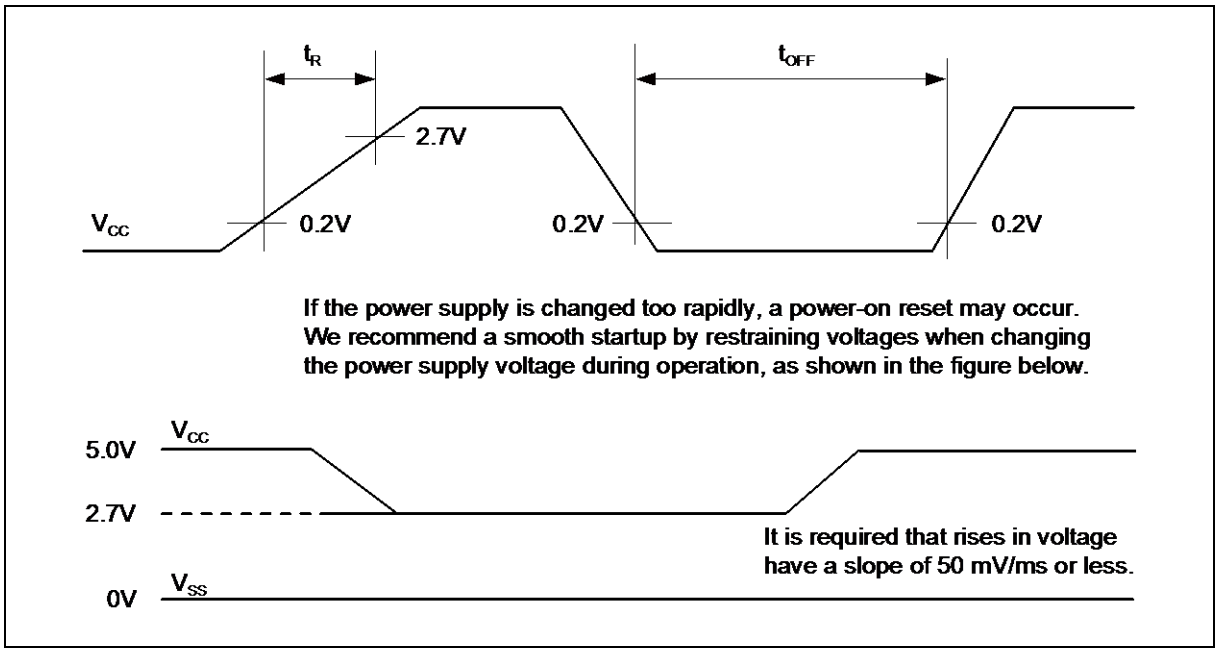
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs



14.4.7 *Power-on Reset Timing*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms



14.5 A/D Converter

14.5.1 *Electrical Characteristics for the A/D Converter*

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	AVRL+ 0.5LSB	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	AVRH- 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} < 4.5V
Sampling time*	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} < 4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH and AVRL)	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	AN2 to 4, 6 to 8, 10 to 12, 14, 15	-	-	16.0	pF	Normal outputs
		AN16 to 31	-	-	17.8	pF	High current outputs
Analog impedance	R_{VIN}	ANn	-	-	2050	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
			-	-	3600	Ω	2.7V ≤ AV_{CC} < 4.5V
Analog port input current (during conversion)	I_{AIN}	AN2 to 4, 6 to 8, 10 to 12, 14, 15	- 0.3	-	+ 0.3	µA	AV_{SS} , AVRL < V_{AIN} < AV_{CC}, AVRH
		AN16 to 31	- 3.0	-	+ 3.0	µA	
Analog input voltage	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC} - 0.1	-	AV_{CC}	V	
	-	AVRL	AV_{SS}	-	AV_{SS}+ 0.1	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

14.8 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	-	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time		-	-	25	400	µs	Not including system-level overhead time.
Chip erase time		-	-	8.31	40.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[1].

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20 [2]
10,000	10 [2]
100,000	5 [2]

[1]: See "14.7 Low Voltage Detection Function Characteristics".

[2]: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

Page	Section	Change Results
61	8. Flash Memory Write/Erase Characteristics	Changed the Value of “Sector erase time”
		Added “Security Sector” to “Sector erase time”
		Changed the Parameter “Half word (16 bit) write time” “Word (16-bit) write time”
		Changed the Value of “Chip erase time”
		Changed the Remarks of “Sector erase time” Excludes write time prior to internal erase Includes write time prior to internal erase
		Added the Note and annotation *1
		Deleted “(targeted value)” from title “ Write/Erase cycles and data hold time”
62 to 63	■EXAMPLE CHARACTERISTICS	Added a section
65	■ORDERING INFORMATION	Changed part number MCU with CAN controller MB96F696RAPMC-GSE1* → MB96F696RBPMC-GSE1 MB96F696RAPMC-GSE2* → MB96F696RBPMC-GSE2
		Added part number MCU with CAN controller MB96F693RBPMC-GSE1 MB96F693RBPMC-GSE2 MB96F695RBPMC-GSE1 MB96F695RBPMC-GSE2 MCU without CAN controller MB96F693ABPMC-GSE1 MB96F693ABPMC-GSE2 MB96F695ABPMC-GSE1 MB96F695ABPMC-GSE2
Revision 1.1		
-	-	Company name and layout design change

NOTE: Please see “Document History” about later revised information.

Page	Section	Change Results
Rev.*B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
7, 9, 66,67	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-100P-M20 → LQI100

Document History

Document Title: CY96690 Series F²MC-16FX 16-Bit Proprietary Microcontroller
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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	TORS	01/31/2014	Migrated to Cypress and assigned document number 002-04717. No change to document contents or format.
*A	5148388	TORS	09/22/2016	Updated to Cypress template
*B	6006770	MIYH	12/28/2017	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension For details, please see 18. Major Changes.