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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I <sup>2</sup> C, LINbus, SD, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	63
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2hg4e0agv20000



#### **VBAT**

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- **■**RTC
- ■32 kHz oscillation circuit
- ■Power-on circuit
- ■Back up register : 32 bytes
- ■Port circuit

#### Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

### **Unique ID**

Unique value of the device (41-bit) is set.

### **Power Supply**

Two Power Supplies

■ Wide range voltage: VCC = 2.7 V to 5.5 V ■ Power supply for VBAT: VBAT = 2.7 V to 5.5 V



	Pin Nu	ımber		Pin Name	I/O Circuit	Pin State								
LQFP120	LQFP100	LQFP80	FBGA121	Fill Name	Type	Туре								
00	24	24	1.4	P46	Р	C								
39	34	24	L4	X0A	Р	S								
40	35	25	K4	P47	Q	Т								
40	33	23	11.4	X1A	Q	'								
41	36	26	K5	P48	0	U								
			110	VREGCTL										
42	37	27	K6	P49	0	U								
				VWAKEUP										
43	38	28	L5	VBAT	-	-								
44	39	29	L6	C	-	-								
45	40	30	L7	VSS	-	-								
46	41	31	K7	VCC	-	-								
				P4B										
47	42	32	J6	TIOB1_0	E	1								
				SCS7_1										
				MAD03_0										
				P4C										
				TIOB2_0	-									
48	8 43	43	43	43	43	43	43	3 43	43	33	J7	SCK7_1	N	1
				(SCL7_1)	_									
				AIN1_2										
				MAD04_0		+								
				P4D										
				TIOB3_0	-									
40	4.4	0.4	10	SOT7_1 (SDA7_1)	N	12								
49	44	34	J8	(SDA7_1)	N	K								
				BIN1_2	1									
				INT13_2	-									
				MAD05_0 P4E										
				TIOB4_0	-									
				SIN7_1	-									
				ZIN1_2	-									
50	45	35	K8	FRCK1_1	I	Q								
				INT11_1	-									
				WKUP2	-									
				MAD06_0	-									
				P70										
				TIOA4_2										
51	-	-	H6	AINO_1	Е	1								
				IC13_1										
				TX0_0										



	Pin Nu	ımber		Pin Name	I/O Circuit	Pin State					
LQFP120	LQFP100	LQFP80	FBGA121	Fill Name	Type	Туре					
				P20							
				AN18							
00	74		B11	AIN1_1	F	N/L					
89	74	-	BII	INT05_0		М					
				MAD24_0							
				RTO25_0							
90	75	60	A11	VSS	-	-					
91	76	61	A10	VCC	-	-					
				P0E							
				TIOB5_2							
92	77	62	B9	SCS6_1	L						
92	11	62	БЭ	IC13_0	L	I					
				S_CLK_0							
				MDQM1_0							
				P0D							
				TIOA5_2							
	78			SCK6_1							
93		78	78	78	78	93 78	63	A9	(SCL6_1)	L	1
				IC12_0							
				S_CMD_0							
				MDQM0_0	1						
				P0C							
				TIOA6_1	1						
				SOT6_1							
94	79	64	C8	(SDA6_1)	L	1					
				IC11_0							
				S_DATA1_0	-						
				MALE_0							
				P0B							
				TIOB6_1							
				SIN6_1							
95	80	65	В8	IC10_0	L	K					
				INT00_1							
				S_DATA0_0							
				MCSX0_0							
				P0A							
				SIN1_0							
				FRCK1_0	1						
96	81	66	A8	INT12_2	L	K					
				S_DATA3_0							
				MCSX1_0	1						



	Pin Number		Pin Name	I/O Circuit	Pin State												
LQFP120	LQFP100	LQFP80	FBGA121	i iii Naiile	Туре	Туре											
		67		P09													
		07		AN19													
	-		TRACED0														
				TIOA3_2													
97	82	07	D7	SOT1_0 (SDA1_0)	M	N											
		67		S_DATA2_0													
				MCSX5_0													
				IC23_1													
				P08													
				AN20													
				TRACED1													
98	83		C7	TIOB3_2	F	N											
90	03	-	C/	SCK1_0 (SCL1_0)	r	IN											
				MCSX4_0													
				IC22_1													
				P07													
				AN21													
				TRACED2													
00	0.4	84 -	-	-	-	-	-	-	-						TIOA0_2	1	
99	99   84									В7	SCK7_0	M	N				
													(SCL7_0)	_			
					MCLKOUT_0												
				IC21_1													
				P06													
				AN22													
				TRACED3													
100	85	_	A7	TIOB0_2	F	N											
100		-	65 -	-	-	_	$\Delta i$	SOT7_0		14							
							(SDA7_0)										
					MCSX3_0												
				IC20_1													
				P05													
				AN23	1												
				ADTG_0	1												
101	86	-	D6	TRACECLK	F	0											
				SIN7_0	-												
				INT01_1	-												
				MCSX2_0													
				FRCK2_1													
100	07	60	D.C	P04	_												
102	87	68	В6	TDO	Е	G											
				SWO P03													
103	88	69	C6	TMS	E	G											
103	00	09	00	SWDIO	-	G											
L	J	J		טוטאא													



					No No	
Pin Function	Pin Name	Function Description	LQFP 120	LQFP 100	LQFP 80	FBGA 121
	DTTI1X_0	Input signal controlling wave form	8	8	8	E3
	DTTI1X_1	generator outputs RTO10 to RTO15 of Multi-function timer 1.	55	-	-	J9
	FRCK1_0	16-bit free-run timer ch.1 external clock	96	81	66	A8
	FRCK1_1	input pin	50	45	35	K8
	IC10_0		95	80	65	В8
	IC10_1		54	-	-	H8
	IC11_0		94	79	64	C8
	IC11_1	16-bit input capture ch.1 input pin of	53	-	-	G7
	IC12_0	Multi-function timer 1. ICxx describes channel number.	93	78	63	A9
	IC12_1		52	-	-	H7
NALILLI ELLO ALIO A	IC13_0		92	77	62	B9
Multi- function Timer 1	IC13_1		51	-	-	H6
	RTO10_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1.	2	2	2	C1
	RTO10_1 (PPG10_1)	This pin operates as PPG10 when it is used in PPG1 output modes.	32	27	-	L2
	RTO11_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1.	3	3	3	C2
	RTO11_1 (PPG10_1)	This pin operates as PPG10 when it is used in PPG1 output modes.	33	28	-	J3
	RTO12_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1.	4	4	4	D1
	RTO12_1 (PPG12_1)	This pin operates as PPG12 when it is used in PPG1 output modes.	34	29	-	J5
	RTO13_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1.	5	5	5	D2
	RTO13_1 (PPG12_1)	This pin operates as PPG12 when it is used in PPG1 output modes.	35	30	-	H5
	RTO14_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1.	6	6	6	D3
	RTO14_1 (PPG14_1)	This pin operates as PPG14 when it is used in PPG1 output modes.	36	31	21	K3
	RTO15_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1.	7	7	7	E2
	RTO15_1 (PPG14_1)	This pin operates as PPG14 when it is used in PPG1 output modes.	37	32	22	J4

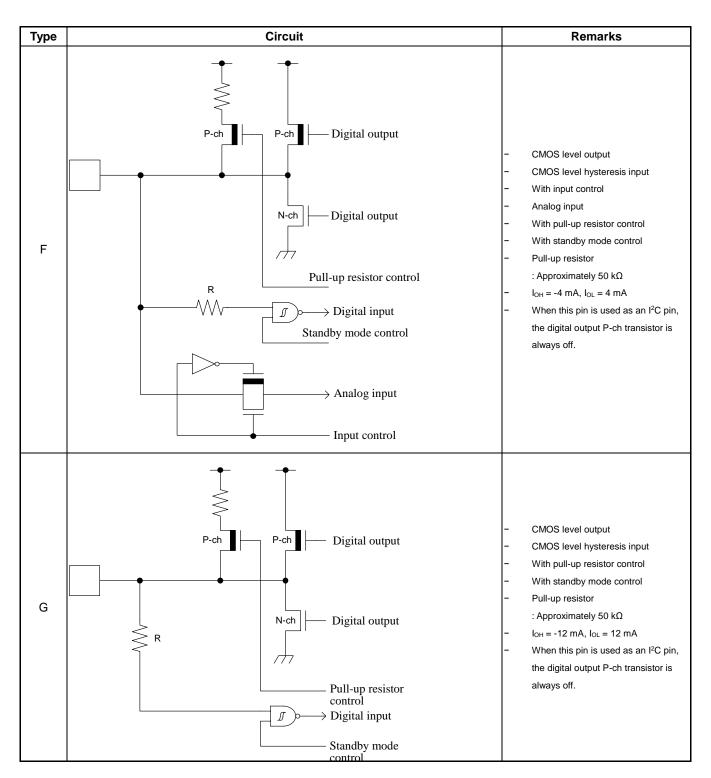


			Pin No				
Pin Function	Pin Name	Function Description	LQFP 120	LQFP 100	LQFP 80	FBGA 121	
	AIN1_0		10	-	-	F5	
	AIN1_1	QPRC ch.1 AIN input pin	89	74	-	B11	
Our destructions	AIN1_2	7 ' '		43	33	J7	
Quadrature	BIN1_0		11	-	-	F6	
Position/	BIN1_1	QPRC ch.1 BIN input pin	88	73	-	C11	
Revolution Counter 1	BIN1_2		49	44	34	J8	
Counter	ZIN1_0		12	-	-	G5	
	ZIN1_1	QPRC ch.1 ZIN input pin	87	72	-	C10	
	ZIN1_2		50	45	35	K8	
	AIN2_0		33	28	-	J3	
	AIN2_1	QPRC ch.2 AIN input pin	119	99	79	A2	
	AIN2_2	·	69	59	48	F9	
Quadrature	BIN2_0		34	29	-	J5	
Position/	BIN2_1	QPRC ch.2 BIN input pin	118	98	78	A3	
Revolution Counter 2	BIN2_2		68	58	47	F10	
Counter 2	ZIN2_0		35	30	-	H5	
	ZIN2_1	QPRC ch.2 ZIN input pin	115	95	75	B3	
	ZIN2_2	r i i	67	57	46	G8	
	RTCCO_0		115	95	75	В3	
	RTCCO_1	0.5 seconds pulse output pin of Real-time	64	54	43	H9	
Real-time	RTCCO_2	clock	23	18	13	H1	
clock	SUBOUT_0		115	95	75	B3	
0.00.1	SUBOUT_1	Sub clock output pin	64	54	43	H9	
	SUBOUT_2		23	18	13	H1	
	WKUP0	Deep standby mode return signal input pin 0	116	96	76	B2	
Low-Power Consumption	WKUP1	Deep standby mode return signal input pin	14	9	9	E1	
Mode	WKUP2	Deep standby mode return signal input pin 2	50	45	35	K8	
WKUP3		Deep standby mode return signal input pin 3	69	59	48	F9	
DAC	DA0	D/A converter ch.0 analog output pin	36	31	21	K3	
2,10	DA1	D/A converter ch.1 analog output pin	37	32	22	J4	
	VREGCTL	On-board regulator control pin	41	36	26	K5	
VBAT	VWAKEUP	The return signal input pin from a hibernation state	42	37	27	K6	
	S_CLK_0	SD memory card interface SD memory card clock output pin	92	77	62	В9	
	S_CMD_0	SD memory card interface SD memory card command output	93	78	63	A9	
	S_DATA1_0		94	79	64	C8	
SD I/F		SD memory card interface	95	80	65	B8	
05 1/1		SD memory card data bus	96	81	66	A8	
	S_DATA2_0		97	82	67	D7	
	S_CD_0	SD memory card interface SD memory card detection pin	113	93	73	B4	
	S_WP_0	SD memory card interface SD memory card write protection	114	94	74	C3	



Туре	Circuit	Remarks
С	N-ch Digital input  Digital output	<ul><li>Open drain output</li><li>CMOS level hysteresis input</li></ul>
Е	P-ch P-ch Digital output  N-ch Digital output  Pull-up resistor control  Digital input  Standby mode control	<ul> <li>CMOS level output</li> <li>CMOS level hysteresis input</li> <li>With pull-up resistor control</li> <li>With standby mode control</li> <li>Pull-up resistor         <ul> <li>Approximately 50 kΩ</li> </ul> </li> <li>I<sub>OH</sub> = -4 mA, I<sub>OL</sub> = 4 mA</li> <li>When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>







# Table for Package Thermal Resistance and Maximum Permissible Power

Doolsono	Printed Circuit Board	Thermal Resistance	Maximum Permissible Power (mW)			
Package	Frinted Circuit Board	θja (°C/W)	T <sub>A</sub> =+85°C	T <sub>A</sub> =+105°C		
LQH080	Single-layered both sides	82	488	244		
(0.5mm pitch)	4 layers	56	714	357		
LQI100	Single-layered both sides	59	678	339		
(0.5mm pitch)	4 layers	39	1026	513		
LQM120	Single-layered both sides	71	563	282		
(0.5mm pitch)	4 layers	50	800	400		
FDI121	Single-layered both sides	63	635	317		
(0.5mm pitch)	4 layers	37	1081	540		

#### **WARNING:**

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All
of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.

Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device

failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.



#### Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

 $Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$ 

 $\begin{array}{lll} \text{I}_{\text{OL}} : & \text{L level output current} \\ \text{I}_{\text{OH}} : & \text{H level output current} \\ \text{V}_{\text{OL}} : & \text{L level output voltage} \\ \text{V}_{\text{OH}} : & \text{H level output voltage} \\ \end{array}$ 

 $I_{\text{CC}}$  is a current consumed in device. It can be analyzed as follows.

 $I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$ 

Icc(INT): Current consumed in internal logic and memory, etc. through regulator

ΣI<sub>CC</sub>(IO): Sum of current (I/O switching current) consumed in output pin

For Icc (INT), it can be anticipated by (1) Current Rating in 3. DC Characteristics (This rating value does not include Icc (IO) for a value at pin fixed).

For Icc (IO), it depends on system used by customers.

The calculation formula is shown below.

 $I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$ 

Cint: Pin internal load capacitance

C<sub>EXT</sub>: External load capacitance of output pin

f<sub>SW</sub>: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
		4 mA type	1.93 pF
Pin internal load capacitance	CINT	8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate Icc (Max) as follows when the power dissipation can be evaluated by yourself.

- 1. Measure current value I<sub>CC</sub> (Typ) at normal temperature (+25°C).
- 2. Add maximum leak current value Icc (leak\_max) at operating on a value in (1).

$$Icc(Max) = Icc(Typ) + Icc(Ieak_max)$$

Parameter	Symbol	Conditions	Current Value
		$T_J = +125^{\circ}C$	16.8 mA
Maximum leak current at operating	lcc(leak_max)	$T_J = +105^{\circ}C$	8.6 mA
		T <sub>J</sub> = +85°C	5.8 mA



#### 13.4 AC Characteristics

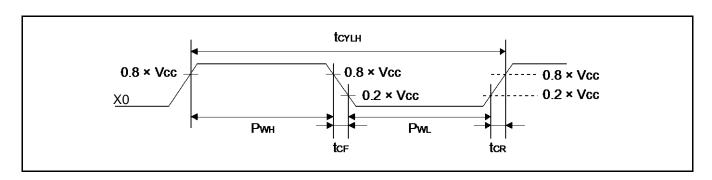
### 13.4.1 Main Clock Input Characteristics

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

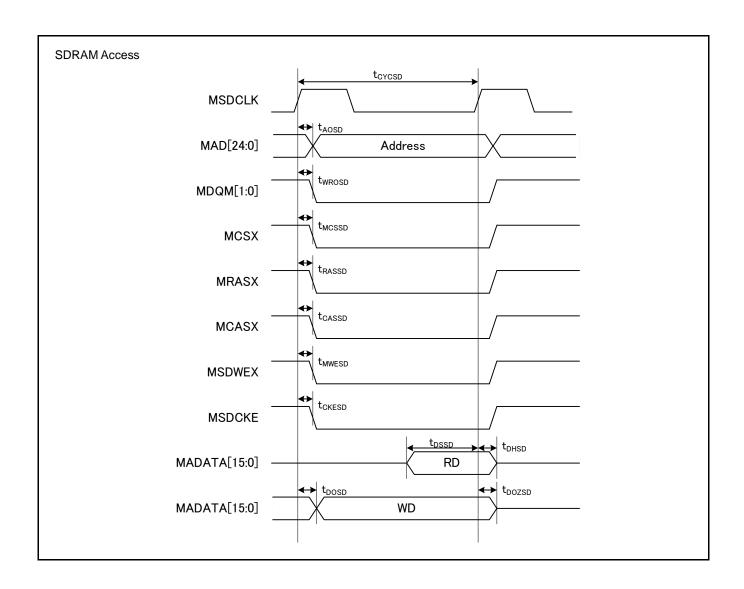
Parameter	Symbol	Pin Name	Conditions	Va	lue	Unit	Remarks	
Parameter	Symbol	FIII Name	Conditions	Min	Max	Offic	Remarks	
			V <sub>CC</sub> ≥ 4.5 V	4	48	MHz	When crystal oscillator is	
Input frequency	fсн		Vcc < 4.5 V	4	20	IVIITZ	connected	
Imput mequeincy	ICH		V <sub>CC</sub> ≥ 4.5 V	4	48	MHz	When using external clock	
			V <sub>CC</sub> < 4.5 V	4	20	IVII IZ	When using external clock	
Input clock cycle	tcylh	X0,	V <sub>CC</sub> ≥ 4.5 V	20.83	250	ns	When using external clock	
iliput ciock cycle	ICYLH	X1	V <sub>CC</sub> < 4.5 V	50	250	113	When using external clock	
Input clock pulse width	-		Pwn/tcyln, Pwl/tcyln	45	55	%	When using external clock	
Input clock rising time and falling time	t <sub>CF</sub> , t <sub>CR</sub>		-	-	5	ns	When using external clock	
	fcc	-	-	-	160	MHz	Base clock (HCLK/FCLK)	
Internal operating	f <sub>CP0</sub>	-	-	-	80	MHz	APB0 bus clock*2	
clock*1 frequency	f <sub>CP1</sub>	-	-	-	160	MHz	APB1 bus clock*2	
	f <sub>CP2</sub>	-	-	-	80	MHz	APB2 bus clock*2	
	tcycc	-	-	6.25	-	ns	Base clock (HCLK/FCLK)	
Internal operating	t <sub>CYCP0</sub>	-	-	12.5	-	ns	APB0 bus clock*2	
clock*1 cycle time	t <sub>CYCP1</sub>	-	-	6.25	-	ns	APB1 bus clock*2	
	tcycp2	-	-	12.5	-	ns	APB2 bus clock*2	

<sup>\*1:</sup> For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main part (002-04856).

<sup>\*2:</sup> For about each APB bus which each peripheral is connected to, see 1. S6E2H Series Block Diagram" in this data sheet.







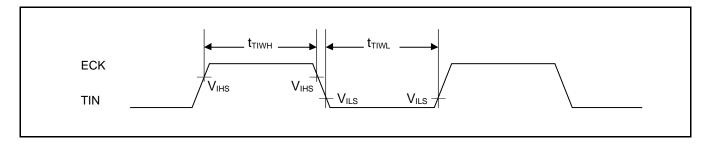


#### 13.4.10 Base Timer Input Timing

# **Timer Input Timing**

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

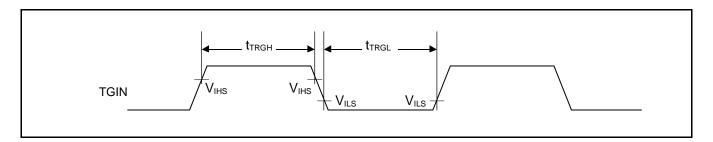
Parameter	Symbol Pin Name		Conditions	Value		Unit	Remarks
Farailletei	Symbol	FIII Name	Conditions	Min	Max	Offic	Remarks
Input pulse width	tтıwн, tтıwL	TIOAn/TIOBn (when using as ECK, TIN)	-	2tcycp	-	ns	



# **Trigger Input Timing**

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
Parameter	Symbol	FIII Name	Conditions Min N		Max	Onit	Remarks
Input pulse width	tтrgн, tтrgl	TIOAn/TIOBn (when using as TGIN)	-	2t <sub>CYCP</sub>	-	ns	



## Note:

t<sub>CYCP</sub> indicates the APB bus clock cycle time.
 About the APB bus number which the Base Timer is connected to, see 1. S6E2H Series Block Diagram in this data sheet.



### When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Conditions	V <sub>cc</sub> <	4.5 V	V <sub>CC</sub> ≥	Unit	
i arameter	Symbol	Conditions	Min	Max	Min	Max	Oille
SCS↓→SCK↓setup time	tcssı	Internal shift	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	tcsнı	clock	(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	tcsdi	operation	(*3)-50 +5tcycp	(*3)+50 +5tcycp	(*3)-50 +5tcycp	(*3)+50 +5tcycp	ns
SCS↓→SCK↓setup time	tcsse		3tcycp+30	-	3tcycp+30	-	ns
SCK↑→SCS↑ hold time	tcshe	External shift	0	-	0	-	ns
SCS deselect time	t <sub>CSDE</sub>	clock	3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCS↓→SUT delay time	tose	operation	-	40	-	40	ns
SCS↑→SUT delay time	t <sub>DEE</sub>		0	-	0	-	ns

(\*1): CSSU bit valuexserial chip select timing operating clock cycle [ns]

(\*2): CSHD bit valuexserial chip select timing operating clock cycle [ns]

(\*3): CSDS bit valuexserial chip select timing operating clock cycle [ns]

### Notes:

- tcycp indicates the APB bus clock cycle time.
   About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).
- When the external load capacitance  $C_L = 30 pF$ .



### When Using High-speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
raiametei	Symbol	Conditions	Min	Max	Min	Max	Unit
SCS↑→SCK↓setup time	t <sub>CSSI</sub>		(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	tcsнı	Internal shift	(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	tcsdi	clock operation	(*3)-20 +5tcycp	(*3)+20 +5tcycp	(*3)-20 +5tcycp	(*3)+20 +5tcycp	ns
SCS↑→SCK↓setup time	tcsse		3tcycp+15	-	3tcycp+15	-	ns
SCK↑→SCS↓ hold time	tcshe		0	-	0	-	ns
SCS deselect time	tcsde	External shift clock operation	3tcycp+15	-	3tcycp+15	-	ns
SCS↑→SOT delay time	t <sub>DSE</sub>	ciock operation.	-	25	-	25	ns
SCS↓→SOT delay time	t <sub>DEE</sub>	]	0	-	0	-	ns

(\*1): CSSU bit valuexserial chip select timing operating clock cycle [ns]

(\*2): CSHD bit valuexserial chip select timing operating clock cycle [ns]

(\*3): CSDS bit valuexserial chip select timing operating clock cycle [ns]

#### Notes:

- t<sub>CYCP</sub> indicates the APB bus clock cycle time.
   About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).
- When the external load capacitance  $C_L = 30 \text{ pF}$ .



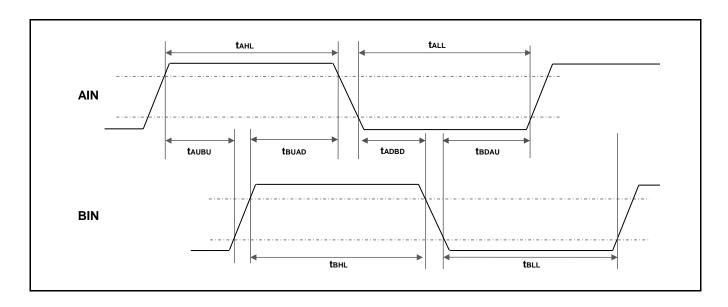
#### 13.4.13 Quadrature Position/Revolution Counter Timing

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Conditions	Va	Unit	
Farameter	Symbol	Conditions	Min	Max	Offic
AIN pin H width	t <sub>AHL</sub>	-			
AIN pin L width	tall	-			
BIN pin H width	t <sub>BHL</sub>	-			
BIN pin L width	t <sub>BLL</sub>	-			
BIN rising time from	t <sub>AUBU</sub>	PC_Mode2 or PC_Mode3			
AIN pin H level	7.020				
AIN falling time from	<b>t</b> BUAD	PC_Mode2 or PC_Mode3			
BIN pin H level	-50/15				
BIN falling time from	taded	PC_Mode2 or PC_Mode3			
AIN pin L level	*ADDD	1 0_1110d02 01 1 0_1110d00			
AIN rising time from	<b>t</b> BDAU	PC_Mode2 or PC_Mode3			
BIN pin L level	IDDAO	1 0_1110d02 01 1 0_1110d00			
AIN rising time from	<b>t</b> BUAU	PC_Mode2 or PC_Mode3	2tcycp*	_	ns
BIN pin H level	BOAG	1 0_INICOC 01 1 0_INICOC	2.010		1.0
BIN falling time from	t <sub>AUBD</sub>	PC_Mode2 or PC_Mode3			
AIN pin H level	TAUBD	1 O_INIOGCZ OI 1 O_INIOGCO			
AIN falling time from	<b>t</b> BDAD	PC Mode2 or PC Mode3			
BIN pin L level	IBDAD	1 C_IVIOGEZ OF 1 C_IVIOGES			
BIN rising time from	t <sub>ADBU</sub>	PC_Mode2 or PC_Mode3			
AIN pin L level	LADBO	1 C_IVIOGEZ OF 1 C_IVIOGES			
ZIN pin H width	tzhl	QCR:CGSC="0"			
ZIN pin L width	tzll	QCR:CGSC="0"			
AIN/BIN rising and falling time from	4	OCB:CCSC_"1"			
determined ZIN level	t <sub>ZABE</sub>	QCR:CGSC="1"			
Determined ZIN level from AIN/BIN rising and falling time	t <sub>ABEZ</sub>	QCR:CGSC="1"			

<sup>\*:</sup> tcycp indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode.

About the APB bus number which Quadrature Position/Revolution Counter is connected to, see 1. S6E2H Series Block Diagram in this data sheet.





### **High-Speed Mode**

■ Clock CLK (All values are referred to V<sub>IH</sub> and V<sub>IL</sub>)

 $(V_{CC} = 2.7V \text{ to } 3.6V, V_{SS} = 0V)$ 

Parameter	Symbol	Pin Name	Conditions	Value		Remarks	
Parameter	Syllibol	riii Naiile	anie Conditions		Max	Remarks	
Clock frequency Data Transfer Mode	f <sub>PP</sub>	S_CLK		0	40	MHz	
Clock low time	tw∟	S_CLK	C <sub>CARD</sub> ≤ 10 pF	7	-	ns	
Clock high time	twн	S_CLK	(1 card)	7	-	ns	
Clock rising time	tTLH	S_CLK		1	3	ns	
Clock falling time	t <sub>THL</sub>	S_CLK		-	3	ns	

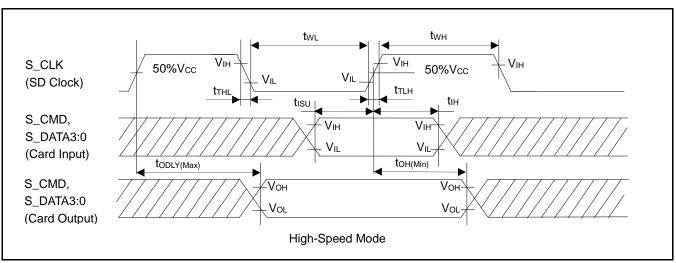
■ Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks	
Parameter	Syllibol	Fili Naille	Conditions	Min			
Input set-up time	tısu	S_CMD, S_DATA3:0	C <sub>CARD</sub> ≤ 10 pF	8	-	ns	
Input hold time	tıн	S_CMD, S_DATA3:0	(1 card)	2	-	ns	

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Din Name	Conditions	Value		Remarks	
Parameter	Symbol Pin Name		Conditions	Min	Max		
Output Delay time during Data Transfer Mode	todly	S_CMD, S_DATA3:0	C <sub>L</sub> ≤ 40 pF (1 card)	-	22	ns	
Output Hold time	tон	S_CMD, S_DATA3:0	C <sub>L</sub> ≥ 15 pF (1 card)	2.5	-	ns	
Total System capacitance for each line*	CL	-	1 card	-	40	pF	

<sup>\*:</sup> In order to satisfy severe timing, host shall drive only one card.



#### Notes:

- The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host
- For more information about clock frequency (fPP), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).



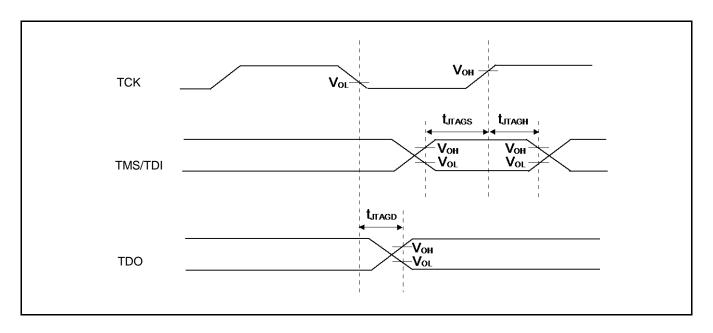
### 13.4.17 JTAG Timing

 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$ 

Parameter	Symbol	Pin Name	Conditions	Va	Value		Remarks
Parameter	Syllibol	Pili Naille	Conditions	Min	Max	Unit	Remarks
TMS, TDI setup time	t <sub>JTAGS</sub>	TCK,	V <sub>CC</sub> ≥ 4.5 V	15	-	ns	
		TMS, TDI	$V_{CC}$ < 4.5 V				
TMS, TDI hold time	<b>t</b> JTAGH	TCK,	V <sub>CC</sub> ≥ 4.5 V	15	-	ns	
	UTAGH	TMS, TDI	Vcc < 4.5 V				
TDO delay time	t	TCK,	V <sub>CC</sub> ≥ 4.5 V	-	25	nc	
TDO delay lime	tjtagd	TDO	Vcc < 4.5 V	-	45	ns	

### Note:

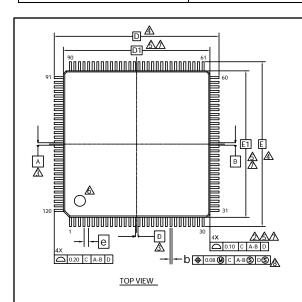
When the external load capacitance C<sub>L</sub>= 30 pF.

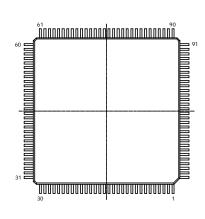




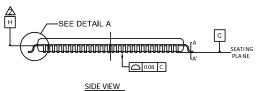
### 15. Package Dimensions

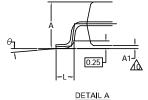
Package Type	Package Code			
LQFP 120	LQM120			





BOTTOM VIEW







SYMBOL	DIV	DIMENSIONS				
STIVIBOL	MIN.	NOM.	MAX.			
Α	_	_	1.70			
A1	0.05	_	0.15			
b	0.17	0.22	0.27			
С	0.115	_	0.195			
D	18	8.00 BS0				
D1	10	6.00 BS0				
е	0	.50 BSC				
E	18.00 BSC					
E1	16.00 BSC					
L	0.45	0.60	0.75			
θ	0°	_	8°			

#### <u>NOTES</u>

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- ⚠ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- ⚠ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- A TO BE DETERMINED AT SEATING PLANE C.
- ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.

  DIMENSIONS D1 AND E1 INCLUDE MOLD PROTRUSION.

  ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.

  DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATI IM PI ANE H
- ⚠ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- 9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 11. JEDEC SPECIFICATION NO. REF: N/A.

PACKAGE OUTLINE, 120 LEAD LQFP 18.0X18.0X1.7 MM LQM120 REV\*\*

002-16172 \*\*



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