Infineon Technologies - S6E2HG4F0AGV20000 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2hg4f0agv20000

6. Pin Description

6.1 List of Pin Numbers

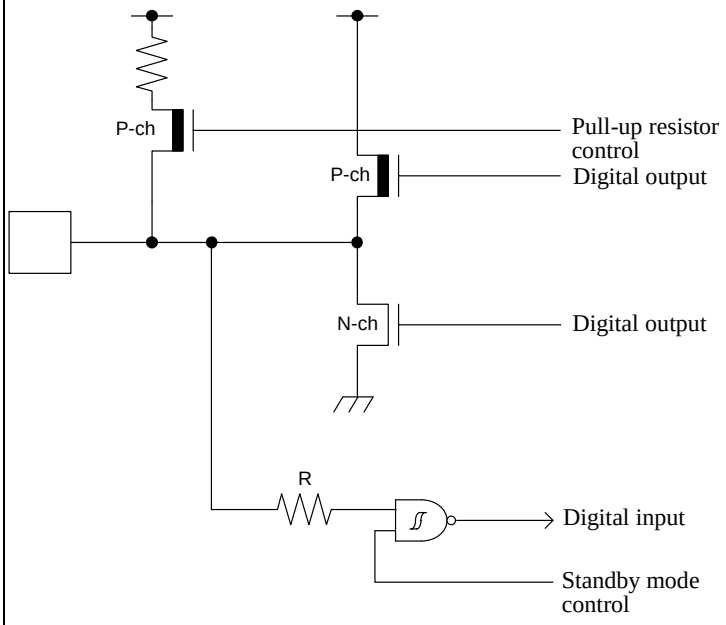
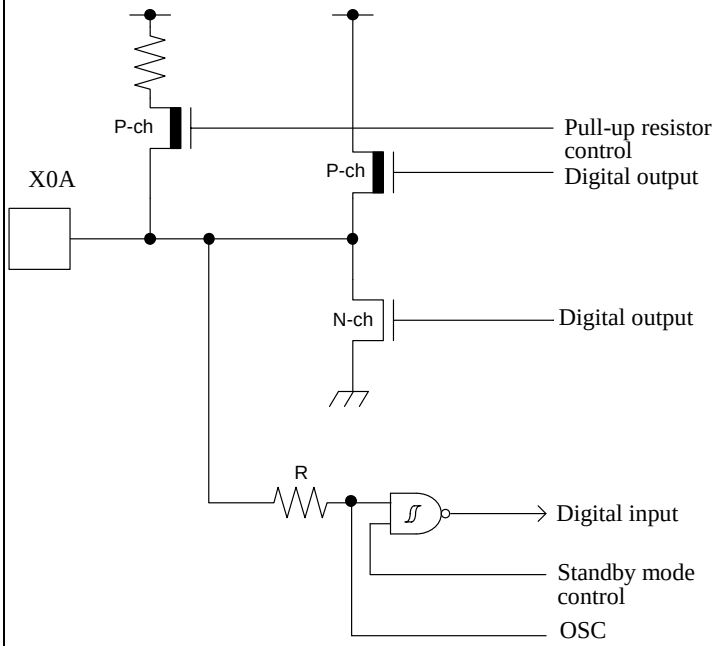
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
1	1	1	B1	VCC	-	-
2	2	2	C1	P50 CTS4_0 AIN0_2 RTO10_0 (PPG10_0) INT00_0 MADATA00_0	E	K
3	3	3	C2	P51 RTS4_0 BIN0_2 RTO11_0 (PPG10_0) INT01_0 MADATA01_0	E	K
4	4	4	D1	P52 SCK4_0 (SCL4_0) ZIN0_2 RTO12_0 (PPG12_0) MADATA02_0	E	I
5	5	5	D2	P53 TIOA1_2 SOT4_0 (SDA4_0) RTO13_0 (PPG12_0) MADATA03_0	E	I
6	6	6	D3	P54 TIOB1_2 SIN4_0 RTO14_0 (PPG14_0) INT02_0 MADATA04_0	E	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
14	9	9	E1	P30	E	Q
				TIOB0_1		
				RTS4_2		
				INT15_2		
				WKUP1		
-			-	MADATA07_0		
14	-	-	E1	MADATA12_0		
	9	9		RTO25_1		
15	10	10	F4	P31	I	K
				TIOB1_1		
				SIN3_1		
				INT09_2		
-			-	MADATA08_0		
15	-	-	F4	MADATA13_0		
	10	10		DTTI2X_1		
16	11	11	F3	P32	N	K
				TIOB2_1		
				SOT3_1 (SDA3_1)		
				INT10_1		
-			-	MADATA09_0		
16	-	-	F3	MADATA14_0		
17	12	12	F2	P33	N	K
				ADTG_6		
				TIOB3_1		
				SCK3_1 (SCL3_1)		
				INT04_0		
-			-	MADATA10_0		
17	-	-	F2	MADATA15_0		
18	13	-	F1	P34	E	I
				TIOB4_1		
				FRCK0_0		
				TX0_1		
-			-	MADATA11_0		
18	-	-	F1	MNALE_0		
19	14	-	G1	P35	E	K
				TIOB5_1		
				IC03_0		
				INT08_1		
				RX0_1		
-			-	MADATA12_0		
19	-	-	G1	MNCLE_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
104	89	70	C5	P02 TDI MCSX6_0	E	H
105	90	71	B5	P01 TCK SWCLK	E	G
106	91	72	A5	P00 TRSTX MCSX7_0	E	H
107	92	-	A6	VSS	-	-
108	-	-	E6	P68 TIOB7_2 SCK3_0 (SCL3_0) INT00_2	E	K
109	-	-	E5	P67 TIOA7_2 SOT3_0 (SDA3_0)	E	I
110	-	-	D5	P66 ADTG_8 SIN3_0 INT11_2	E	K
111	-	-	D4	P65 TIOB7_0 SCK5_1 (SCL5_1)	E	I
112	-	-	C4	P64 TIOA7_0 SOT5_1 (SDA5_1) INT10_2	E	K
113	93	73	B4	P63 CROUT_1	E	K
	-	-		SIN5_1		
	93	73		INT03_0 S_CD_0 MWEX_0 IC23_0 RX0_2		

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Multi-function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	53	-	-	G7
	SIN2_1		85	-	-	B10
	SIN2_2		68	58	47	F10
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I2C (operation mode 4).	54	-	-	H8
	SOT2_1 (SDA2_1)		84	-	-	C9
	SOT2_2 (SDA2_2)		69	59	48	F9
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I2C (operation mode 4).	55	-	-	J9
	SCK2_1 (SCL2_1)		83	-	-	D8
	SCK2_2 (SCL2_2)		74	64	53	F8
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	110	-	-	D5
	SIN3_1		15	10	10	F4
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I2C (operation mode 4).	109	-	-	E5
	SOT3_1 (SDA3_1)		16	11	11	F3
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I2C (operation mode 4).	108	-	-	E6
	SCK3_1 (SCL3_1)		17	12	12	F2
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	6	6	6	D3
	SIN4_1		75	65	54	E11
	SIN4_2		10	-	-	F5
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I2C (operation mode 4).	5	5	5	D2
	SOT4_1 (SDA4_1)		76	66	55	E10
	SOT4_2 (SDA4_2)		11	-	-	F6
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an I2C (operation mode 4).	4	4	4	D1
	SCK4_1 (SCL4_1)		77	67	56	E9
	SCK4_2 (SCL4_2)		12	-	-	G5
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	2	2	2	C1
	CTS4_1		78	68	-	E8
	CTS4_2		13	-	-	G6
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	3	3	3	C2
	RTS4_1		79	69	-	D10
	RTS4_2		14	9	9	E1

Type	Circuit	Remarks
O		– CMOS level output – CMOS level hysteresis input – 5 V tolerant – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual
P		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual

Lead-Free Packaging

CAUTION: When ball grid array (FBGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

Table 12-4 Typical and Maximum Current Consumption in Normal Operation(other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 wait-cycle Mode and Read Access 0 wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (main oscillation)	*5*6	4 MHz	4.0	24	mA	*3 When all peripheral clocks are ON
						3.2	24	mA	*3 When all peripheral clocks are OFF
			Normal operation (built-in high-speed CR)	*5	4 MHz	3.2	24	mA	*3 When all peripheral clocks are ON
						2.7	23	mA	*3 When all peripheral clocks are OFF
			Normal operation (sub oscillation)	*5	32 kHz	0.34	21	mA	*3 When all peripheral clocks are ON
						0.30	21	mA	*3 When all peripheral clocks are OFF
			Normal operation (built-in low-speed CR)	*5	100 kHz	0.36	21	mA	*3 When all peripheral clocks are ON
						0.33	21	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, VC_C=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0"

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 000)

*6: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-5 Typical and Maximum Current Consumption in Sleep Operation(PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation *6 (PLL)	160 MHz	35	55	mA	*3 When all peripheral clocks are ON
				144 MHz	32	52		
				120 MHz	27	47		
				100 MHz	23	43		
				80 MHz	18	39		
				60 MHz	14	34		
				40 MHz	9.9	30		
				20 MHz	5.5	26		
				8 MHz	3.1	23		
				4 MHz	2.3	23		
				160 MHz	14	35	mA	*3 When all peripheral clocks are OFF
				144 MHz	13	33		
				120 MHz	11	31		
				100 MHz	9.5	30		
				80 MHz	7.8	28		
				60 MHz	6.3	27		
				40 MHz	4.6	25		
				20 MHz	2.9	23		
				8 MHz	2.2	23		
				4 MHz	2.0	22		

Table 12-6 Typical and Maximum Current Consumption in Sleep Operation(PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*5	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation *6 (PLL)	72 MHz	23	43	mA	*3 When all peripheral clocks are ON
				60 MHz	19	39		
				48 MHz	16	36		
				36 MHz	12	32		
				24 MHz	8.5	29		
				12 MHz	5.1	25		
				8 MHz	3.9	24		
				4 MHz	2.7	23		
				72 MHz	8.8	29	mA	*3 When all peripheral clocks are OFF
				60 MHz	7.6	28		
				48 MHz	6.3	27		
				36 MHz	5.1	25		
				24 MHz	3.9	24		
				12 MHz	2.7	23		
				8 MHz	2.3	23		
				4 MHz	1.9	22		

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0"

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*6: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-8 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.21	0.94	mA	*3, *4 T_A=+25°C
					-	7.6	mA	*3, *4 T_A=+85°C
					-	10	mA	*3, *4 T_A=+105°C
	I_{CCT}		Timer mode *5 (main oscillation)	4 MHz	1.4	2.1	mA	*3, *4 T_A=+25°C
					-	8.8	mA	*3, *4 T_A=+85°C
					-	11	mA	*3, *4 T_A=+105°C
			Timer mode (built-in high-speed CR)	4 MHz	0.49	1.2	mA	*3, *4 T_A=+25°C
					-	7.9	mA	*3, *4 T_A=+85°C
					-	11	mA	*3, *4 T_A=+105°C
			Timer mode (sub oscillation)	32 kHz	0.23	0.96	mA	*3, *4 T_A=+25°C
					-	7.6	mA	*3, *4 T_A=+85°C
					-	10	mA	*3, *4 T_A=+105°C
			Timer mode (built-in low-speed CR)	100 kHz	0.24	0.97	mA	*3, *4 T_A=+25°C
					-	7.6	mA	*3, *4 T_A=+85°C
					-	10	mA	*3, *4 T_A=+105°C
	I_{CCR}		RTC mode (sub oscillation)	32 kHz	0.21	0.94	mA	*3, *4 T_A=+25°C
					-	7.6	mA	*3, *4 T_A=+85°C
					-	10	mA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0"

*4: When LVD is OFF

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-9 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCHD}	VCC	Deep standby Stop mode (When RAM is OFF)	-	24	40	µA	*3, *4 T_A=+25°C
					-	640	µA	*3, *4 T_A=+85°C
					-	813	µA	*3, *4 T_A=+105°C
			Deep standby Stop mode (When RAM is ON)		41	146	µA	*3, *4 T_A=+25°C
					-	1616	µA	*3, *4 T_A=+85°C
					-	2059	µA	*3, *4 T_A=+105°C
	I_{CCRD}		Deep standby RTC mode (When RAM is OFF)	32 kHz	24	40	µA	*3, *4 T_A=+25°C
					-	640	µA	*3, *4 T_A=+85°C
					-	813	µA	*3, *4 T_A=+105°C
			Deep standby RTC mode (When RAM is ON)		41	146	µA	*3, *4 T_A=+25°C
					-	1616	µA	*3, *4 T_A=+85°C
					-	2059	µA	*3, *4 T_A=+105°C
	I_{CCVBAT}	VBAT	RTC stop*7	-	0.015	0.14	µA	*3, *4, *5 T_A=+25°C
					-	4.0	µA	*3, *4, *5 T_A=+85°C
					-	9.4	µA	*3, *4, *5 T_A=+105°C
			RTC operation *6, *7		1.3	2.4	µA	*3, *4 T_A=+25°C
					-	6.2	µA	*3, *4 T_A=+85°C
					-	12	µA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0"

*4: When LVD is OFF

*5: When sub oscillation is OFF

*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

*7: In the case of setting RTC after VCC power on

13.4.9 External Bus Timing

External Bus Clock Output Characteristics

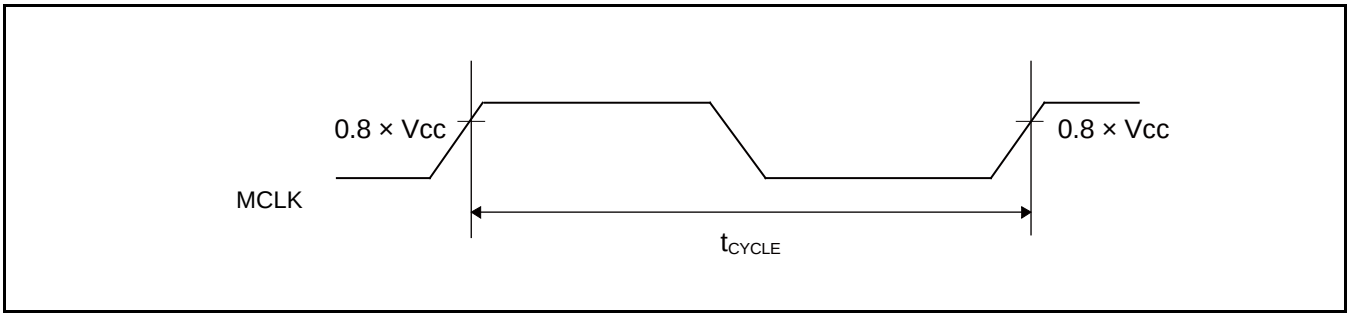
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	$V_{CC} \geq 4.5$ V	-	50*2	MHz
			$V_{CC} < 4.5$ V	-	32*3	MHz

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main part (002-04856).

*2: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 100 MHz.

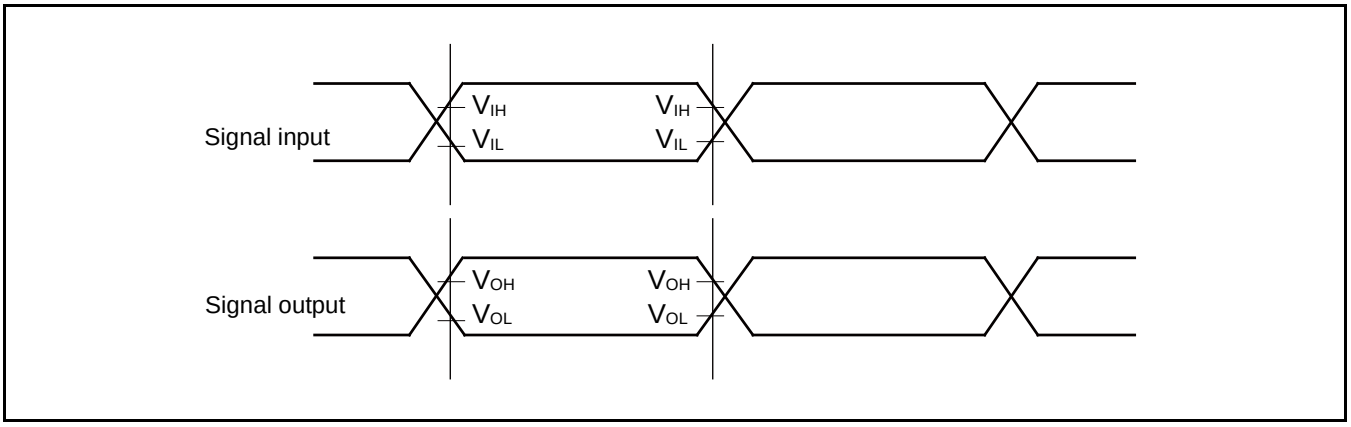
*3: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 64 MHz.



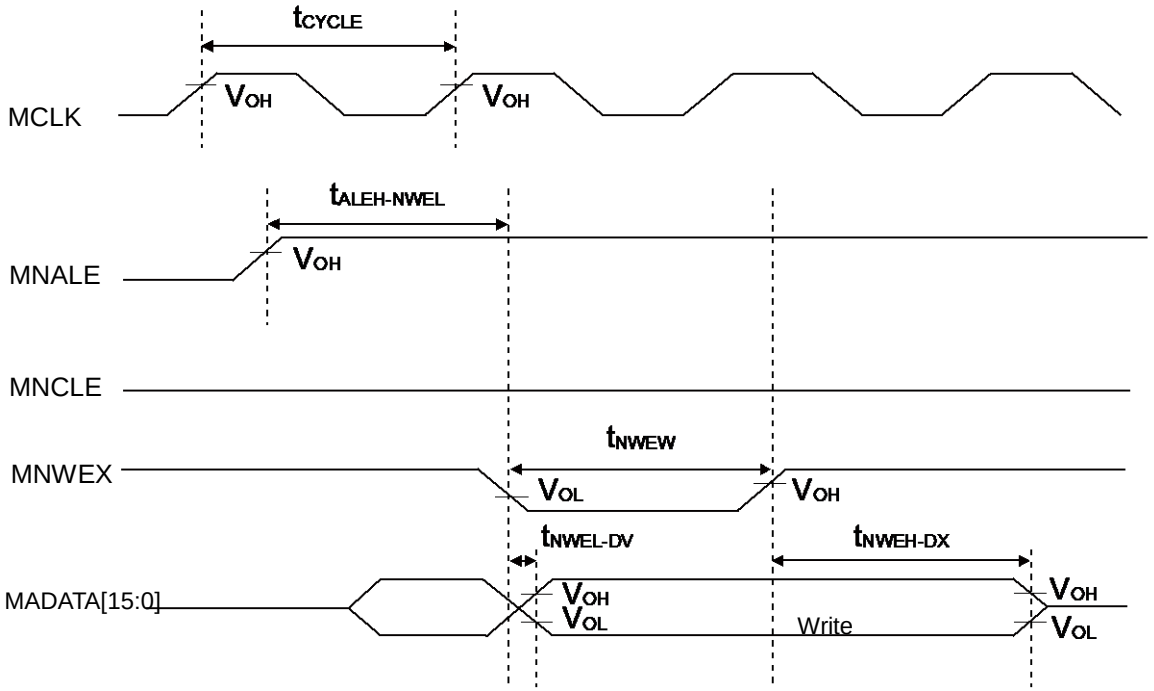
External Bus Signal Input/output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

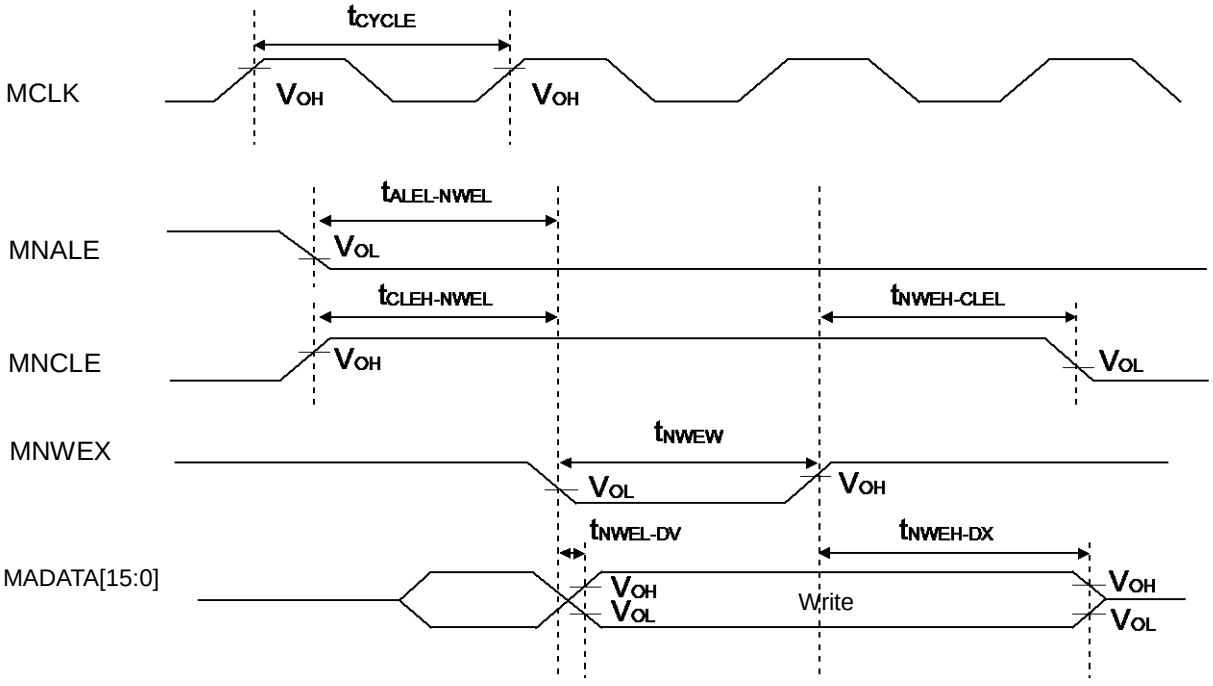
Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	

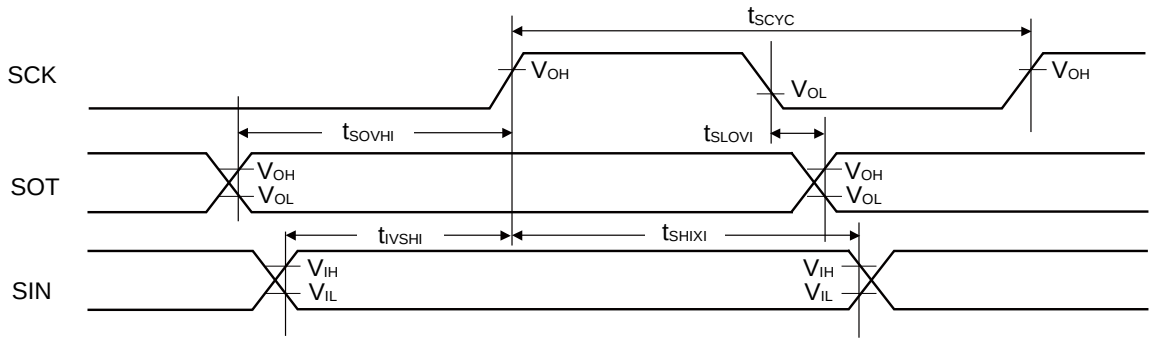


NAND Flash Address Write

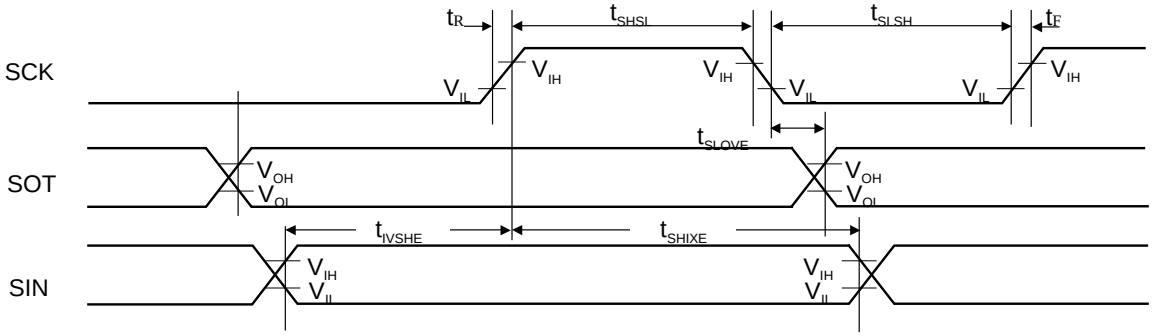


NAND Flash Command Write

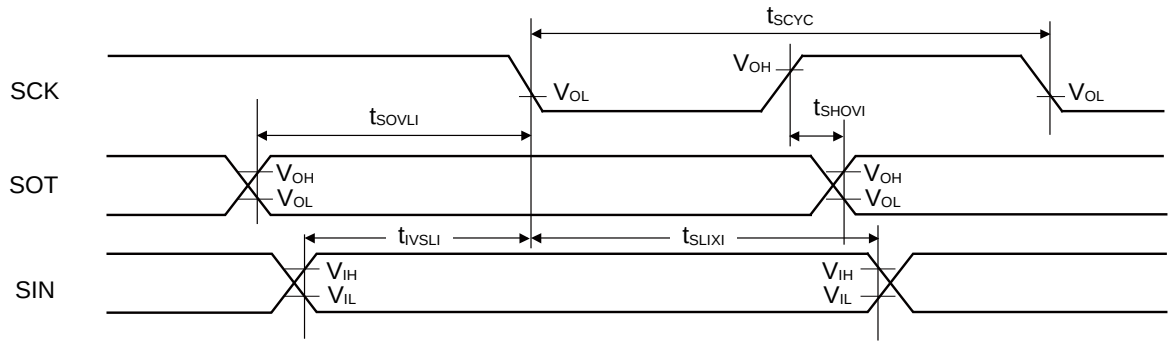




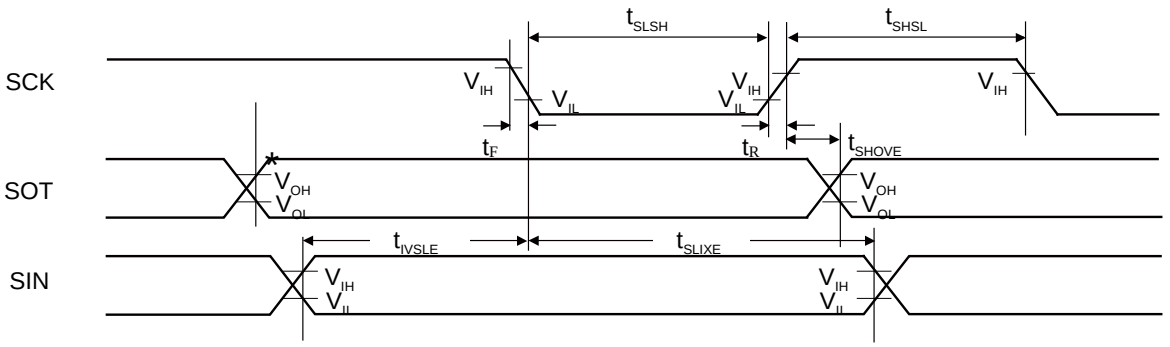
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

High-speed Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Internal shift clock operation	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ →SOT delay time	t_{SLOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK ↑ →SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ →SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK ↑ →SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
- *No chip select: SIN4_1, SOT4_1, SCK4_1*
- *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

When Using High-speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

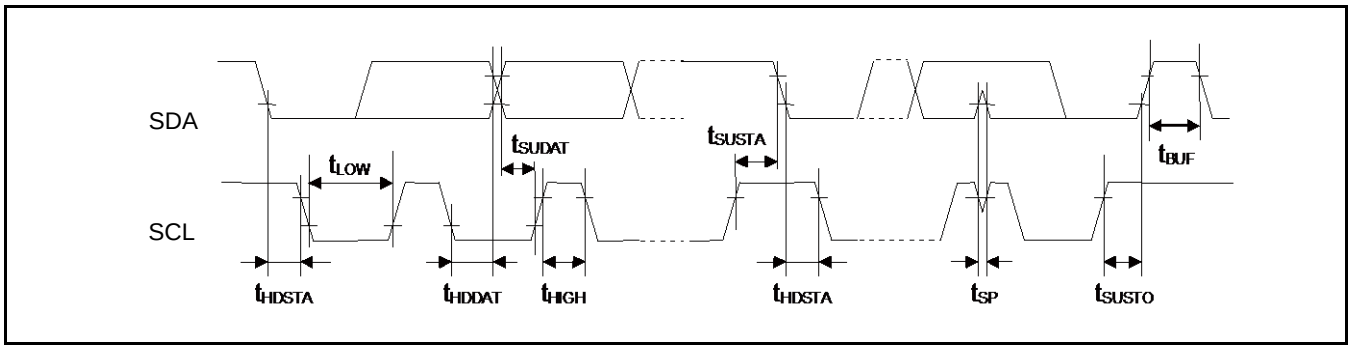
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

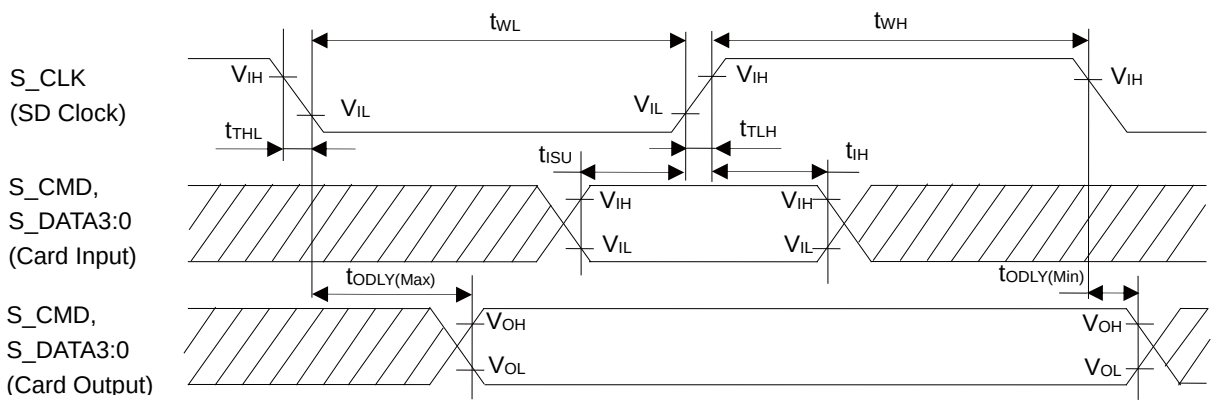
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO



Default-Speed Mode

Note:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*

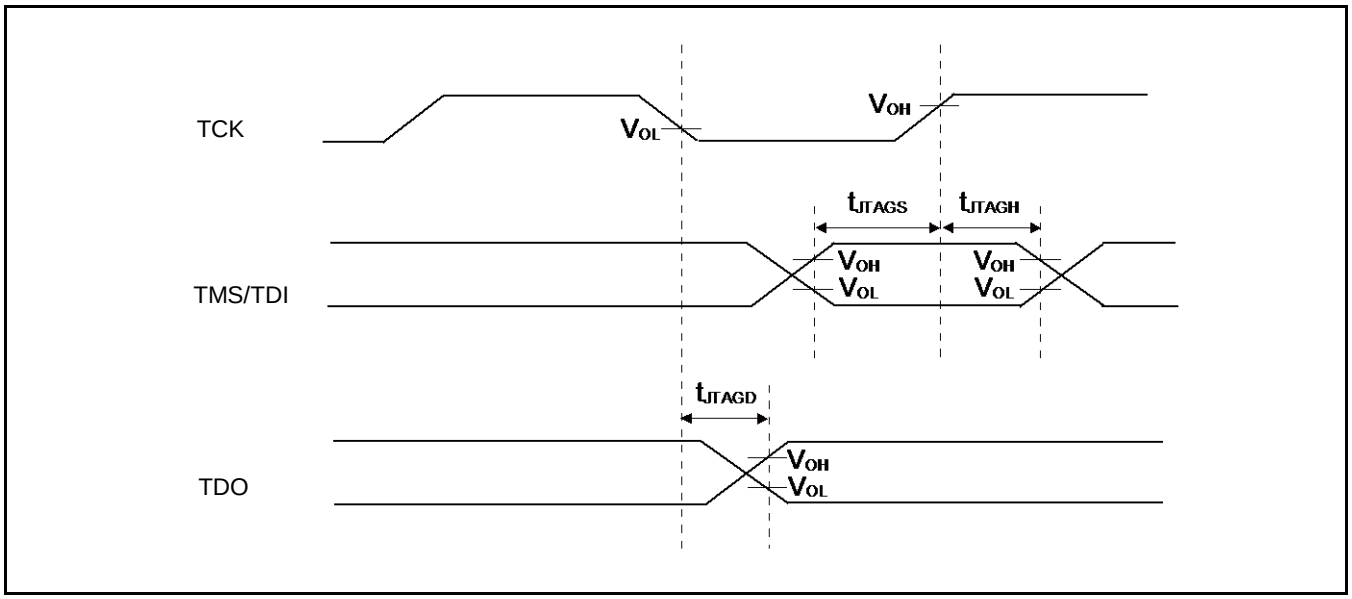
13.4.17 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

Note:

- *When the external load capacitance C_L= 30 pF.*



13.7 Low-Voltage Detection Characteristics

13.7.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

13.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	4480× t_{CYCP}*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.