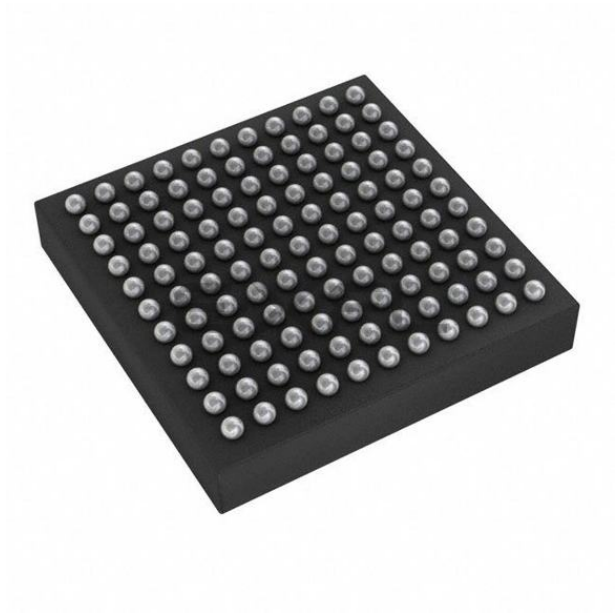

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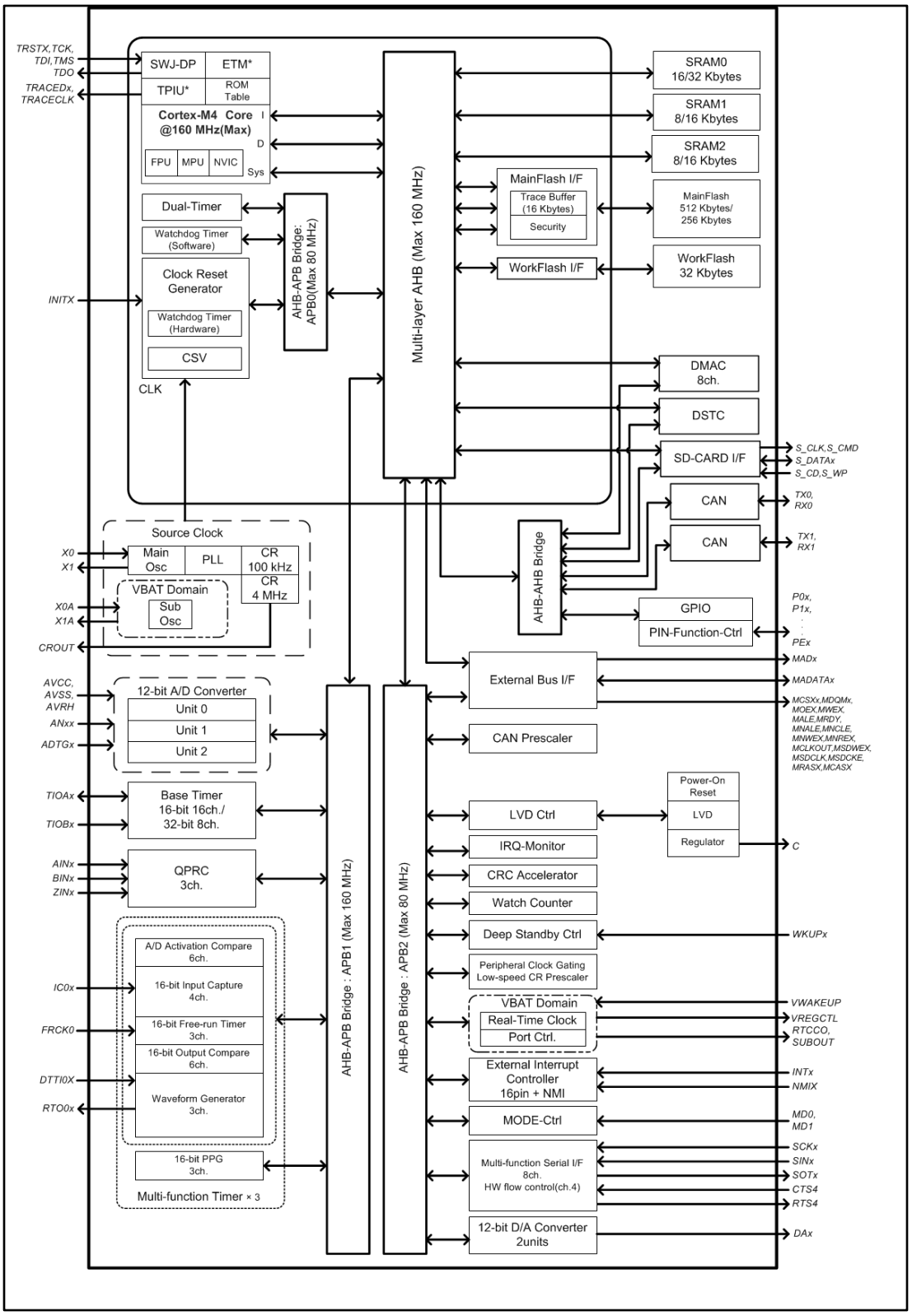
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2hg4g0agb3000a

1. S6E2H Series Block Diagram



4. Detailed Product Features

32-bit ARM Cortex-M4F Core

- Up to 160 MHz Frequency Operation
- FPU built-in
- Support DSP instruction
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

- Flash memory

These series are based on two independent on-chip Flash memories.

  - MainFlash memory
    - Up to 512 Kbytes
    - Built-in Flash Accelerator System with 16 Kbytes trace buffer memory
    - The read access to Flash memory can be achieved without wait-cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
    - Security function for code protection
  - WorkFlash memory
    - 32 Kbytes
    - Read cycle:
    - 6 wait-cycle: the operation frequency more than 120 MHz, and up to 160 MHz
    - 4 wait-cycle: the operation frequency more than 72 MHz, and up to 120 MHz
    - 2 wait-cycle: the operation frequency more than 40 MHz, and up to 72 MHz
    - 0 wait-cycle: the operation frequency up to 40 MHz
    - Security function is shared with code protection

- SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to I-code bus or D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to System bus of Cortex-M4F core.

  - SRAM0: Up to 32 Kbytes
  - SRAM1: Up to 16 Kbytes
  - SRAM2: Up to 16 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND Flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Supports Address/Data multiplex
- Supports external RDY function
- Supports scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key
  - **Note**: It is necessary to prepare the dedicated software library to use the scramble function.

CAN Interface (Max 2 channels)

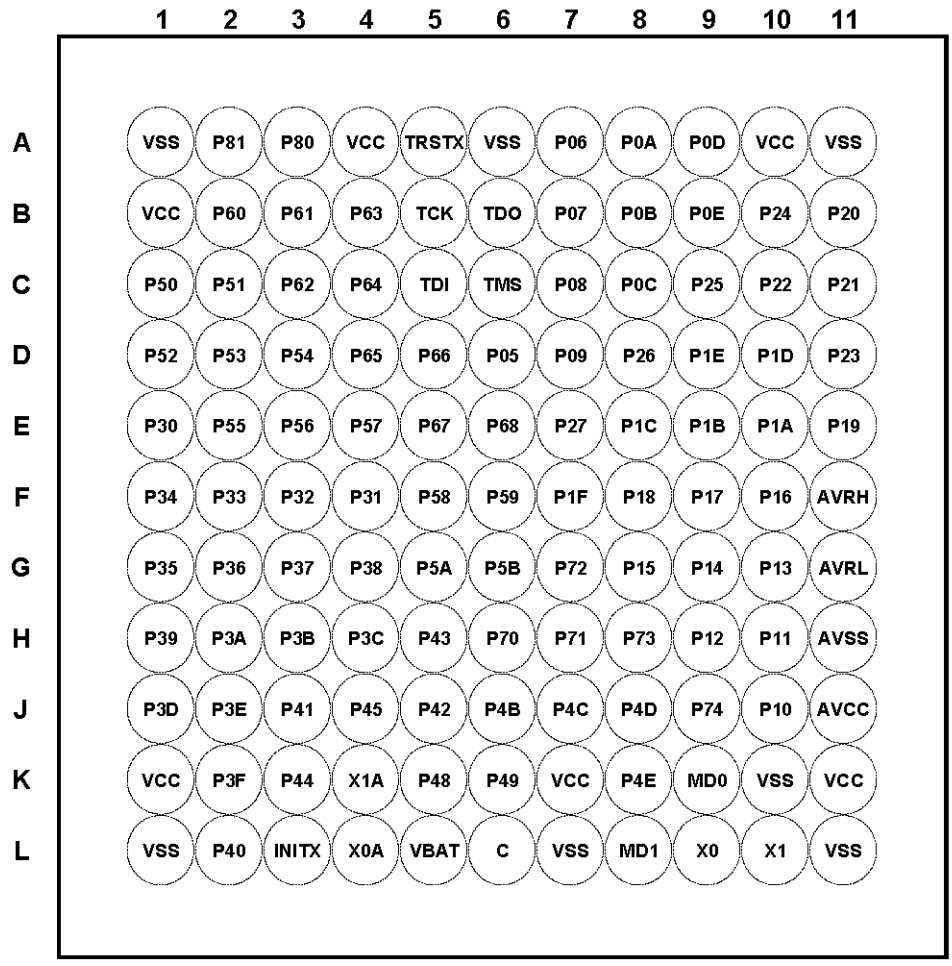
- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32 message buffer

Multi-function Serial Interface (Max 8 channels)

- 64 bytes with FIFO (the FIFO step numbers are variable depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 and ch.7 only)
  - Supports high-speed SPI (ch.4 and ch.6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation (can change to 13 to 16-bit length)
  - LIN break delimiter generation (can change to 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)

FDI121

(TOP VIEW)



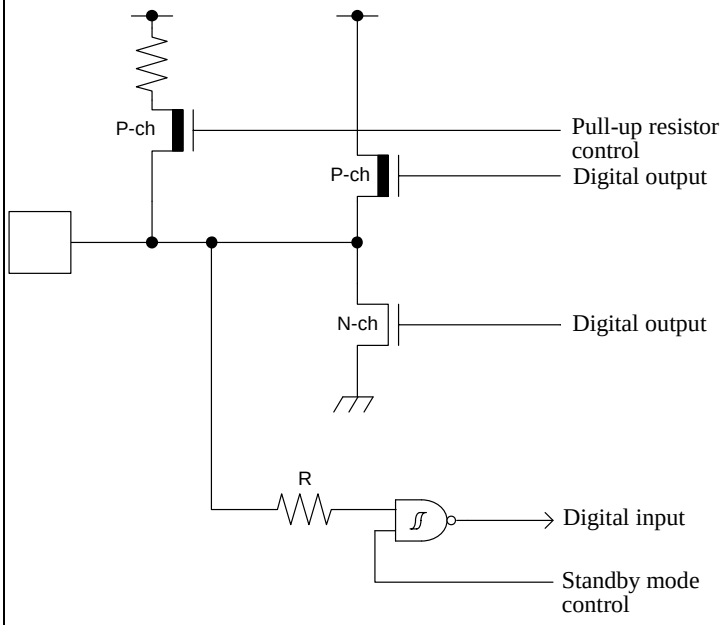
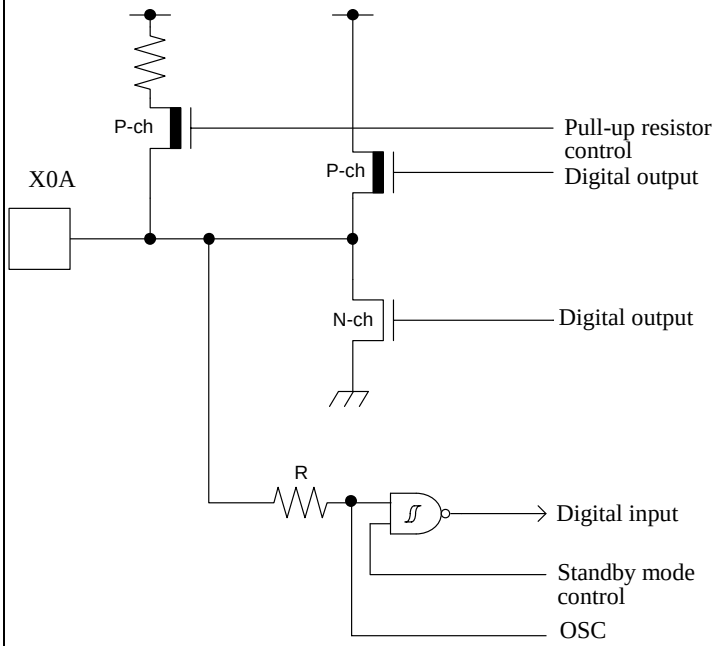
PFBGA-121

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
14	9	9	E1	P30	E	Q
				TIOB0_1		
				RTS4_2		
				INT15_2		
				WKUP1		
-			-	MADATA07_0		
14	-	-	E1	MADATA12_0		
	9	9		RTO25_1		
15	10	10	F4	P31	I	K
				TIOB1_1		
				SIN3_1		
				INT09_2		
-			-	MADATA08_0		
15	-	-	F4	MADATA13_0		
	10	10		DTTI2X_1		
16	11	11	F3	P32	N	K
				TIOB2_1		
				SOT3_1 (SDA3_1)		
				INT10_1		
-			-	MADATA09_0		
16	-	-	F3	MADATA14_0		
17	12	12	F2	P33	N	K
				ADTG_6		
				TIOB3_1		
				SCK3_1 (SCL3_1)		
				INT04_0		
-			-	MADATA10_0		
17	-	-	F2	MADATA15_0		
18	13	-	F1	P34	E	I
				TIOB4_1		
				FRCK0_0		
				TX0_1		
-			-	MADATA11_0		
18	-	-	F1	MNALE_0		
19	14	-	G1	P35	E	K
				TIOB5_1		
				IC03_0		
				INT08_1		
				RX0_1		
-			-	MADATA12_0		
19	-	-	G1	MNCLE_0		

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	-	H5
	TIOA3_1		27	22	17	J1
	TIOA3_2		97	82	67	D7
	TIOB3_0	Base timer ch.3 TIOB pin	49	44	34	J8
	TIOB3_1		17	12	12	F2
	TIOB3_2		98	83	-	C7
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	21	K3
	TIOA4_1		28	23	18	J2
	TIOA4_2		51	-	-	H6
	TIOB4_0	Base timer ch.4 TIOB pin	50	45	35	K8
	TIOB4_1		18	13	-	F1
	TIOB4_2		52	-	-	H7
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	84	-	-	C9
	TIOA5_1		29	24	19	K2
	TIOA5_2		93	78	63	A9
	TIOB5_0	Base timer ch.5 TIOB pin	83	-	-	D8
	TIOB5_1		19	14	-	G1
	TIOB5_2		92	77	62	B9
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-	G7
	TIOA6_1		94	79	64	C8
	TIOA6_2		82	-	-	E7
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-	H8
	TIOB6_1		95	80	65	B8
	TIOB6_2		81	-	-	F7
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-	C4
	TIOA7_1		86	71	57	D11
	TIOA7_2		109	-	-	E5
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-	D4
	TIOB7_1		87	72	58	C10
	TIOB7_2		108	-	-	E6
Debugger	SWCLK	Serial wire debug interface clock input pin	105	90	71	B5
	SWDIO	Serial wire debug interface data input / output pin	103	88	69	C6
	SWO	Serial wire viewer output pin	102	87	68	B6
	TCK	JTAG test clock input pin	105	90	71	B5
	TDI	JTAG test data input pin	104	89	70	C5
	TDO	JTAG debug data output pin	102	87	68	B6
	TMS	JTAG test mode state input/output pin	103	88	69	C6
	TRACECLK	Trace CLK output pin of ETM	101	86	-	D6
	TRACED0	Trace data output pin of ETM	97	82	-	D7
	TRACED1		98	83	-	C7
	TRACED2		99	84	-	B7
	TRACED3		100	85	-	A7
	TRSTX	JTAG test reset Input pin	106	91	72	A5

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Bus	MAD00_0	External bus interface address bus	27	22	17	J1
	MAD01_0		28	23	18	J2
	MAD02_0		29	24	19	K2
	MAD03_0		47	42	32	J6
	MAD04_0		48	43	33	J7
	MAD05_0		49	44	34	J8
	MAD06_0		50	45	35	K8
	MAD07_0		62	52	41	J10
	MAD08_0		63	53	42	H10
	MAD09_0		64	54	43	H9
	MAD10_0		65	55	44	G10
	MAD11_0		66	56	45	G9
	MAD12_0		67	57	46	G8
	MAD13_0		68	58	47	F10
	MAD14_0		69	59	48	F9
	MAD15_0		74	64	53	F8
	MAD16_0		75	65	54	E11
	MAD17_0		76	66	55	E10
	MAD18_0		77	67	56	E9
	MAD19_0		78	68	-	E8
	MAD20_0		79	69	-	D10
	MAD21_0		80	70	-	D9
	MAD22_0		86	71	-	D11
	MAD23_0		88	73	-	C11
	MAD24_0		89	74	-	B11

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	C1
	INT00_1		95	80	65	B8
	INT00_2		108	-	-	E6
	INT01_0	External interrupt request 01 input pin	3	3	3	C2
	INT01_1		101	86	-	D6
	INT01_2		85	-	-	B10
	INT02_0	External interrupt request 02 input pin	6	6	6	D3
	INT02_1		62	52	41	J10
	INT02_2		82	-	-	E7
	INT03_0	External interrupt request 03 input pin	113	93	73	B4
	INT03_1		65	55	44	G10
	INT03_2		54	-	-	H8
	INT04_0	External interrupt request 04 input pin	17	12	12	F2
	INT04_1		114	94	74	C3
	INT04_2		10	-	-	F5
	INT05_0	External interrupt request 05 input pin	89	74	-	B11
	INT05_1		75	65	54	E11
	INT05_2		21	16	-	G3
	INT06_1	External interrupt request 06 input pin	88	73	59	C11
	INT06_2		22	17	-	G4
	INT07_1	External interrupt request 07 input pin	11	-	-	F6
	INT07_2		7	7	7	E2
	INT08_1	External interrupt request 08 input pin	19	14	-	G1
	INT08_2		8	8	8	E3
	INT09_1	External interrupt request 09 input pin	20	15	-	G2
	INT09_2		15	10	10	F4
	INT10_1	External interrupt request 10 input pin	16	11	11	F3
	INT10_2		112	-	-	C4
	INT11_1	External interrupt request 11 input pin	50	45	35	K8
	INT11_2		110	-	-	D5
	INT12_1	External interrupt request 12 input pin	32	27	-	L2
	INT12_2		96	81	66	A8
	INT13_1	External interrupt request 13 input pin	33	28	-	J3
	INT13_2		49	44	34	J8
	INT14_1	External interrupt request 14 input pin	68	58	47	F10
	INT14_2		53	-	-	G7
	INT15_1	External interrupt request 15 input pin	52	-	-	H7
	INT15_2		14	9	9	E1
External Interrupt	NMIX	Non-Maskable Interrupt input pin	116	96	76	B2

Type	Circuit	Remarks
O		– CMOS level output – CMOS level hysteresis input – 5 V tolerant – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual
P		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual

8. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation(other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation *5 (main oscillation)	4MHz	2.1	22	mA	*3 When all peripheral clocks are ON
					1.3	22	mA	*3 When all peripheral clocks are OFF
			Sleep operation (built-in high-speed CR)	4 MHz	1.3	22	mA	*3 When all peripheral clocks are ON
					0.8	21	mA	*3 When all peripheral clocks are OFF
			Sleep operation (sub oscillation)	32 kHz	0.28	21	mA	*3 When all peripheral clocks are ON
					0.27	21	mA	*3 When all peripheral clocks are OFF
			Sleep operation (built-in low-speed CR)	100 kHz	0.29	21	mA	*3 When all peripheral clocks are ON
					0.28	21	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0"

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
		8 mA type	$V_{CC} \geq 4.5$ V, I_{OH} = 8 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OH} = 4 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OH} = 4 mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5$ V, I_{OH} = 3 mA					
			$V_{CC} \leq 5.5$ V, I_{OH} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

13.4.9 External Bus Timing

External Bus Clock Output Characteristics

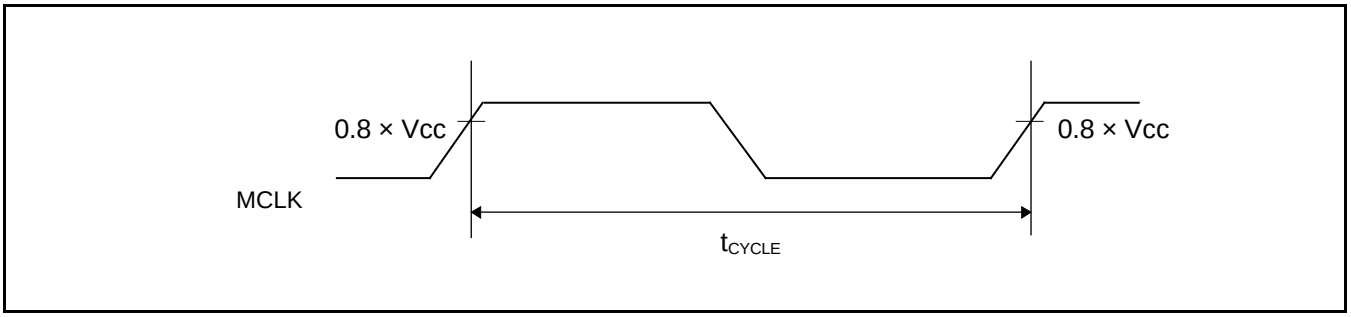
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	$V_{CC} \geq 4.5$ V	-	50*2	MHz
			$V_{CC} < 4.5$ V	-	32*3	MHz

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main part (002-04856).

*2: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 100 MHz.

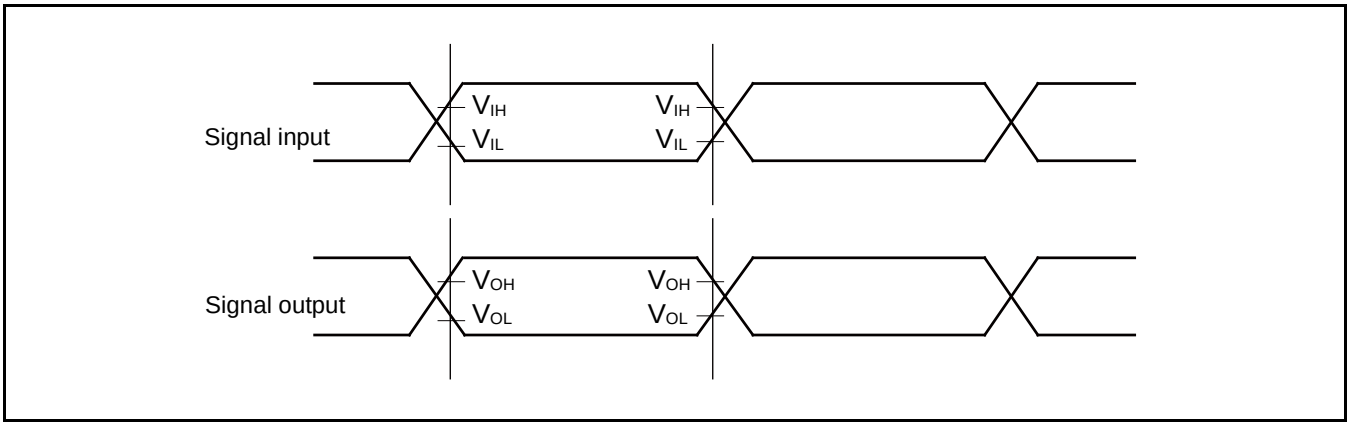
*3: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 64 MHz.

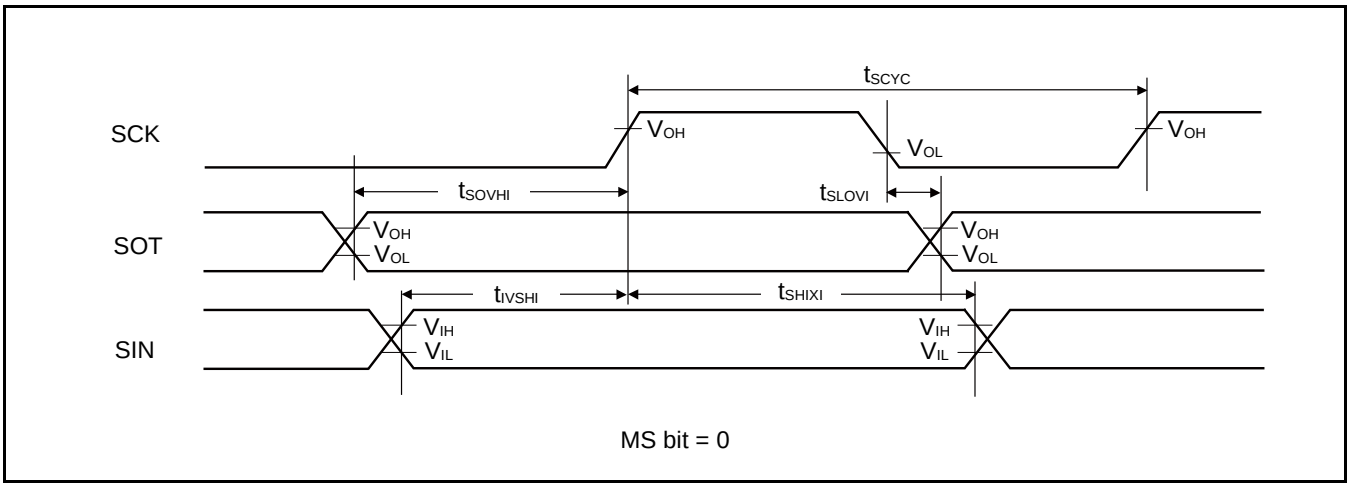


External Bus Signal Input/output Characteristics

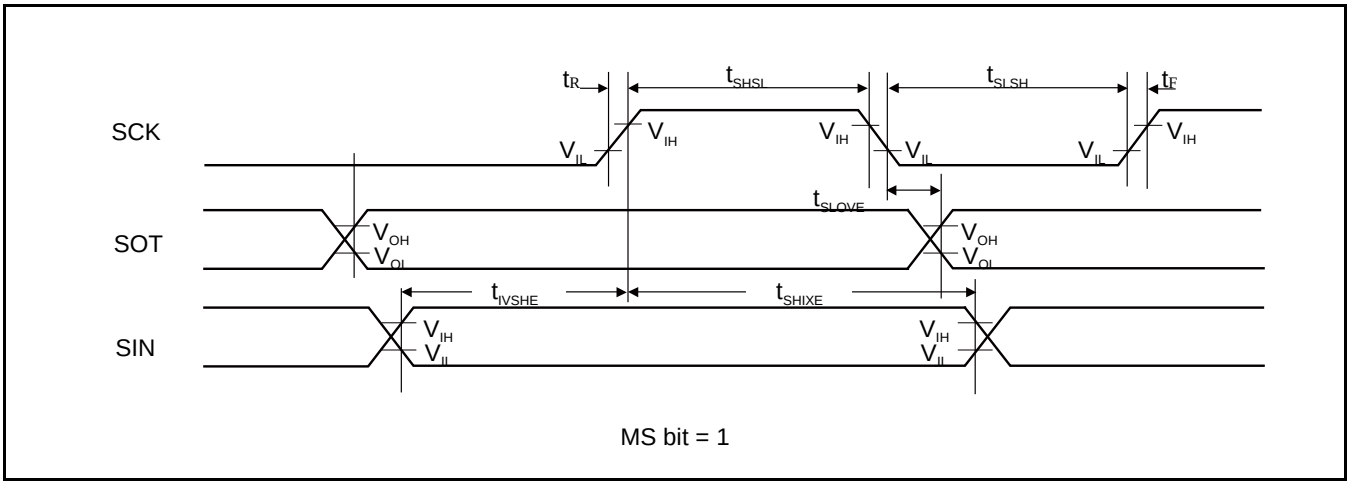
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	





MS bit = 0



MS bit = 1

When Using High-speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

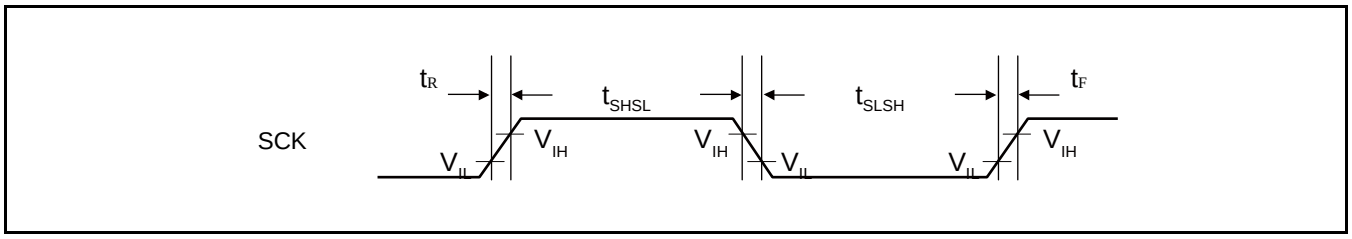
Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

External Clock (EXT = 1): when in Asynchronous Mode Only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



13.4.14 I²C Timing

Standard-mode, Fast-mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP}<40 MHz	$2t_{CYCP}$*4	-	$2t_{CYCP}$*4	-	ns	*5
		40 MHz ≤ t_{CYCP}<60 MHz	$4t_{CYCP}$*4	-	$4t_{CYCP}$*4	-	ns	
		60 MHz ≤ t_{CYCP}<80 MHz	$6t_{CYCP}$*4	-	$6t_{CYCP}$*4	-	ns	
		80 MHz ≤ t_{CYCP}<100 MHz	$8t_{CYCP}$*4	-	$8t_{CYCP}$*4	-	ns	
		100 MHz ≤ t_{CYCP}<120 MHz	$10t_{CYCP}$*4	-	$10t_{CYCP}$*4	-	ns	
		120 MHz ≤ t_{CYCP}<140 MHz	$12t_{CYCP}$*4	-	$12t_{CYCP}$*4	-	ns	
		140 MHz ≤ t_{CYCP}<160 MHz	$14t_{CYCP}$*4	-	$14t_{CYCP}$*4	-	ns	
		160 MHz ≤ t_{CYCP}<180 MHz	$16t_{CYCP}$*4	-	$16t_{CYCP}$*4	-	ns	

1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

2: The maximum t_{HDDAT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

3: Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I²C is connected, see 1.S6E2H Series Block Diagram in this data sheet.
When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.
When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.

5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

Fast Mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast Mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	1000	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock L width	t_{LOW}		0.5	-	µs	
SCL clock H width	t_{HIGH}		0.26	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		0.26	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP}<80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP}<100 MHz	8 t_{CYCP}*4	-	ns	
		100 MHz ≤ t_{CYCP}<120 MHz	10 t_{CYCP}*4	-	ns	
		120 MHz ≤ t_{CYCP}<140 MHz	12 t_{CYCP}*4	-	ns	
		140 MHz ≤ t_{CYCP}<160 MHz	14 t_{CYCP}*4	-	ns	
		160 MHz ≤ t_{CYCP}<180 MHz	16 t_{CYCP}*4	-	ns	

1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

2: The maximum t_{HDDAT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

3: The Fast mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns."

4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I^2C is connected, see 1.S6E2H Series Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register.
See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.

13.7 Low-Voltage Detection Characteristics

13.7.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

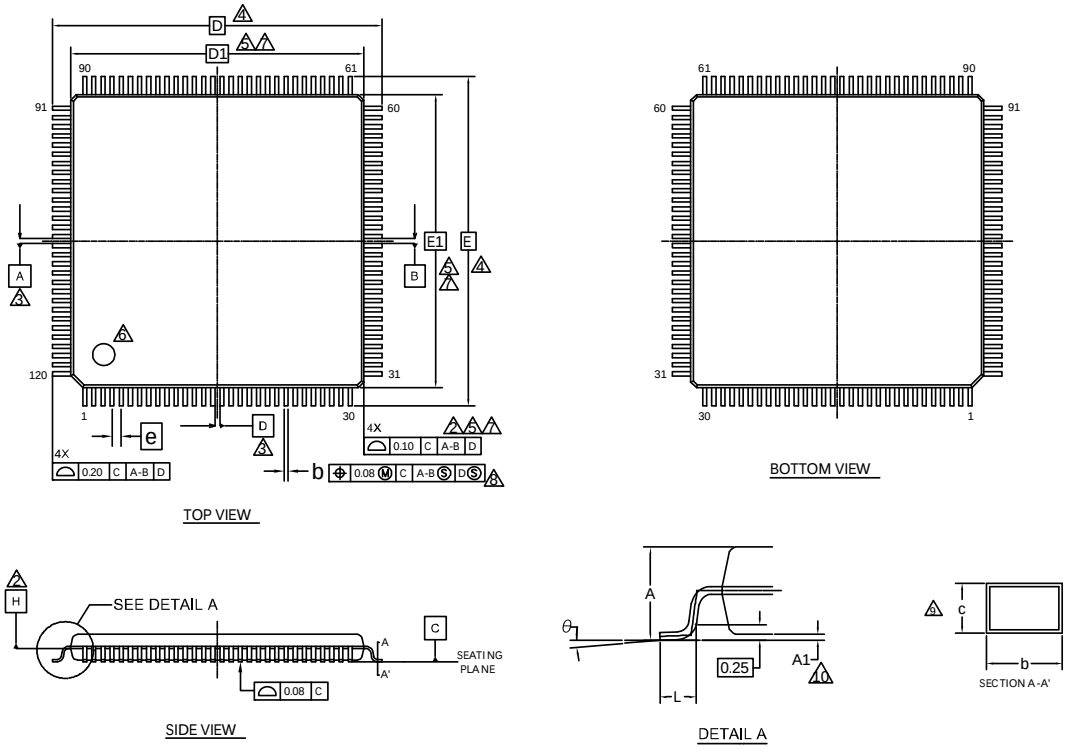
13.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	4480× t_{CYCP}*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

15. Package Dimensions

Package Type	Package Code
LQFP 120	LQM120



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.50 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

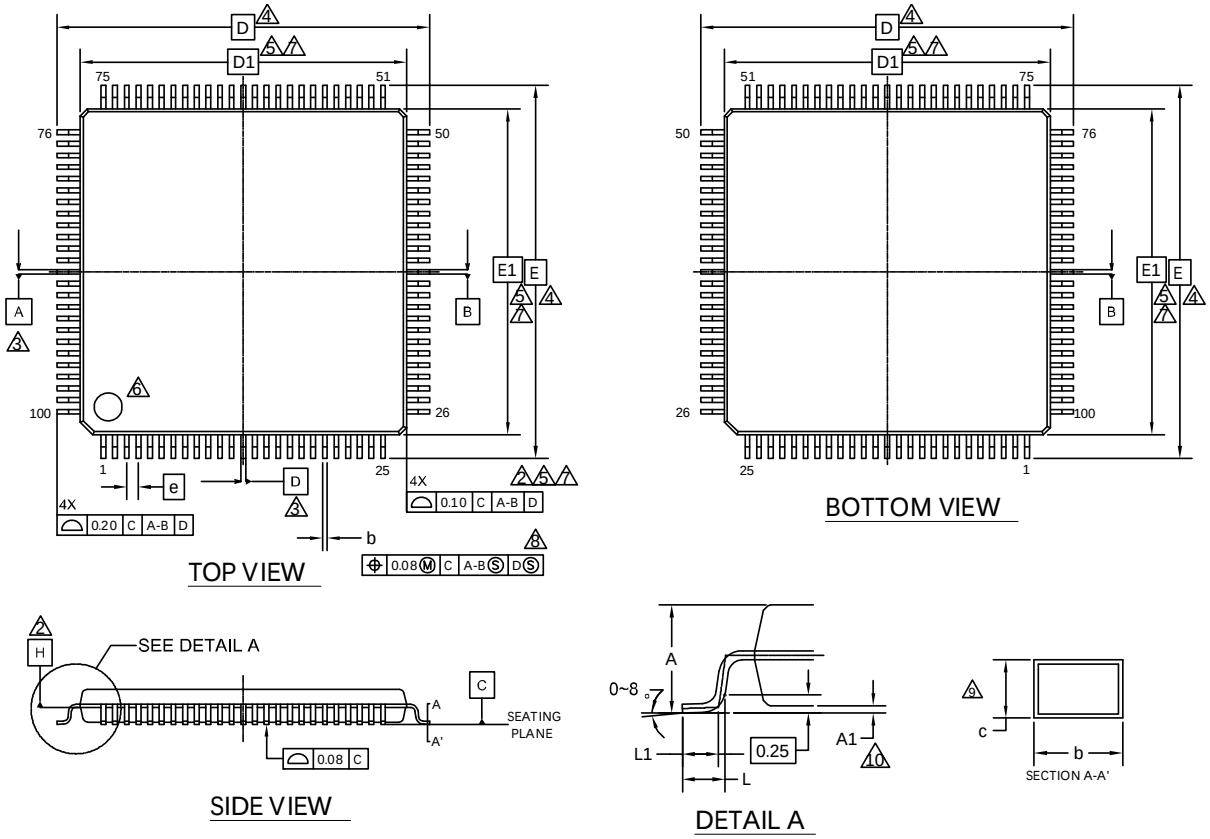
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

002-16172 **

Package Type	Package Code
LQFP 100	LQI100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 Rev** 002-11500 **