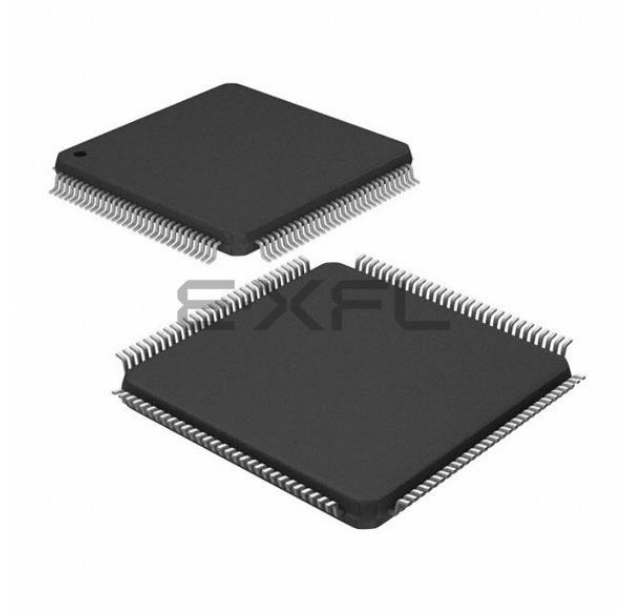


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2hg4g0agv20000

4. Detailed Product Features

32-bit ARM Cortex-M4F Core

- Up to 160 MHz Frequency Operation
- FPU built-in
- Support DSP instruction
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

- Flash memory

These series are based on two independent on-chip Flash memories.

  - MainFlash memory
    - Up to 512 Kbytes
    - Built-in Flash Accelerator System with 16 Kbytes trace buffer memory
    - The read access to Flash memory can be achieved without wait-cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
    - Security function for code protection
  - WorkFlash memory
    - 32 Kbytes
    - Read cycle:
    - 6 wait-cycle: the operation frequency more than 120 MHz, and up to 160 MHz
    - 4 wait-cycle: the operation frequency more than 72 MHz, and up to 120 MHz
    - 2 wait-cycle: the operation frequency more than 40 MHz, and up to 72 MHz
    - 0 wait-cycle: the operation frequency up to 40 MHz
    - Security function is shared with code protection

- SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to I-code bus or D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to System bus of Cortex-M4F core.

  - SRAM0: Up to 32 Kbytes
  - SRAM1: Up to 16 Kbytes
  - SRAM2: Up to 16 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND Flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Supports Address/Data multiplex
- Supports external RDY function
- Supports scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key
  - **Note**: It is necessary to prepare the dedicated software library to use the scramble function.

CAN Interface (Max 2 channels)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32 message buffer

Multi-function Serial Interface (Max 8 channels)

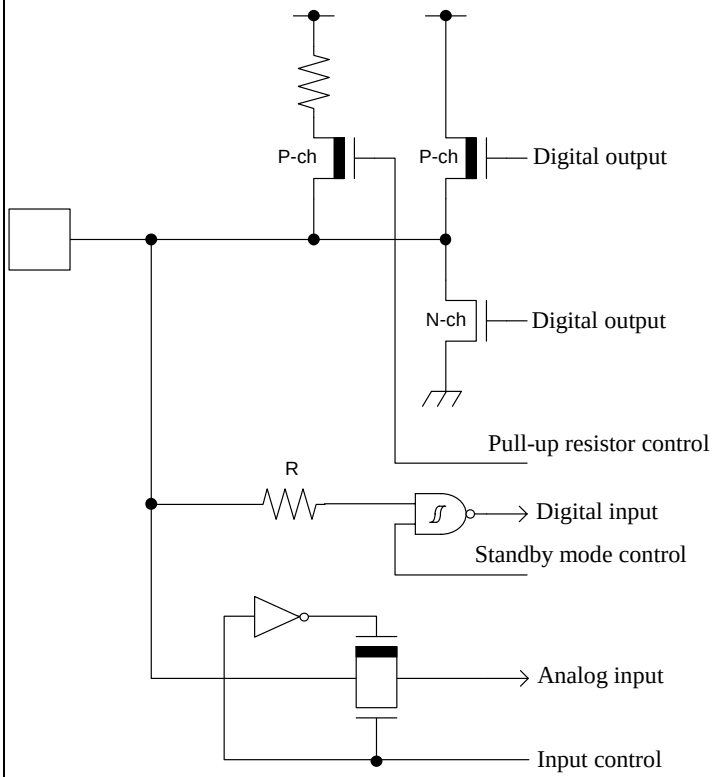
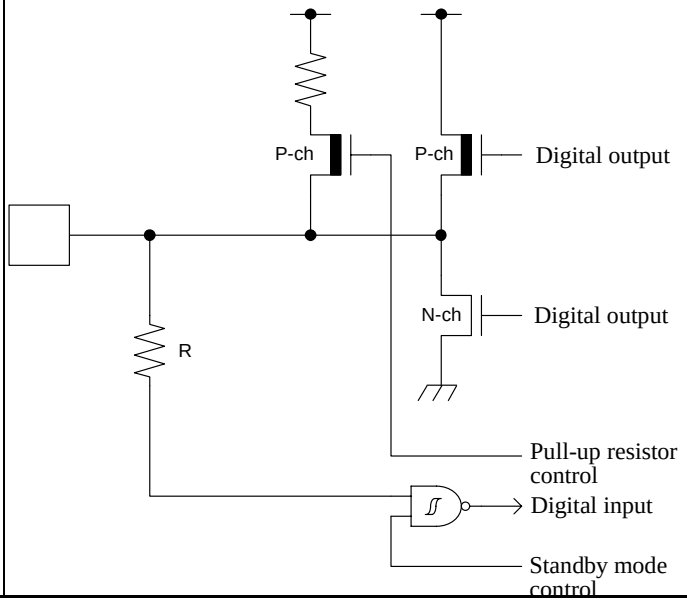
- 64 bytes with FIFO (the FIFO step numbers are variable depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 and ch.7 only)
  - Supports high-speed SPI (ch.4 and ch.6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation (can change to 13 to 16-bit length)
  - LIN break delimiter generation (can change to 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)

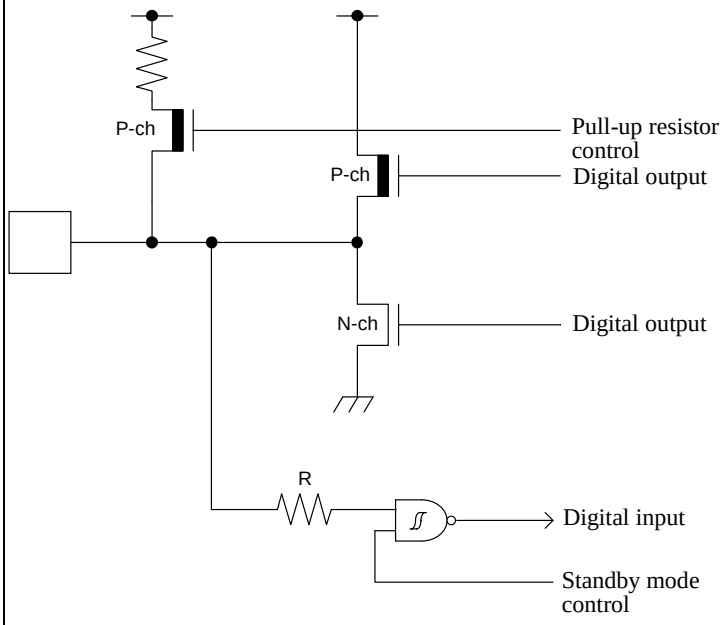
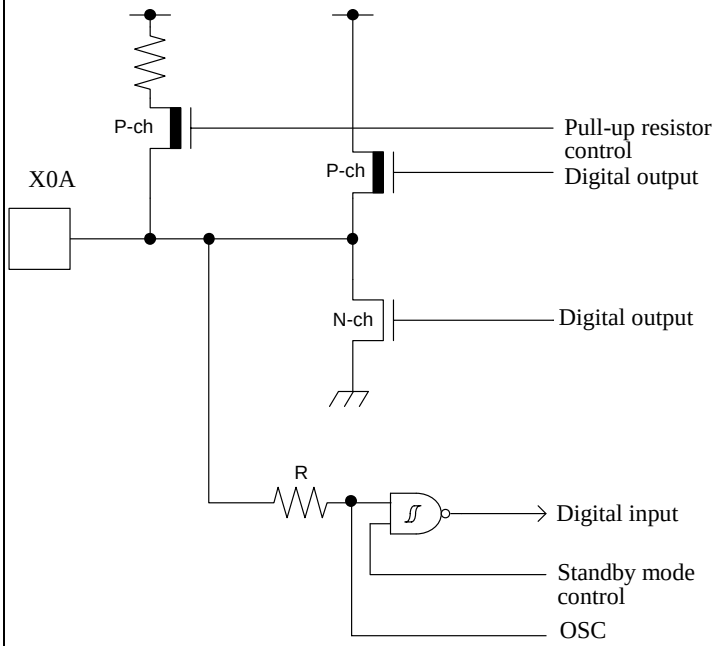
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
28	23	18	J2	P3E TIOA4_1 RTO04_0 (PPG04_0) MAD01_0	G	I
29	24	19	K2	P3F TIOA5_1 RTO05_0 (PPG04_0) MAD02_0	G	I
30	25	20	L1	VSS	-	-
31	26	-	K1	VCC	-	-
32	27	-	L2	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	K
33	28	-	J3	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1 AIN2_0	G	K
34	29	-	J5	P42 TIOA2_0 RTO12_1 (PPG12_1) MSDWEX_0 BIN2_0	G	I
35	30	-	H5	P43 ADTG_7 TIOA3_0 RTO13_1 (PPG12_1) MCSX8_0 ZIN2_0	G	I
36	31	21	K3	P44 TIOA4_0 RTO14_1 (PPG14_1) DA0	R	J
37	32	22	J4	P45 TIOB0_0 RTO15_1 (PPG14_1) DA1	R	J
38	33	23	L3	INITX	B	C

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
74	64	53	F8	P18 AN08 SCK2_2 (SCL2_2) MAD15_0 DTTI2X_0	F	L
75	65	54	E11	P19 AN09 SIN4_1 IC00_1 INT05_1 MAD16_0	F	M
76	66	55	E10	P1A AN10 SOT4_1 (SDA4_1) IC01_1 MAD17_0	M	L
77	67	56	E9	P1B AN11 SCK4_1 (SCL4_1) IC02_1 MAD18_0	M	L
78	68	-	E8	P1C AN12 CTS4_1 IC03_1 MAD19_0	F	L
79	69	-	D10	P1D AN13 RTS4_1 DTTI0X_1 MAD20_0	F	L
80	70	-	D9	P1E AN14 ADTG_5 FRCK0_1 MAD21_0	F	L
81	-	-	F7	P1F ADTG_4 TIOB6_2 RTO05_1 (PPG04_1)	E	I

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	-	H5
	TIOA3_1		27	22	17	J1
	TIOA3_2		97	82	67	D7
	TIOB3_0	Base timer ch.3 TIOB pin	49	44	34	J8
	TIOB3_1		17	12	12	F2
	TIOB3_2		98	83	-	C7
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	21	K3
	TIOA4_1		28	23	18	J2
	TIOA4_2		51	-	-	H6
	TIOB4_0	Base timer ch.4 TIOB pin	50	45	35	K8
	TIOB4_1		18	13	-	F1
	TIOB4_2		52	-	-	H7
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	84	-	-	C9
	TIOA5_1		29	24	19	K2
	TIOA5_2		93	78	63	A9
	TIOB5_0	Base timer ch.5 TIOB pin	83	-	-	D8
	TIOB5_1		19	14	-	G1
	TIOB5_2		92	77	62	B9
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-	G7
	TIOA6_1		94	79	64	C8
	TIOA6_2		82	-	-	E7
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-	H8
	TIOB6_1		95	80	65	B8
	TIOB6_2		81	-	-	F7
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-	C4
	TIOA7_1		86	71	57	D11
	TIOA7_2		109	-	-	E5
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-	D4
	TIOB7_1		87	72	58	C10
	TIOB7_2		108	-	-	E6
Debugger	SWCLK	Serial wire debug interface clock input pin	105	90	71	B5
	SWDIO	Serial wire debug interface data input / output pin	103	88	69	C6
	SWO	Serial wire viewer output pin	102	87	68	B6
	TCK	JTAG test clock input pin	105	90	71	B5
	TDI	JTAG test data input pin	104	89	70	C5
	TDO	JTAG debug data output pin	102	87	68	B6
	TMS	JTAG test mode state input/output pin	103	88	69	C6
	TRACECLK	Trace CLK output pin of ETM	101	86	-	D6
	TRACED0	Trace data output pin of ETM	97	82	-	D7
	TRACED1		98	83	-	C7
	TRACED2		99	84	-	B7
	TRACED3		100	85	-	A7
	TRSTX	JTAG test reset Input pin	106	91	72	A5

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	C1
	INT00_1		95	80	65	B8
	INT00_2		108	-	-	E6
	INT01_0	External interrupt request 01 input pin	3	3	3	C2
	INT01_1		101	86	-	D6
	INT01_2		85	-	-	B10
	INT02_0	External interrupt request 02 input pin	6	6	6	D3
	INT02_1		62	52	41	J10
	INT02_2		82	-	-	E7
	INT03_0	External interrupt request 03 input pin	113	93	73	B4
	INT03_1		65	55	44	G10
	INT03_2		54	-	-	H8
	INT04_0	External interrupt request 04 input pin	17	12	12	F2
	INT04_1		114	94	74	C3
	INT04_2		10	-	-	F5
	INT05_0	External interrupt request 05 input pin	89	74	-	B11
	INT05_1		75	65	54	E11
	INT05_2		21	16	-	G3
	INT06_1	External interrupt request 06 input pin	88	73	59	C11
	INT06_2		22	17	-	G4
	INT07_1	External interrupt request 07 input pin	11	-	-	F6
	INT07_2		7	7	7	E2
	INT08_1	External interrupt request 08 input pin	19	14	-	G1
	INT08_2		8	8	8	E3
	INT09_1	External interrupt request 09 input pin	20	15	-	G2
	INT09_2		15	10	10	F4
	INT10_1	External interrupt request 10 input pin	16	11	11	F3
	INT10_2		112	-	-	C4
	INT11_1	External interrupt request 11 input pin	50	45	35	K8
	INT11_2		110	-	-	D5
	INT12_1	External interrupt request 12 input pin	32	27	-	L2
	INT12_2		96	81	66	A8
	INT13_1	External interrupt request 13 input pin	33	28	-	J3
	INT13_2		49	44	34	J8
	INT14_1	External interrupt request 14 input pin	68	58	47	F10
	INT14_2		53	-	-	G7
	INT15_1	External interrupt request 15 input pin	52	-	-	H7
	INT15_2		14	9	9	E1
External Interrupt	NMIX	Non-Maskable Interrupt input pin	116	96	76	B2

Type	Circuit	Remarks
F		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
G		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -12 mA, I_{OL} = 12 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
O		– CMOS level output – CMOS level hysteresis input – 5 V tolerant – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual
P		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual

9. Handling Devices

Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS near this device.

Power Supply Pins

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  Size: More than 3.2 mm × 1.5 mm
  Load capacitance: Approximately 6 pF to 7 pF
- Lead type
  Load capacitance: Approximately 6 pF to 7 pF

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4002_2FFF		Multi-function timer unit2
0x4002_3000	0x4003_FFFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A Converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		RTC/Port Ctrl
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch.0
0x4006_3000	0x4006_3FFF		CAN ch.1
0x4006_4000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD-Card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4006_7000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		WorkFlash I/F register

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) *1 ,*3	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1 ,*4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1 ,*4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current *5	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
L level average output current *6	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current *7	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current *6	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	8 mA type
			- 20	mA	12 mA type
H level average output current *6	I_{OHAV}	-	- 4	mA	4 mA type
			- 8	mA	8 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current *7	$\sum I_{OHAV}$	-	- 50	mA	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: V_{BAT} must not drop below V_{SS} - 0.5 V.

*4: Ensure that the voltage does not exceed V_{CC} + 0.5V, for example, when the power is turned on.

*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
  Do not exceed any of these ratings.

13.4.9 External Bus Timing

External Bus Clock Output Characteristics

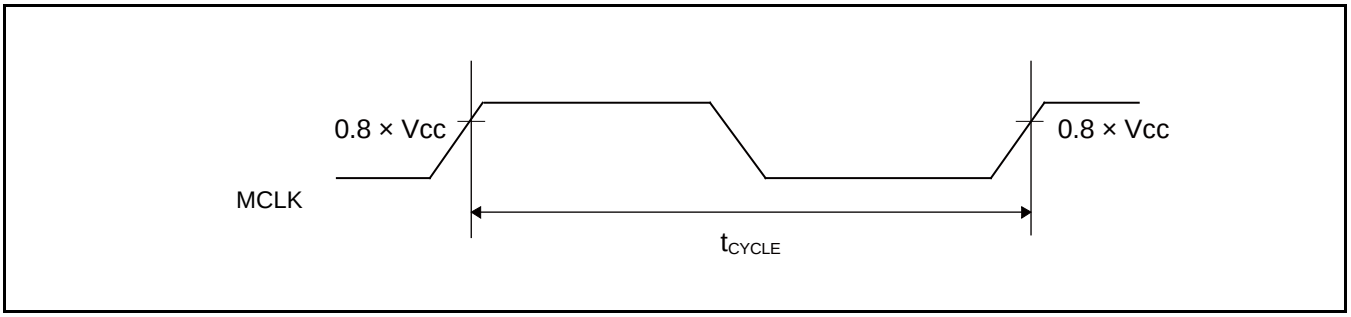
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	$V_{CC} \geq 4.5$ V	-	50*2	MHz
			$V_{CC} < 4.5$ V	-	32*3	MHz

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main part (002-04856).

*2: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 100 MHz.

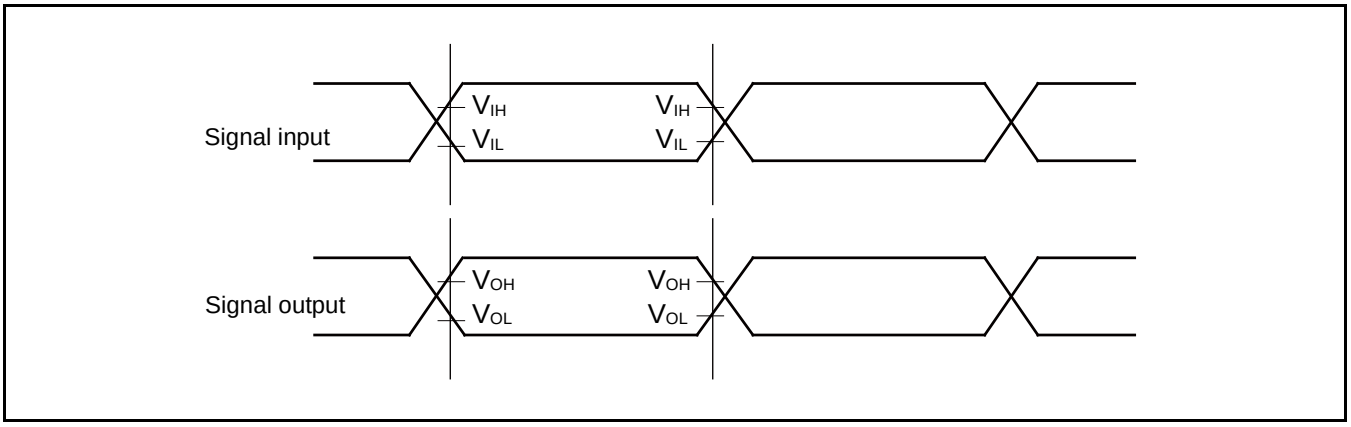
*3: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 64 MHz.



External Bus Signal Input/output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



NAND Flash Mode

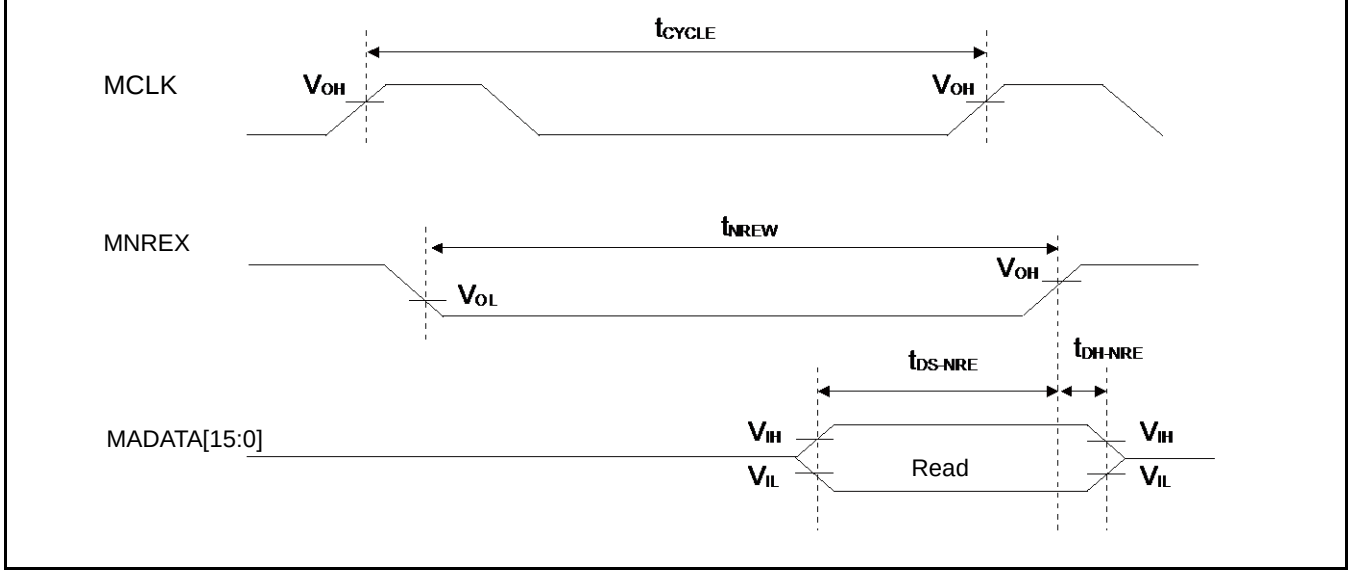
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
Data set up →MNREX↑ time	t_{DS-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MNREX↑→ Data hold time	t_{DH-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MNALE↑→ MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNALE↓→ MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNCLE↑→ MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNWEX↑→ MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MNWEX Min pulse width	t_{NWEW}	MNWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MNWEX↓→ Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	- 9	+ 9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MNWEX↑→ Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

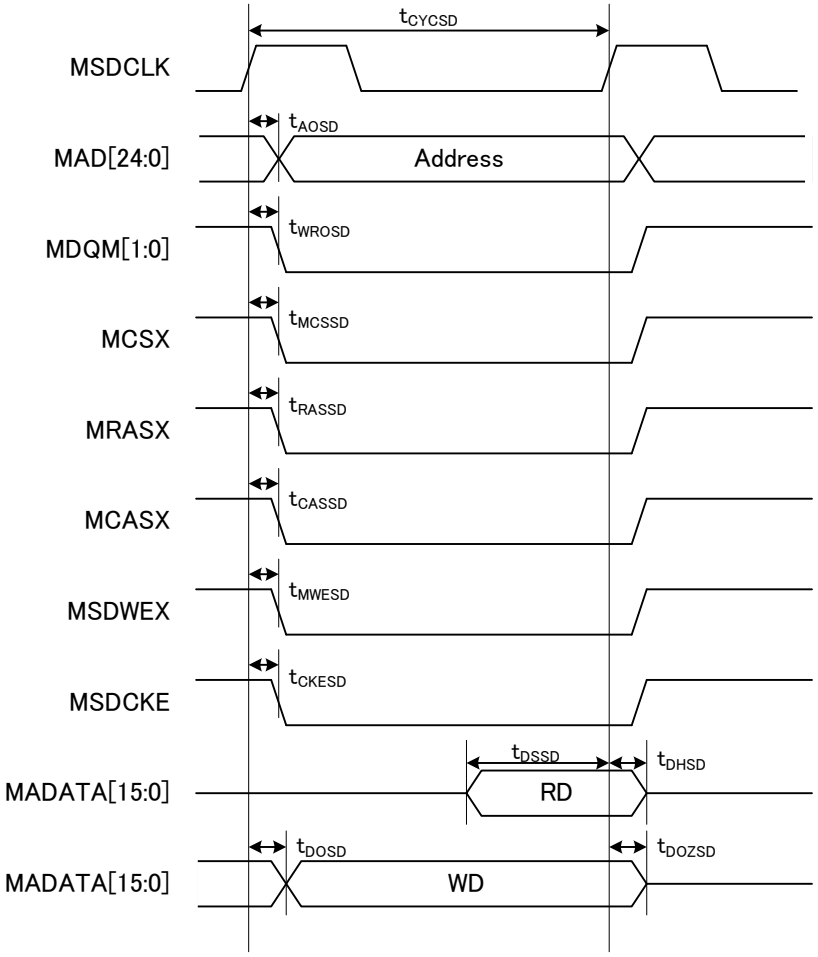
Note:

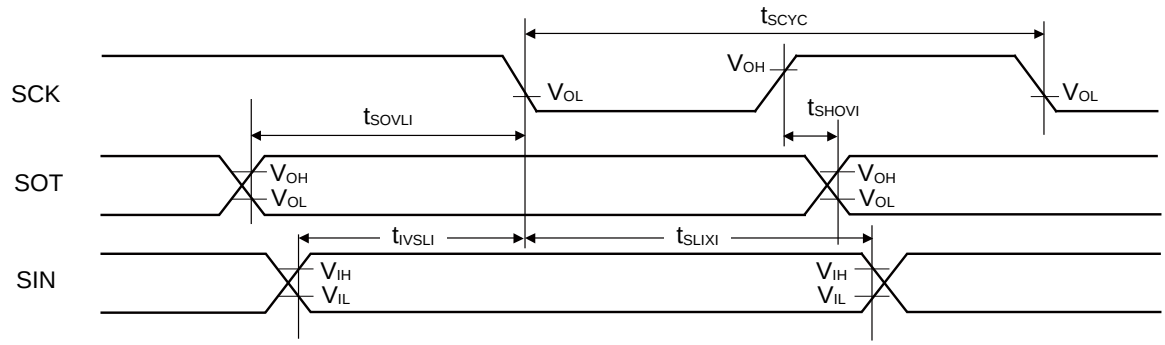
- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*

NAND Flash Read

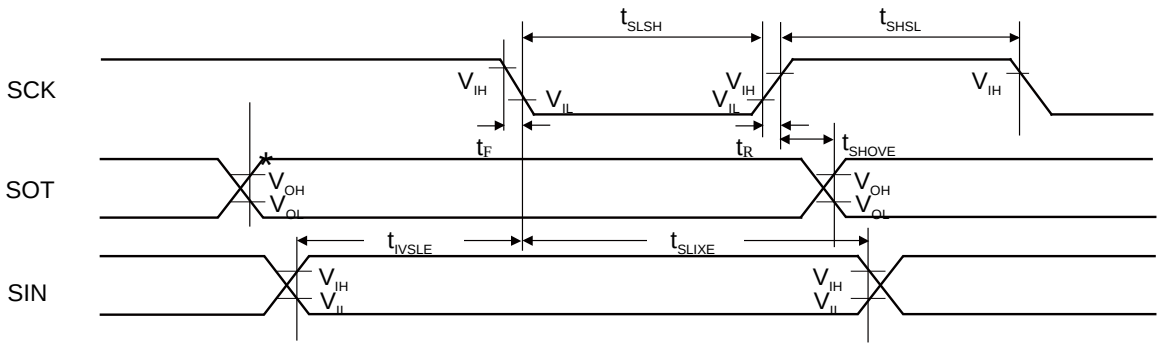


SDRAM Access



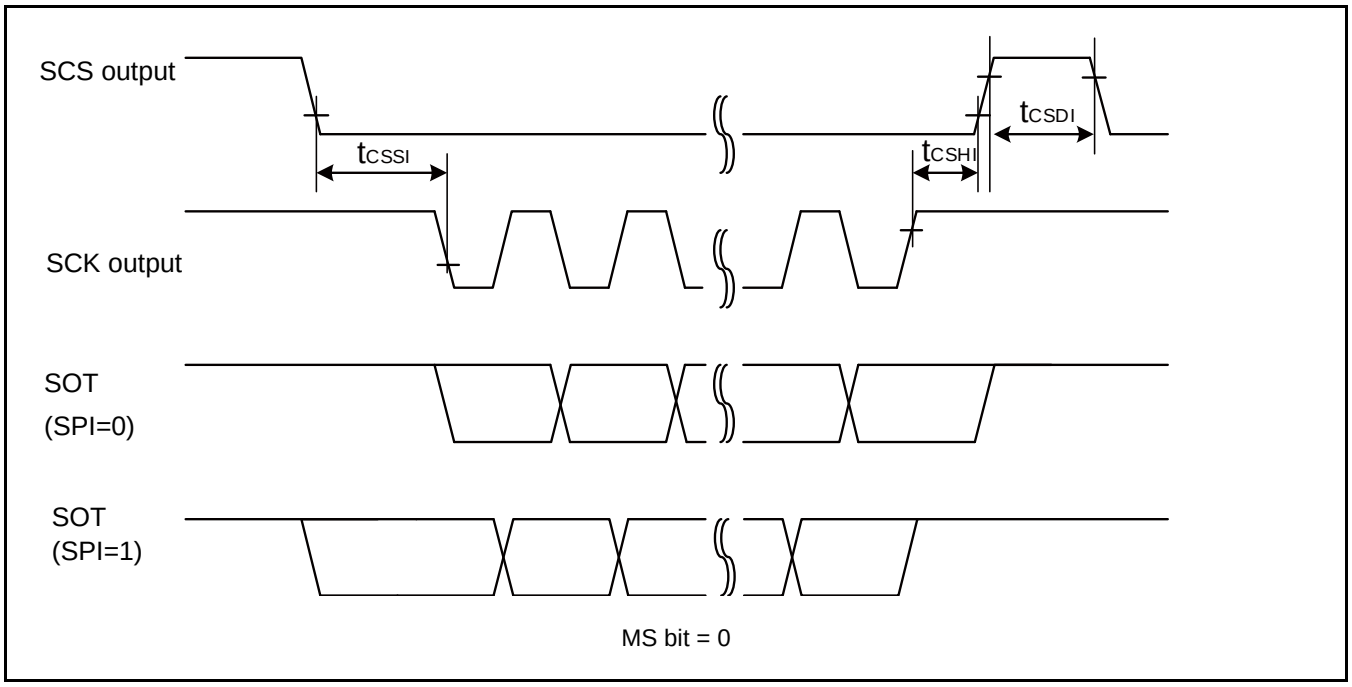


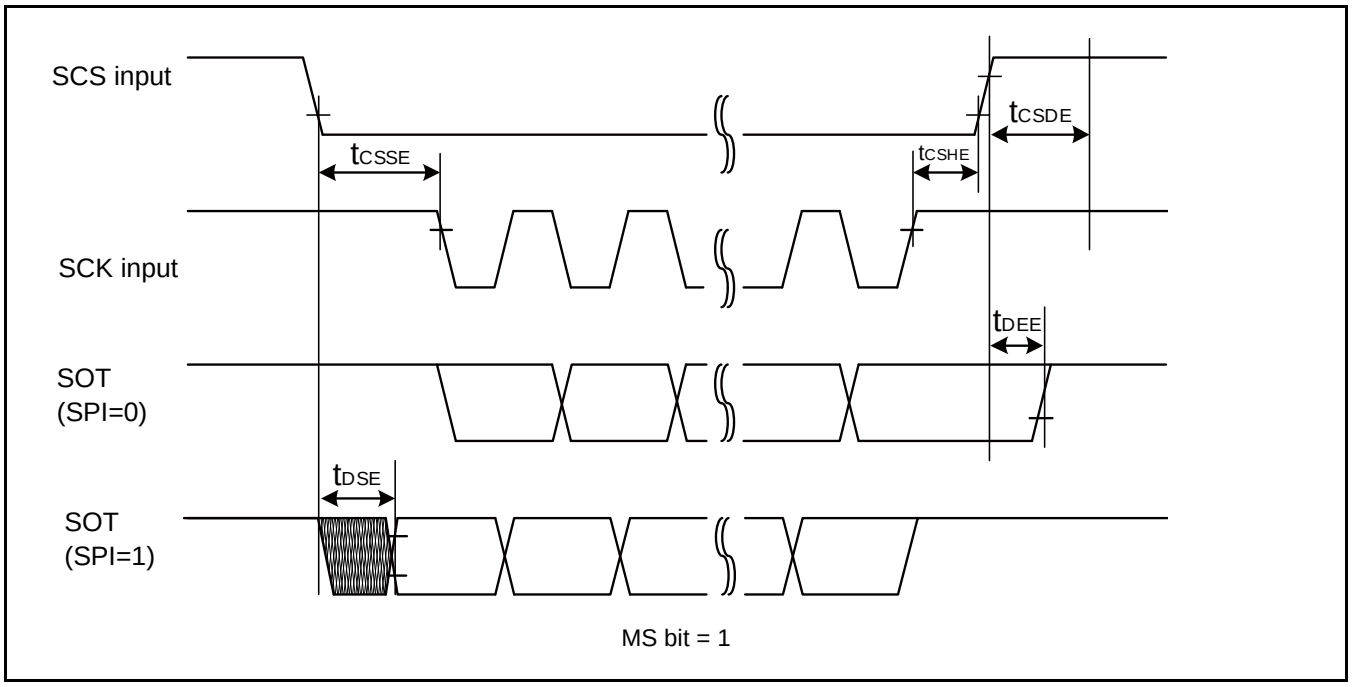
MS bit = 0



MS bit = 1

*: Changes when writing to TDR register


SCS output
tCSSI
tCSDI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)
MS bit = 0


SCS input
tCSSE
tCSDE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)
MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

High-speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ →SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK ↓ →SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ →SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK ↓ →SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
- *No chip select: SIN4_1, SOT4_1, SCK4_1*
- *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

When Using High-speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

13.4.12 External Input Timing

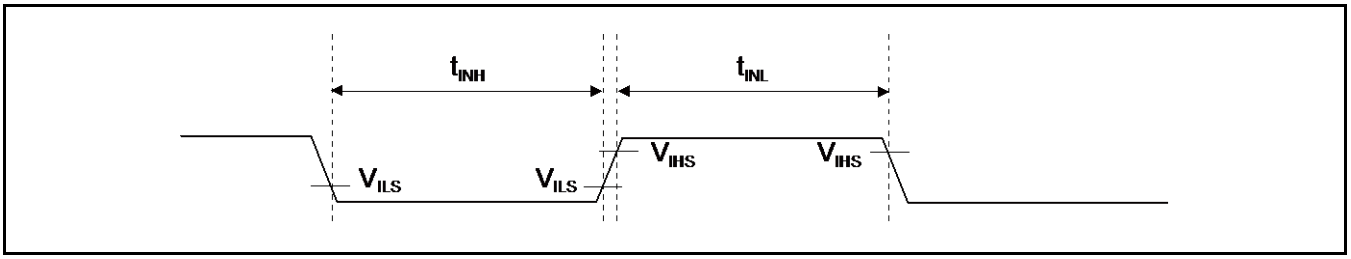
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT15, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

*1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode.
About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see 1. S6E2H Series Block Diagram in this data sheet.

*2: When in Stop mode, in timer mode.

*3: When in deep standby RTC mode, in deep standby Stop mode.



13.4.17 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

Note:

- *When the external load capacitance C_L= 30 pF.*