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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	63
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2hg6e0agv20000

2. Product Lineup

Memory Size

Product name		S6E2HG4 S6E2HE4 S6E2H44 S6E2H14	S6E2HG6 S6E2HE6 S6E2H46 S6E2H16
MainFlash memory		256 Kbytes	512 Kbytes
WorkFlash memory		32 Kbytes	32 Kbytes
On-chip SRAM		32 Kbytes	64 Kbytes
	SRAM0	16 Kbytes	32 Kbytes
	SRAM1	8 Kbytes	16 Kbytes
	SRAM2	8 Kbytes	16 Kbytes

Function Availability by Part

Description			Product Name			
			S6E2HG6 S6E2HG4	S6E2HE6 S6E2HE4	S6E2H46 S6E2H44	S6E2H16 S6E2H14
CPU			Cortex-M4F, MPU, NVIC 128ch.			
	Freq.		160 MHz			
Power supply voltage range			2.7 V to 5.5 V			
CAN			2ch. (Max)	N/A	2ch. (Max)	N/A
DMAC			8ch.			
DSTC			256ch.			
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8ch. (Max)			
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)			
MF Timer	A/D activation compare	6ch.	3 units (Max)			
	Input capture	4ch.				
	Free-run timer	3ch.				
	Output compare	6ch.				
	Waveform generator	3ch.				
	PPG	3ch.				
SD Card Interface			1 unit		N/A	
QPRC			3ch. (Max)			
Dual Timer			1 unit			
Real-Time Clock			1 unit			
Watch Counter			1 unit			

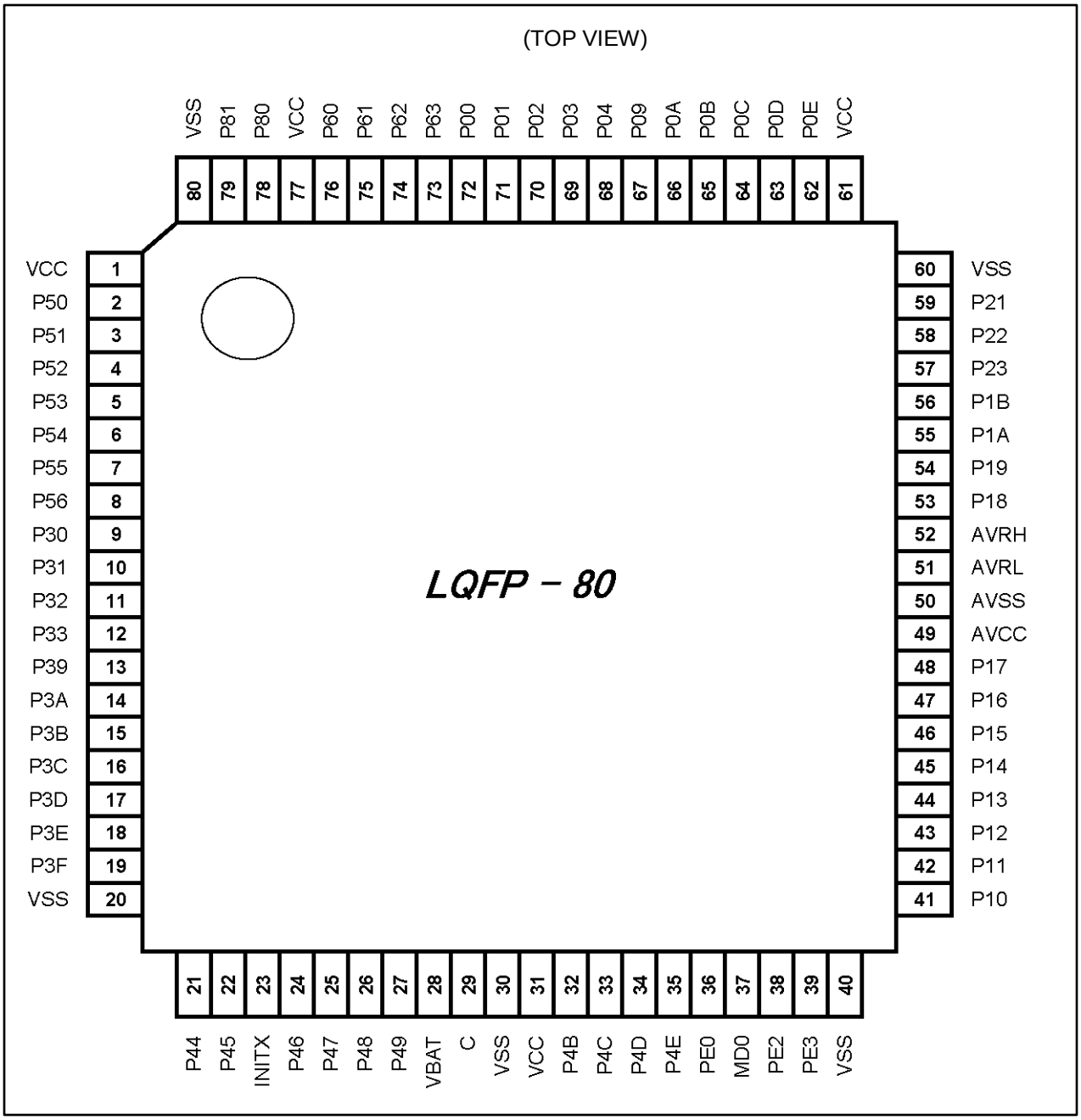
Description		Product Name			
		S6E2HG6 S6E2HG4	S6E2HE6 S6E2HE4	S6E2H46 S6E2H44	S6E2H16 S6E2H14
CRC Accelerator		Yes			
Watchdog Timer		1ch. (SW) + 1ch. (HW)			
External Interrupts		16 pins (Max) + NMI × 1			
12-bit D/A Converter		2 units (Max)			
CSV (Clock Super Visor)		Yes			
LVD (Low-Voltage Detector)		2ch.			
Built-in CR	High-speed	4 MHz (±2%)			
	Low-speed	100 kHz (Typ)			
Debug Function		SWJ-DP/ETM			
Unique ID		Yes			

Notes:

- *Because of package pin limitations, not all functions within the device can be brought out to external pins. You must carefully work out the pin allocation needed for your design.*
  You must use the port relocate function of the I/O port according to your function use.
- *See 13.4.3 Built-in CR Oscillation Characteristics for the accuracy of the built-in CR.*

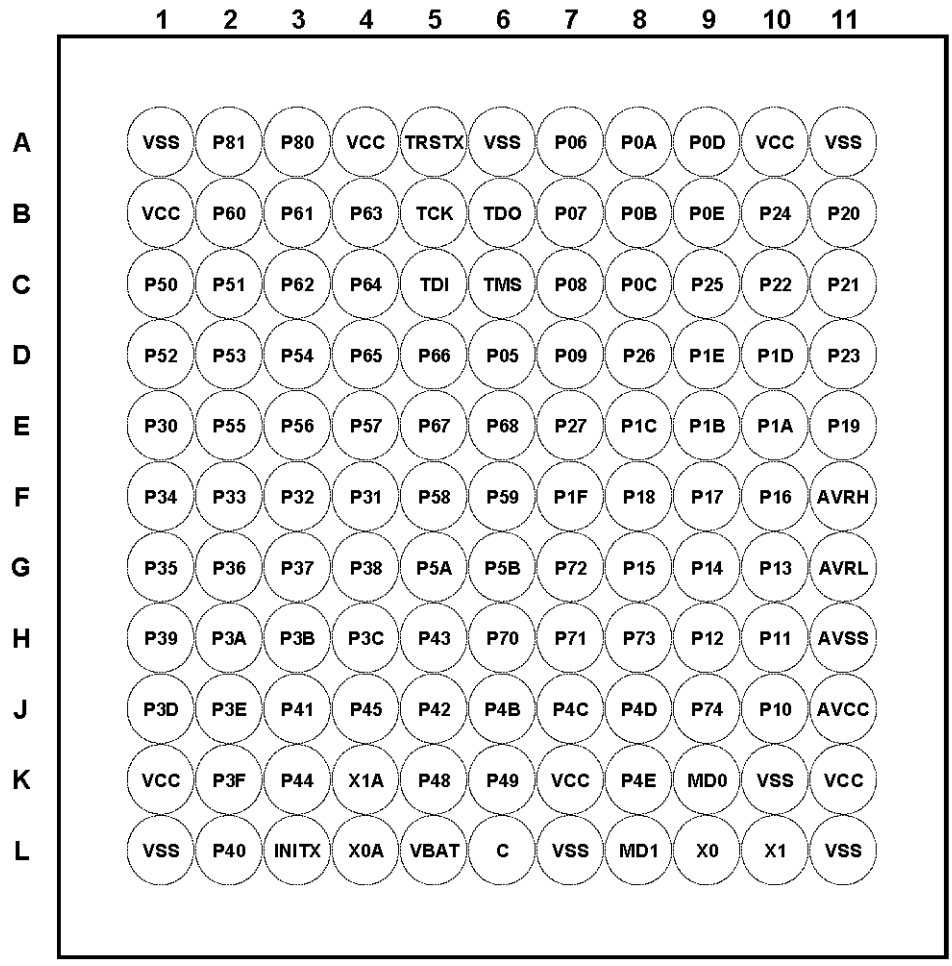
5. Pin Assignment

LQH080



FDI121

(TOP VIEW)

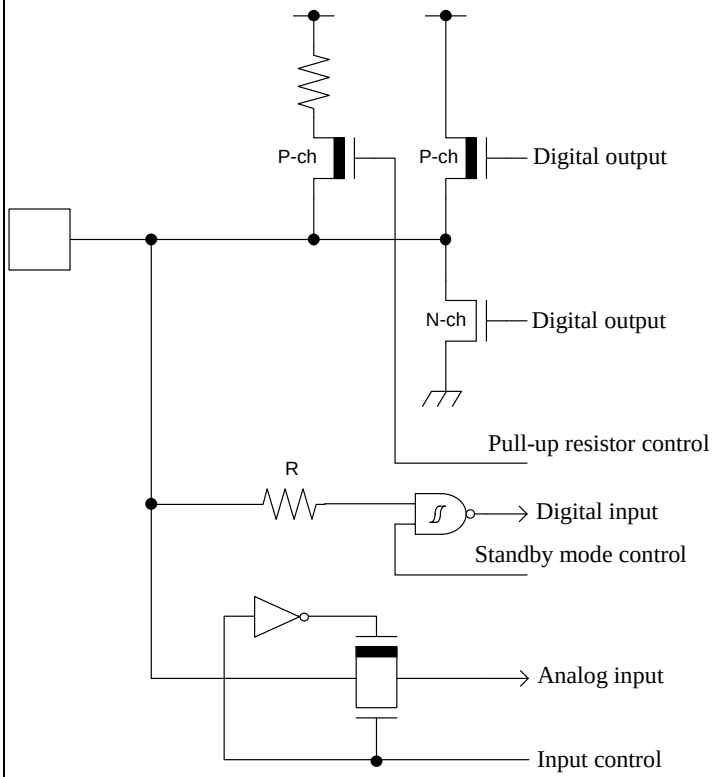
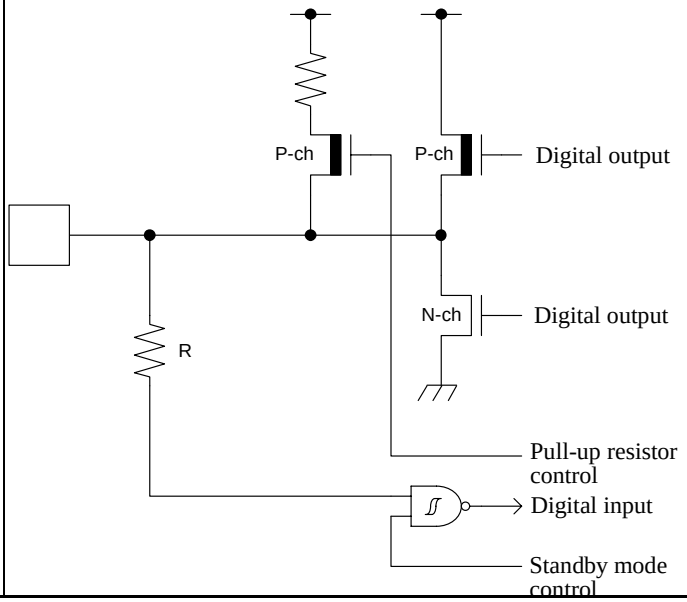


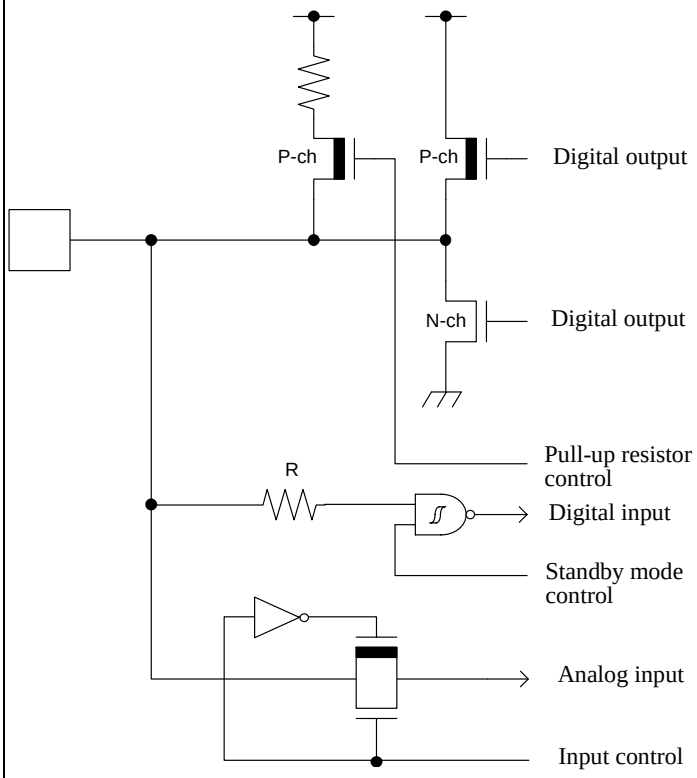
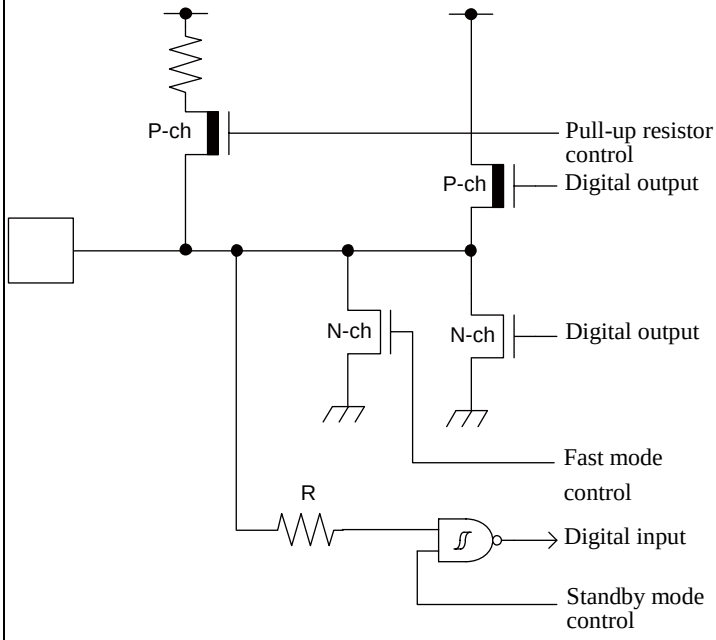
PFBGA-121

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
28	23	18	J2	P3E TIOA4_1 RTO04_0 (PPG04_0) MAD01_0	G	I
29	24	19	K2	P3F TIOA5_1 RTO05_0 (PPG04_0) MAD02_0	G	I
30	25	20	L1	VSS	-	-
31	26	-	K1	VCC	-	-
32	27	-	L2	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	K
33	28	-	J3	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1 AIN2_0	G	K
34	29	-	J5	P42 TIOA2_0 RTO12_1 (PPG12_1) MSDWEX_0 BIN2_0	G	I
35	30	-	H5	P43 ADTG_7 TIOA3_0 RTO13_1 (PPG12_1) MCSX8_0 ZIN2_0	G	I
36	31	21	K3	P44 TIOA4_0 RTO14_1 (PPG14_1) DA0	R	J
37	32	22	J4	P45 TIOB0_0 RTO15_1 (PPG14_1) DA1	R	J
38	33	23	L3	INITX	B	C

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	-	H5
	TIOA3_1		27	22	17	J1
	TIOA3_2		97	82	67	D7
	TIOB3_0	Base timer ch.3 TIOB pin	49	44	34	J8
	TIOB3_1		17	12	12	F2
	TIOB3_2		98	83	-	C7
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	21	K3
	TIOA4_1		28	23	18	J2
	TIOA4_2		51	-	-	H6
	TIOB4_0	Base timer ch.4 TIOB pin	50	45	35	K8
	TIOB4_1		18	13	-	F1
	TIOB4_2		52	-	-	H7
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	84	-	-	C9
	TIOA5_1		29	24	19	K2
	TIOA5_2		93	78	63	A9
	TIOB5_0	Base timer ch.5 TIOB pin	83	-	-	D8
	TIOB5_1		19	14	-	G1
	TIOB5_2		92	77	62	B9
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-	G7
	TIOA6_1		94	79	64	C8
	TIOA6_2		82	-	-	E7
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-	H8
	TIOB6_1		95	80	65	B8
	TIOB6_2		81	-	-	F7
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-	C4
	TIOA7_1		86	71	57	D11
	TIOA7_2		109	-	-	E5
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-	D4
	TIOB7_1		87	72	58	C10
	TIOB7_2		108	-	-	E6
Debugger	SWCLK	Serial wire debug interface clock input pin	105	90	71	B5
	SWDIO	Serial wire debug interface data input / output pin	103	88	69	C6
	SWO	Serial wire viewer output pin	102	87	68	B6
	TCK	JTAG test clock input pin	105	90	71	B5
	TDI	JTAG test data input pin	104	89	70	C5
	TDO	JTAG debug data output pin	102	87	68	B6
	TMS	JTAG test mode state input/output pin	103	88	69	C6
	TRACECLK	Trace CLK output pin of ETM	101	86	-	D6
	TRACED0	Trace data output pin of ETM	97	82	-	D7
	TRACED1		98	83	-	C7
	TRACED2		99	84	-	B7
	TRACED3		100	85	-	A7
	TRSTX	JTAG test reset Input pin	106	91	72	A5

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	C1
	INT00_1		95	80	65	B8
	INT00_2		108	-	-	E6
	INT01_0	External interrupt request 01 input pin	3	3	3	C2
	INT01_1		101	86	-	D6
	INT01_2		85	-	-	B10
	INT02_0	External interrupt request 02 input pin	6	6	6	D3
	INT02_1		62	52	41	J10
	INT02_2		82	-	-	E7
	INT03_0	External interrupt request 03 input pin	113	93	73	B4
	INT03_1		65	55	44	G10
	INT03_2		54	-	-	H8
	INT04_0	External interrupt request 04 input pin	17	12	12	F2
	INT04_1		114	94	74	C3
	INT04_2		10	-	-	F5
	INT05_0	External interrupt request 05 input pin	89	74	-	B11
	INT05_1		75	65	54	E11
	INT05_2		21	16	-	G3
	INT06_1	External interrupt request 06 input pin	88	73	59	C11
	INT06_2		22	17	-	G4
	INT07_1	External interrupt request 07 input pin	11	-	-	F6
	INT07_2		7	7	7	E2
	INT08_1	External interrupt request 08 input pin	19	14	-	G1
	INT08_2		8	8	8	E3
	INT09_1	External interrupt request 09 input pin	20	15	-	G2
	INT09_2		15	10	10	F4
	INT10_1	External interrupt request 10 input pin	16	11	11	F3
	INT10_2		112	-	-	C4
	INT11_1	External interrupt request 11 input pin	50	45	35	K8
	INT11_2		110	-	-	D5
	INT12_1	External interrupt request 12 input pin	32	27	-	L2
	INT12_2		96	81	66	A8
	INT13_1	External interrupt request 13 input pin	33	28	-	J3
	INT13_2		49	44	34	J8
	INT14_1	External interrupt request 14 input pin	68	58	47	F10
	INT14_2		53	-	-	G7
	INT15_1	External interrupt request 15 input pin	52	-	-	H7
	INT15_2		14	9	9	E1
External Interrupt	NMIX	Non-Maskable Interrupt input pin	116	96	76	B2

Type	Circuit	Remarks
F		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
G		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -12 mA, I_{OL} = 12 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
M		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -8 mA, I_{OL} = 8 mA
N		– CMOS level output – CMOS level hysteresis input – 5V tolerant – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA (GPIO) – I_{OL} = 20 mA (Fast Mode Plus) – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

12. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the L level.

- INITX=1

  This is the period when the INITX pin is the H level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation.

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixedat 0 / Analog input enabled	Hi-Z / Internal input fixedat 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

13.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7*4	5.5	V	
Power supply voltage (VBAT)		V_{BAT}	-	2.7	5.5	V	
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	AV_{CC}=V_{CC}
Analog reference voltage		AVRH	-	*3	AV_{CC}	V	
Smoothing capacitor		C_S	-	1	10	µF	for built-in regulator *1
Operating temperature	Junction temperature	T_J	-	- 40	+ 125	°C	
	Ambient temperature	T_A	-	- 40	*2	°C	

*1: See "C pin" in "Handling Devices" for the connection of the smoothing capacitor.

*2: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).
The calculation formula of the ambient temperature (T_A) is shown below.

$$T_A\ (Max) = T_J\ (Max) - Pd\ (Max) \times \theta ja$$

Pd: Power dissipation (W)
θja: Package thermal resistance (°C/W)

$$Pd\ (Max) = V_{CC} \times I_{CC}\ (Max) + \Sigma\ (I_{OL} \times V_{OL}) + \Sigma\ ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

*3 :The minimum value of Analog reference voltage depends on the value of compare clock cycle (Tcck).
See 12.5 12-bit A/D Converter for the details.

*4: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

Package thermal resistance and maximum permissible power for each package are shown below.

The operation is guaranteed maximum permissible power or less for semiconductor devices.

13.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		5 V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
H level output voltage	V_{OH}	4mA type	$V_{CC} \geq 4.5$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 4.5$ V, I_{OH} = - 2 mA					
		8mA type	$V_{CC} \geq 4.5$ V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 4.5$ V, I_{OH} = - 4 mA					
		12mA type	$V_{CC} \geq 4.5$ V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 4.5$ V, I_{OH} = - 8 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
			$V_{CC} < 4.5$ V, I_{OH} = - 3 mA					

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
		8 mA type	$V_{CC} \geq 4.5$ V, I_{OH} = 8 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OH} = 4 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OH} = 4 mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5$ V, I_{OH} = 3 mA					
			$V_{CC} \leq 5.5$ V, I_{OH} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

SDRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Output frequency	t_{CYCSD}	MSDCLK	-	32	MHz
Address delay time	t_{AOSD}	MSDCLK, MAD[15:0]	2	12	ns
MSDCLK↑→Data output delay time	t_{DOSD}	MSDCLK, MADATA[31:0]	2	12	ns
MSDCLK↑→Data output Hi-Z time	t_{DOZSD}	MSDCLK, MADATA[31:0]	2	20	ns
MDQM[1:0] delay time	t_{WROSD}	MSDCLK, MDQM[1:0]	1	12	ns
MCSX delay time	t_{MCSSD}	MSDCLK, MCSX8	2	12	ns
MRASX delay time	t_{RASSD}	MSDCLK, MRASX	2	12	ns
MCASX delay time	t_{CASSD}	MSDCLK, MCASX	2	12	ns
MSDWEX delay time	t_{MWESD}	MSDCLK, MSDWEX	2	12	ns
MSDCKE delay time	t_{CKESD}	MSDCLK, MSDCKE	2	12	ns
Data set up time	t_{DSSD}	MSDCLK, MADATA[31:0]	23	-	ns
Data hold time	t_{DHSD}	MSDCLK, MADATA[31:0]	0	-	ns

Note:

- *When the external load capacitance C_L = 30 pF*

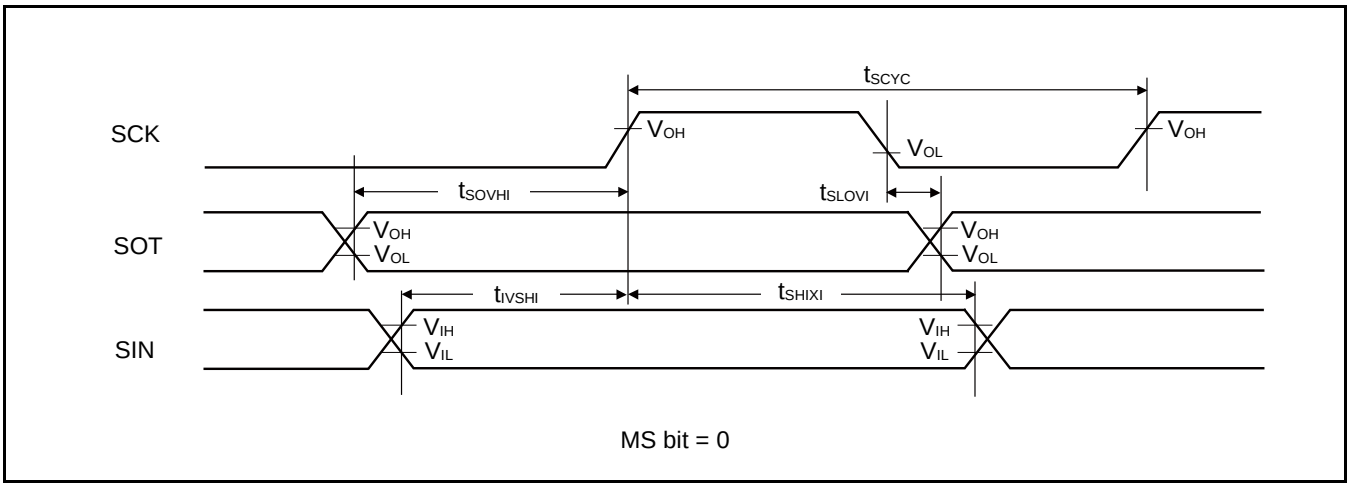
Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

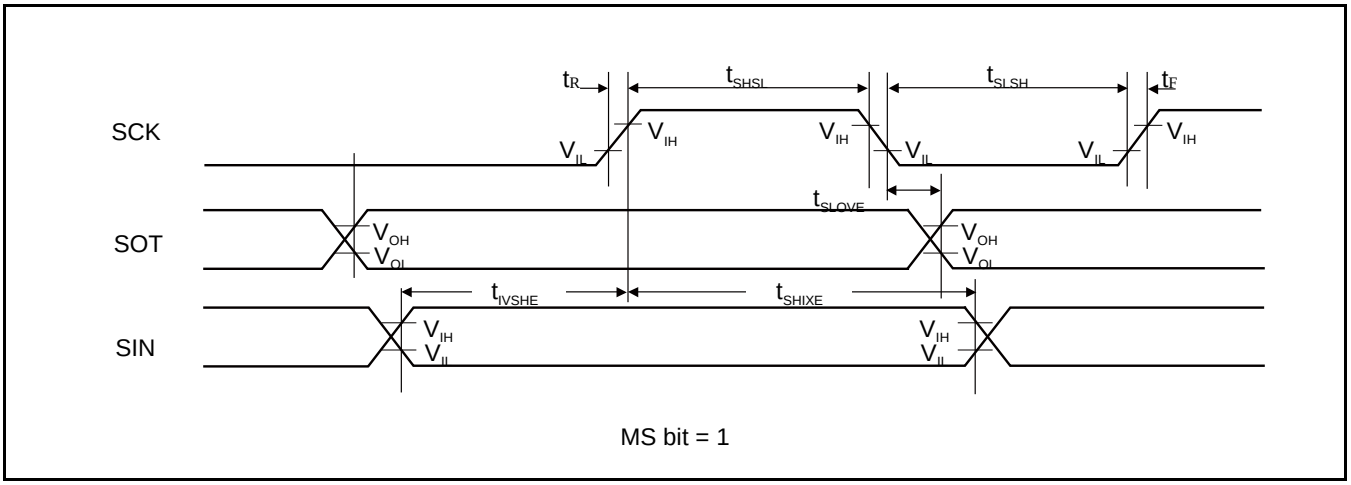
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*

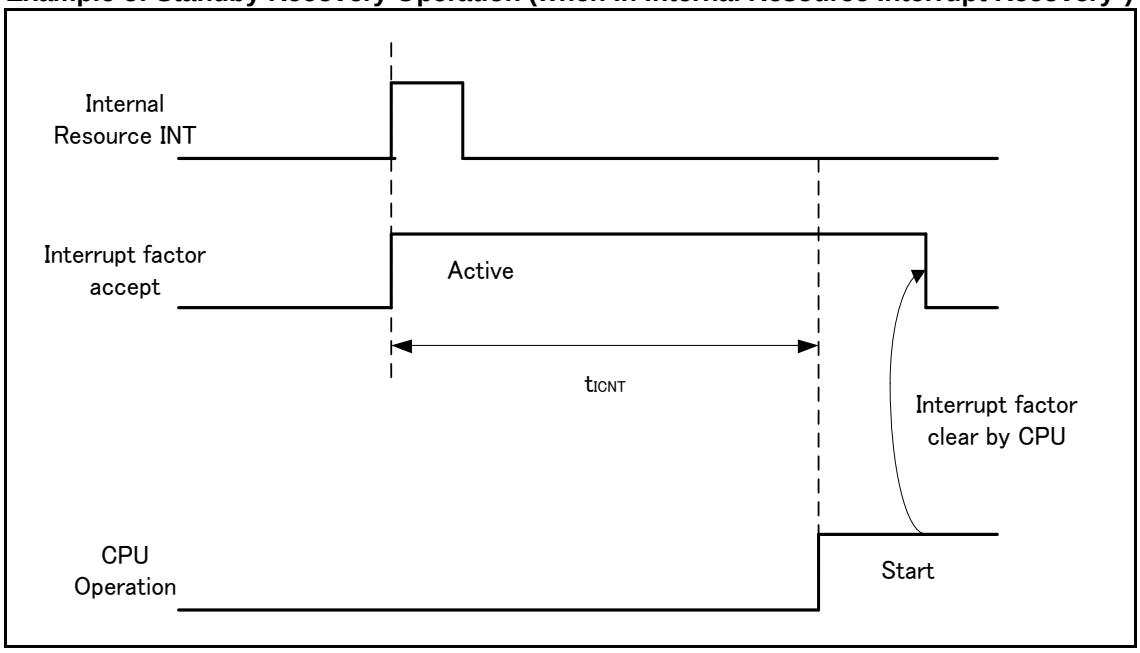


MS bit = 0



MS bit = 1

Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery*)

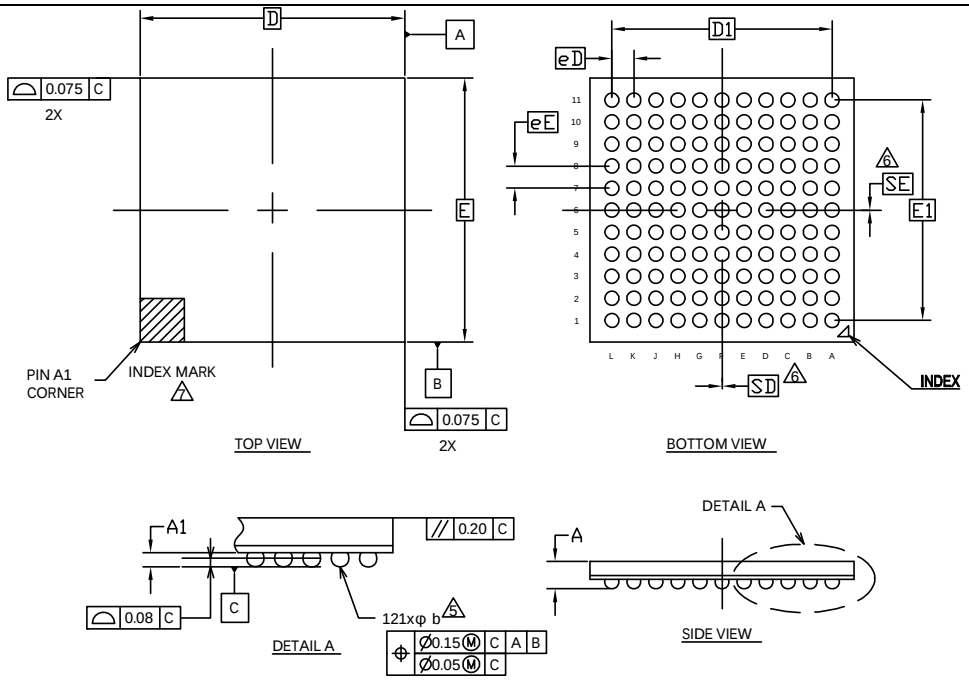


*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main part (002-04856).
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM4 Family Peripheral Manual Main part (002-04856).*

Package Type	Package Code
FBGA 121	FDI121



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
D1		5.00 BSC	
E1		5.00 BSC	
MD		11	
ME		11	
N		121	
∅ b	0.27	0.32	0.37
eD		0.50 BSC	
eE		0.50 BSC	
SD		0.00	
SE		0.00	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATIO N PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

PACKAGE OUTLINE, 121 BALL FBGA
6.0X6.0X1.2 MM FDI121 REV**

002-13227 **

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*E	5639294	NOSU	02/22/2017	Updated Circuit of “type N” in 7 I/O Circuit Type. Added the Baud rate spec in 13.4.11 CSIO Timing (Page 102, 104, 106, 108) Corrected MPNs as below to 14. Ordering Information. S6E2H14G0AGB30000 → S6E2H14G0AGB3000A S6E2H16G0AGB30000 → S6E2H16G0AGB3000A S6E2H44G0AGB30000 → S6E2H44G0AGB3000A S6E2H46G0AGB30000 → S6E2H46G0AGB3000A S6E2HE4G0AGB30000 → S6E2HE4G0AGB3000A S6E2HE6F0AGV20000 → S6E2HE6F0AGV2000A S6E2HE6G0AGB30000 → S6E2HE6G0AGB3000A S6E2HG4G0AGB30000 → S6E2HG4G0AGB3000A S6E2HG6G0AGB30000 → S6E2HG6G0AGB3000A Updated figures in 15. Package Dimensions.