Infineon Technologies - S6E2HG6F0AGV20000 Datasheet

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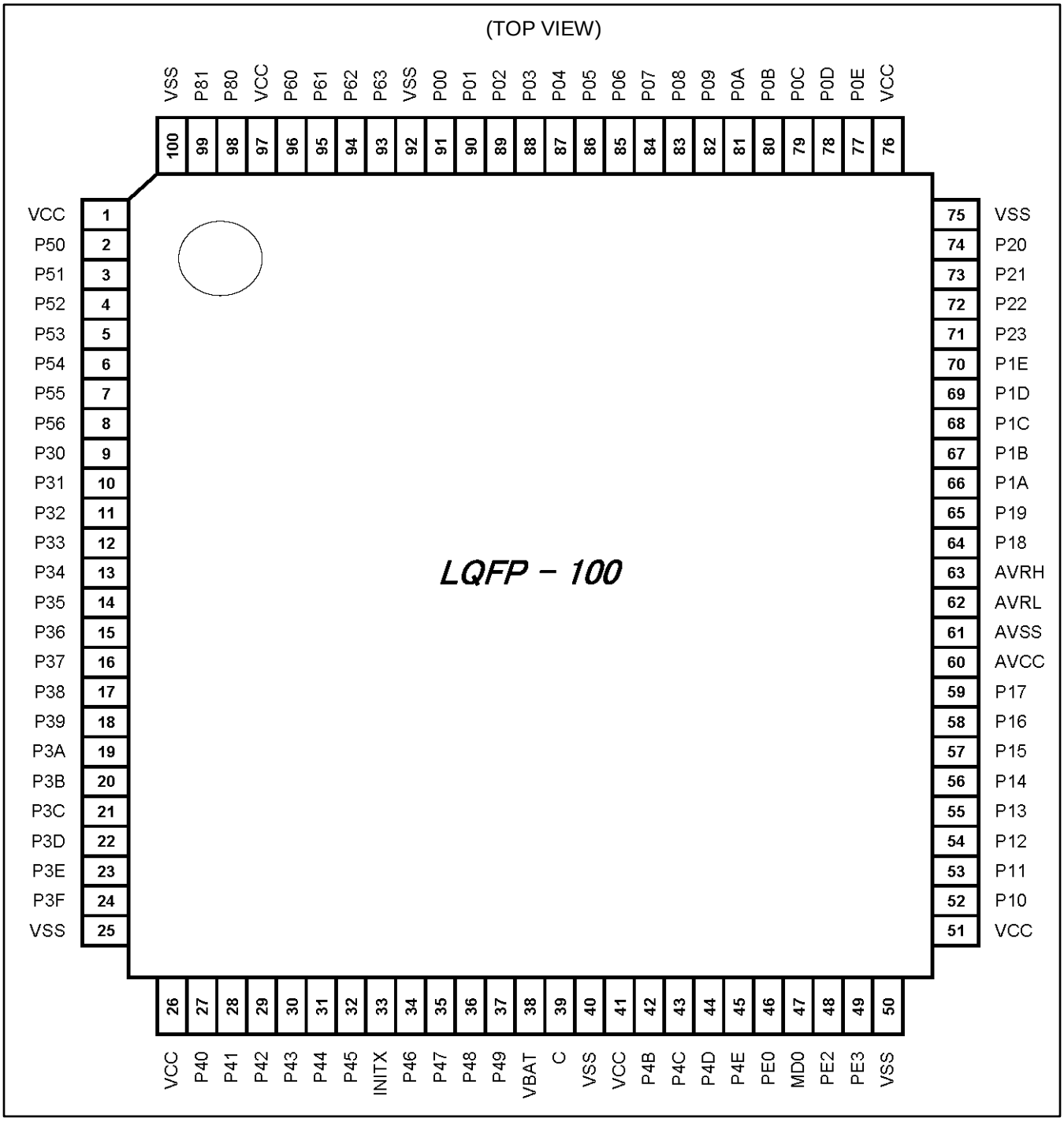
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2hg6f0agv20000

LQI100


(TOP VIEW)
LQFP – 100
1 VCC
2 P50
3 P51
4 P52
5 P53
6 P54
7 P55
8 P56
9 P30
10 P31
11 P32
12 P33
13 P34
14 P35
15 P36
16 P37
17 P38
18 P39
19 P3A
20 P3B
21 P3C
22 P3D
23 P3E
24 P3F
25 VSS
26 VCC
27 P40
28 P41
29 P42
30 P43
31 P44
32 P45
33 INITX
34 P46
35 P47
36 P48
37 P49
38 VBAT
39 C
40 VSS
41 VCC
42 P4B
43 P4C
44 P4D
45 P4E
46 PE0
47 MD0
48 PE2
49 PE3
50 VSS
51 VCC
52 P10
53 P11
54 P12
55 P13
56 P14
57 P15
58 P16
59 P17
60 AVCC
61 AVSS
62 AVRL
63 AVRH
64 P18
65 P19
66 P1A
67 P1B
68 P1C
69 P1D
70 P1E
71 P23
72 P22
73 P21
74 P20
75 VSS
76 VCC
77 P0E
78 P0D
79 P0C
80 P0B
81 P0A
82 P09
83 P08
84 P07
85 P06
86 P05
87 P04
88 P03
89 P02
90 P01
91 P00
92 VSS
93 P63
94 P62
95 P61
96 P60
97 VCC
98 P80
99 P81
100 VSS

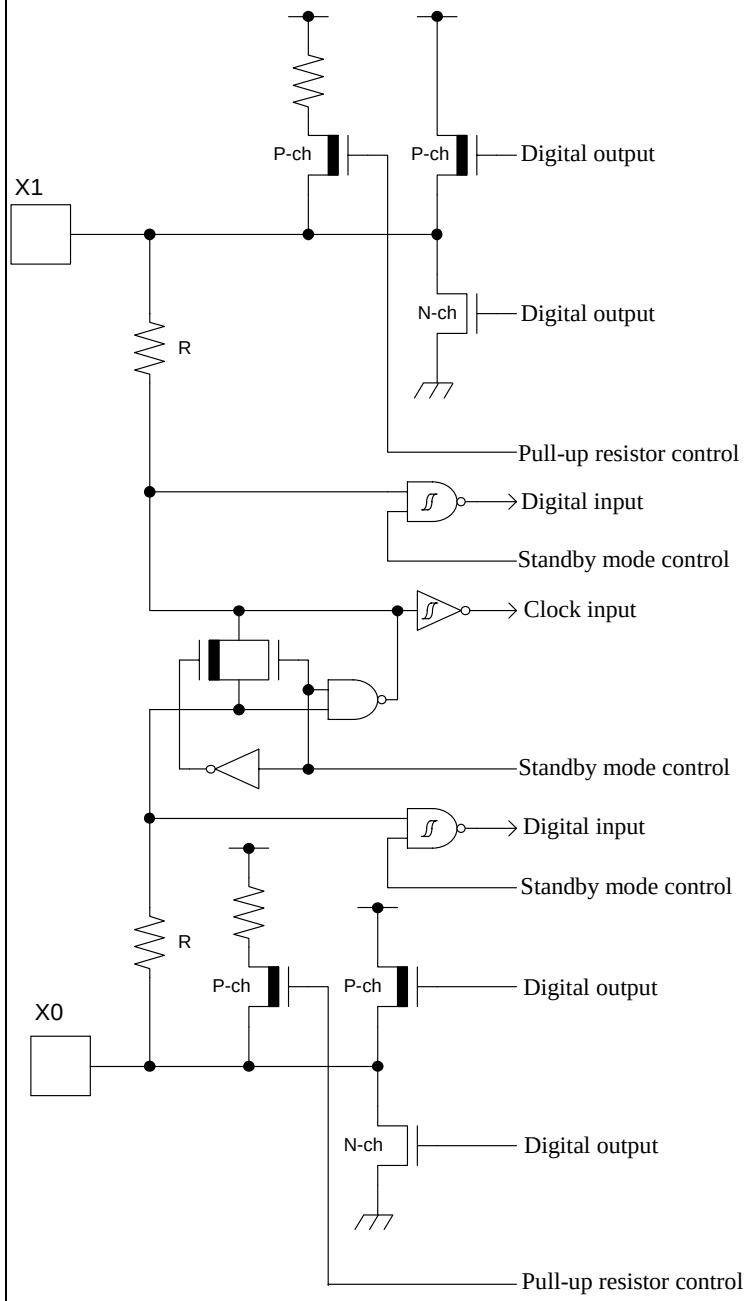
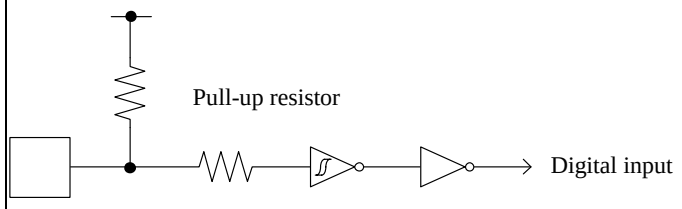
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
82	-	-	E7	P27	E	K
				TIOA6_2		
				RTO04_1 (PPG04_1)		
				INT02_2		
83	-	-	D8	P26	E	I
				TIOB5_0		
				SCK2_1 (SCL2_1)		
				RTO03_1 (PPG02_1)		
84	-	-	C9	P25	E	I
				TIOA5_0		
				SOT2_1 (SDA2_1)		
				RTO02_1 (PPG02_1)		
				TX1_0		
85	-	-	B10	P24	E	K
				SIN2_1		
				RTO01_1 (PPG00_1)		
				INT01_2		
				RX1_0		
86	71	57	D11	P23	F	L
				AN15		
				TIOA7_1		
				SCK0_0 (SCL0_0)		
				RTO00_1 (PPG00_1)		
		-		MAD22_0		
87	72	58	C10	P22	F	L
				CROUT_0		
				AN16		
				TIOB7_1		
				SOT0_0 (SDA0_0)		
		-		ZIN1_1		
		58		RTO23_0		
88	73	59	C11	P21	F	M
				AN17		
				SIN0_0		
		-		BIN1_1		
		59		INT06_1		
		-		MAD23_0		
		59		RTO24_0		

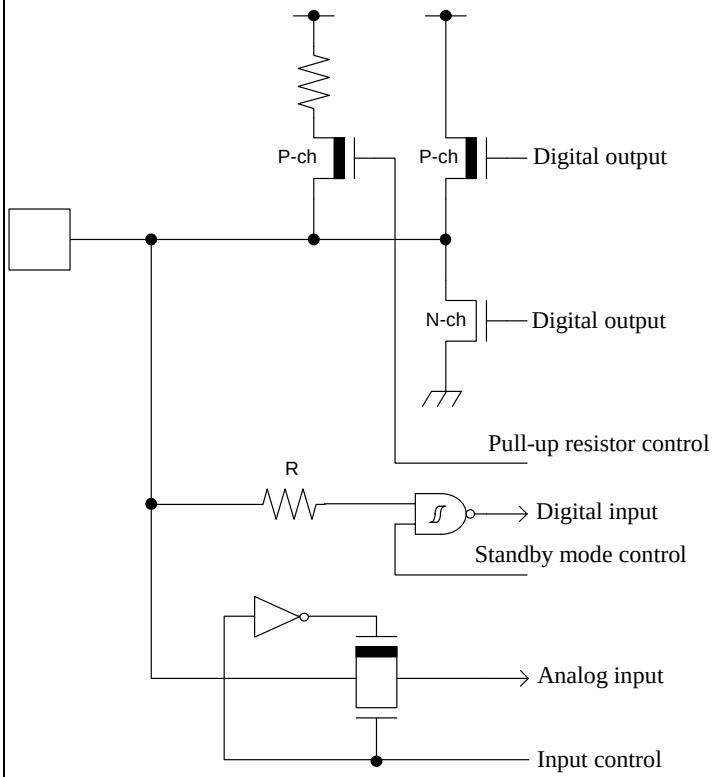
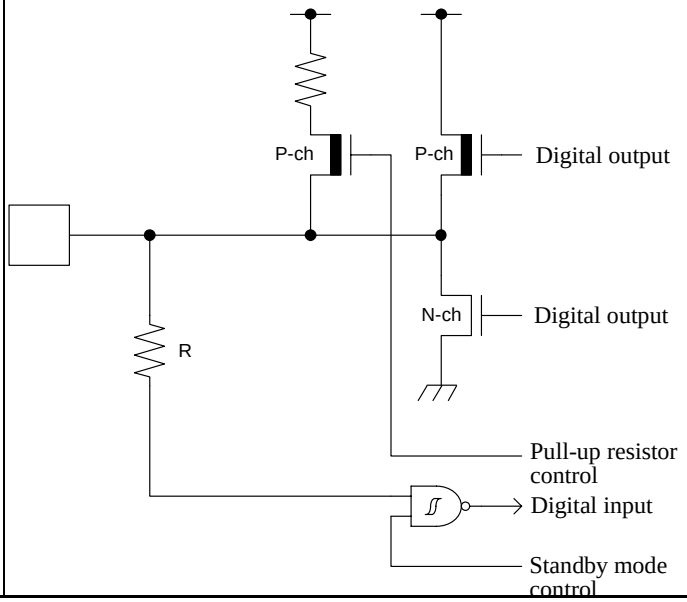
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
89	74	-	B11	P20	F	M
				AN18		
				AIN1_1		
				INT05_0		
				MAD24_0		
				RTO25_0		
90	75	60	A11	VSS	-	-
91	76	61	A10	VCC	-	-
92	77	62	B9	P0E	L	I
				TIOB5_2		
				SCS6_1		
				IC13_0		
				S_CLK_0		
				MDQM1_0		
93	78	63	A9	P0D	L	I
				TIOA5_2		
				SCK6_1 (SCL6_1)		
				IC12_0		
				S_CMD_0		
				MDQM0_0		
94	79	64	C8	P0C	L	I
				TIOA6_1		
				SOT6_1 (SDA6_1)		
				IC11_0		
				S_DATA1_0		
				MALE_0		
95	80	65	B8	P0B	L	K
				TIOB6_1		
				SIN6_1		
				IC10_0		
				INT00_1		
				S_DATA0_0		
				MCSX0_0		
96	81	66	A8	P0A	L	K
				SIN1_0		
				FRCK1_0		
				INT12_2		
				S_DATA3_0		
				MCSX1_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
97	82	67	D7	P09	M	N
				AN19		
		-		TRACED0		
		67		TIOA3_2		
				SOT1_0 (SDA1_0)		
				S_DATA2_0		
				MCSX5_0		
				IC23_1		
98	83	-	C7	P08	F	N
				AN20		
				TRACED1		
				TIOB3_2		
				SCK1_0 (SCL1_0)		
				MCSX4_0		
				IC22_1		
99	84	-	B7	P07	M	N
				AN21		
				TRACED2		
				TIOA0_2		
				SCK7_0 (SCL7_0)		
				MCLKOUT_0		
				IC21_1		
100	85	-	A7	P06	F	N
				AN22		
				TRACED3		
				TIOB0_2		
				SOT7_0 (SDA7_0)		
				MCSX3_0		
				IC20_1		
101	86	-	D6	P05	F	O
				AN23		
				ADTG_0		
				TRACECLK		
				SIN7_0		
				INT01_1		
				MCSX2_0		
				FRCK2_1		
102	87	68	B6	P04	E	G
				TDO		
				SWO		
103	88	69	C6	P03	E	G
				TMS		
				SWDIO		

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Bus	MCSX0_0	External bus interface chip select output pin	95	80	65	B8
	MCSX1_0		96	81	66	A8
	MCSX2_0		101	86	-	D6
	MCSX3_0		100	85	-	A7
	MCSX4_0		98	83	-	C7
	MCSX5_0		97	82	67	D7
	MCSX6_0		104	89	70	C5
	MCSX7_0		106	91	72	A5
	MCSX8_0		35	30	-	H5
	MADATA00_0	External bus interface data bus (Address / data multiplex bus)	2	2	2	C1
	MADATA01_0		3	3	3	C2
	MADATA02_0		4	4	4	D1
	MADATA03_0		5	5	5	D2
	MADATA04_0		6	6	6	D3
	MADATA05_0		7	7	7	E2
	MADATA06_0		8	8	8	E3
	MADATA07_0		9	9	9	E4
	MADATA08_0		10	10	10	F5
	MADATA09_0		11	11	11	F6
	MADATA10_0		12	12	12	G5
	MADATA11_0		13	13	-	G6
	MADATA12_0		14	14	-	E1
	MADATA13_0		15	15	-	F4
	MADATA14_0		16	16	-	F3
	MADATA15_0		17	17	-	F2
	MDQM0_0	External bus interface byte mask signal output pin	93	78	63	A9
	MDQM1_0		92	77	62	B9
	MALE_0	External bus interface Address Latch enable output signal for multiplex	94	79	64	C8
	MRDY_0	External bus interface external RDY input signal	116	96	76	B2
	MCLKOUT_0	External bus interface external clock output pin	99	84	-	B7
	MNALE_0	External bus interface ALE signal to control NAND Flash output pin	18	-	-	F1
	MNCLE_0	External bus interface CLE signal to control NAND Flash output pin	19	-	-	G1
	MNREX_0	External bus interface read enable signal to control NAND Flash	21	-	-	G3
	MNWEX_0	External bus interface write enable signal to control NAND Flash	20	-	-	G2
	MOEX_0	External bus interface read enable signal for SRAM	114	94	74	C3
	MWEX_0	External bus interface write enable signal for SRAM	113	93	73	B4
External Bus	MSDCLK_0	SDRAM interface SDRAM clock output pin	23	18	-	H1
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	24	19	-	H2
	MRASX_0	SDRAM interface SDRAM row address strobe pin	25	20	-	H3
	MCASX_0	SDRAM interface SDRAM column address strobe pin	26	21	-	H4
	MSDWEX_0	SDRAM interface SDRAM write enable pin	34	29	-	J5

7. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. – Oscillation feedback resistor : Approximately 1MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA
B		– CMOS level hysteresis input – Pull-up resistor : Approximately 50 kΩ

Type	Circuit	Remarks
F		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
G		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -12 mA, I_{OL} = 12 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

12. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the L level.

- INITX=1

  This is the period when the INITX pin is the H level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θja (°C/W)	Maximum Permissible Power (mW)	
			T_A=+85°C	T_A=+105°C
LQH080 (0.5mm pitch)	Single-layered both sides	82	488	244
	4 layers	56	714	357
LQI100 (0.5mm pitch)	Single-layered both sides	59	678	339
	4 layers	39	1026	513
LQM120 (0.5mm pitch)	Single-layered both sides	71	563	282
	4 layers	50	800	400
FDI121 (0.5mm pitch)	Single-layered both sides	63	635	317
	4 layers	37	1081	540

WARNING:

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
  Any use of semiconductor devices will be under their recommended operating condition.
  Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
  No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

13.4.7 Power-on Reset Timing

(V_{SS} = 0V)

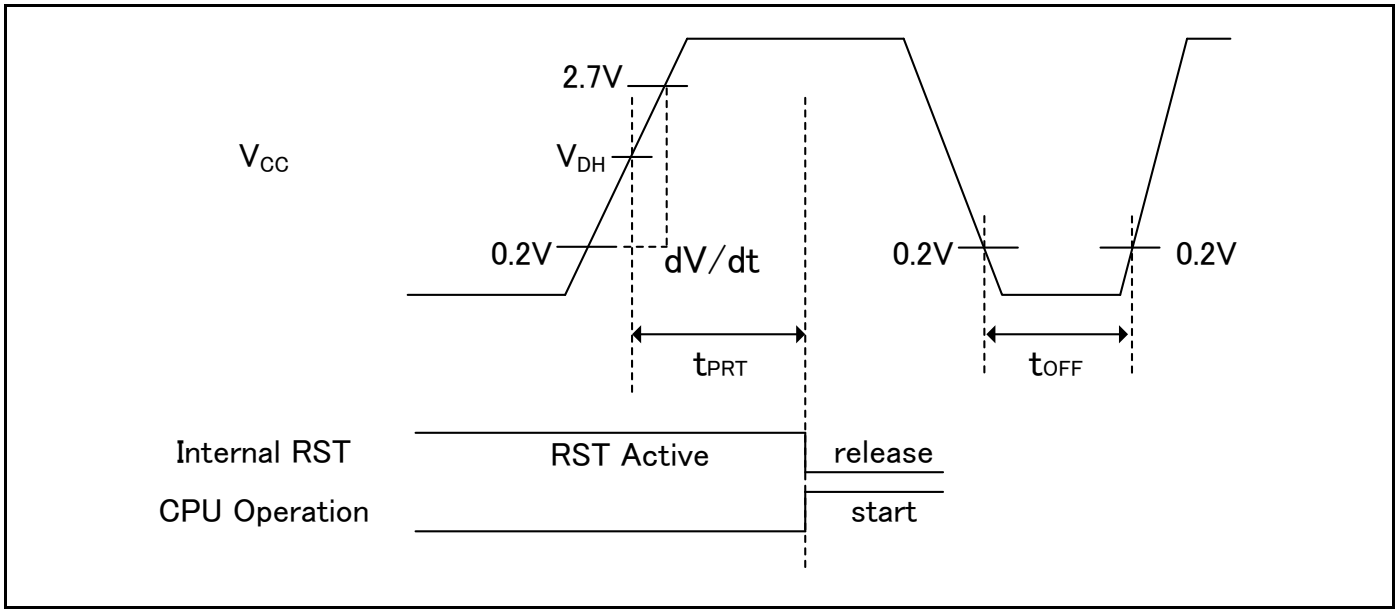
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	50	-	-	ms	*1
Power ramp rate	dV/dt		V_{CC}: 0.2V to 2.70V	1.3	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.33	-	0.60	ms	

*1: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>50ms).

Note:

- *t_{OFF} must be satisfied. When t_{OFF} cannot be satisfied, assert external reset (INITX) at power-up and at any brownout event.*



Glossary

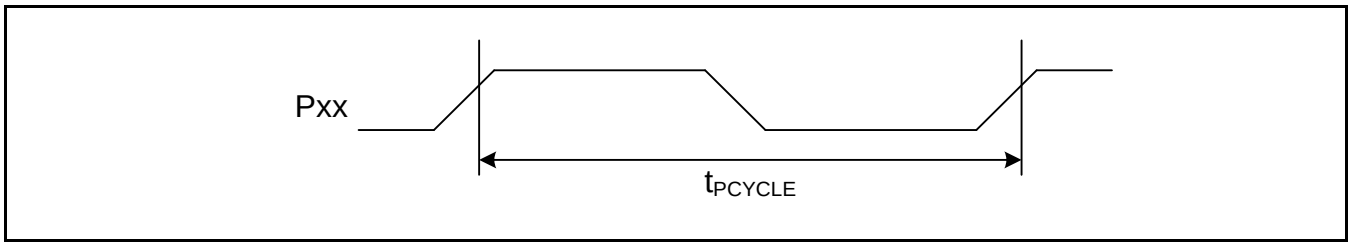
- VDH: detection voltage of Low-Voltage detection reset. See 13.7 Low-Voltage Detection Characteristics.

13.4.8 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{PCYCLE}	Pxx*	$V_{CC} \geq 4.5$ V	-	50	MHz
			$V_{CC} < 4.5$ V	-	32	MHz

*: GPIO is a target.



Separate Bus Access Asynchronous SRAM Mode

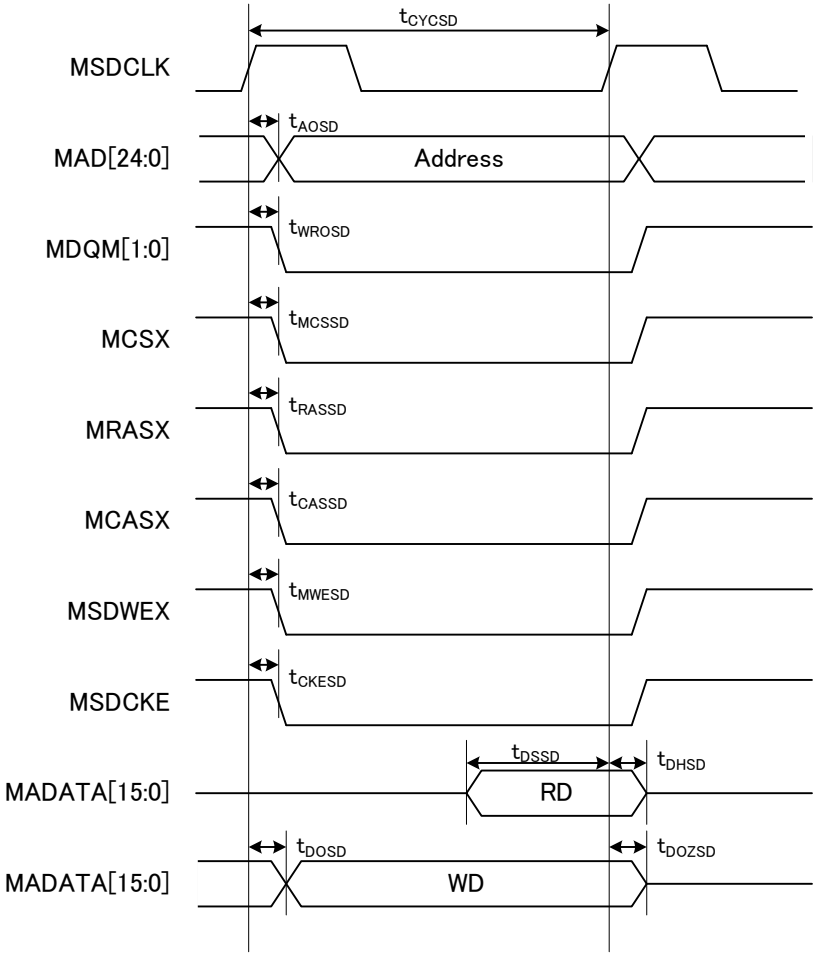
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
MOEX Minimum pulse width	t_{OEW}	MOEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MCSX↓→Address output delay time	t_{CSL-AV}	MCSX[7:0], MAD[24:0]	$V_{CC} \geq 4.5$ V	-9	+9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MOEX↑→Address hold time	t_{OEH-AX}	MOEX, MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX↓→ MOEX↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MOEX↑→ MCSX↑ time	$t_{OEH-CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX↓→MDQM↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
Data set up→MOEX↑ time	t_{DS-OE}	MOEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MOEX↑→ Data hold time	t_{DH-OE}	MOEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MWEX Minimum pulse width	t_{WEW}	MWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MWEX↑→Address output delay time	t_{WEH-AX}	MWEX, MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX↓→MWEX↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MWEX↑→MCSX↑ delay time	$t_{WEH-CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX↓→MDQM↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MWEX↓→ Data output time	t_{CSL-DX}	MCSX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	MCLK-9	MCLK+9	ns
			$V_{CC} < 4.5$ V	MCLK-12	MCLK+12	
MWEX↑→ Data hold time	t_{WEH-DX}	MWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*

SDRAM Access



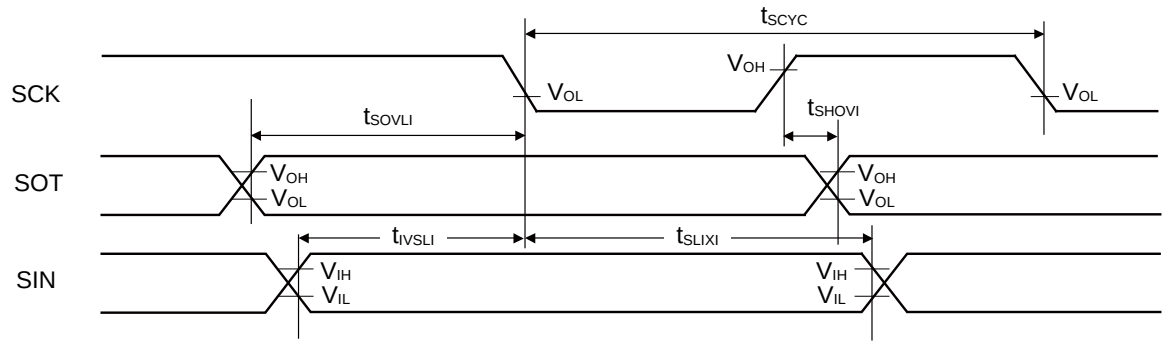
Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

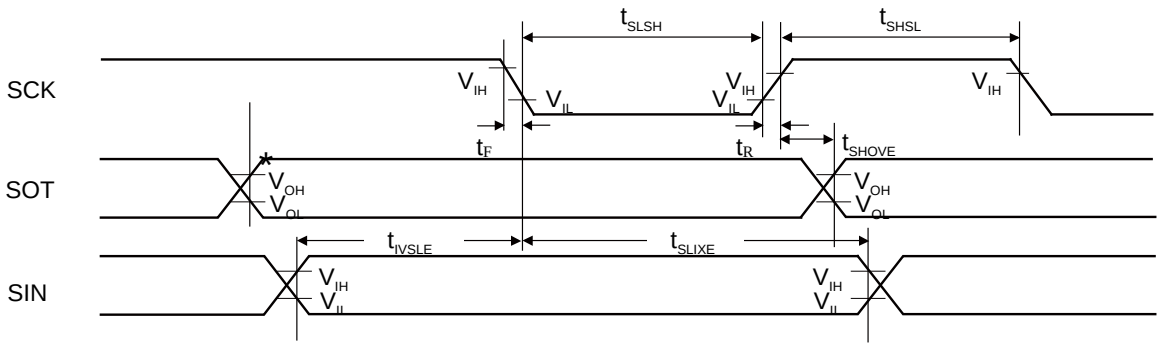
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud Rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

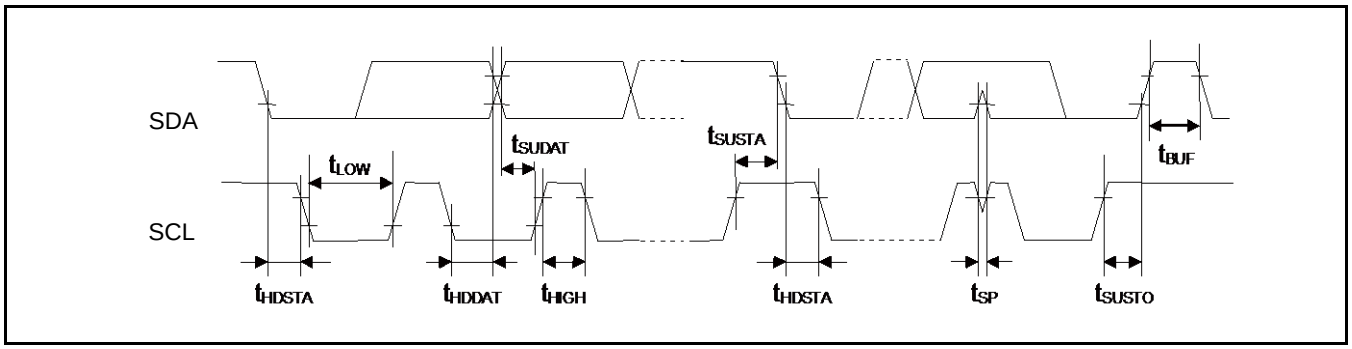
High-speed Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

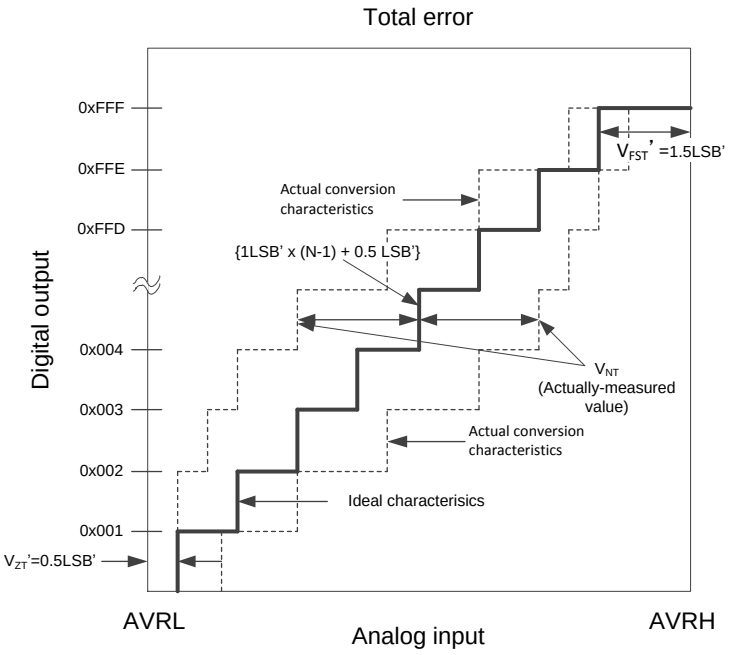
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
- *No chip select: SIN4_1, SOT4_1, SCK4_1*
- *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

■ Total error: A difference between actual value and theoretical value.
The overall error includes zero-transition voltage, full-scale transition voltage and linearity error.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'}\ \text{X}\ (N-1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}\ [\text{LSB}]$$

$$1\ \text{LSB'}\ (\text{ideal value}) = \frac{\text{AVRH} - \text{AVRL}}{4096}\ [\text{V}]$$

V_{ZT}' (ideal value) = AVRL + 0.5 LSB' [V]

V_{FST}' (ideal value) = AVRH - 1.5 LSB' [V]

V_{NT}' : A voltage for causing transition of digital output from (N-1) to N

13.6 12-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	tc20		0.56	0.69	0.81	µs	Load 20 pF
	tc100		2.79	3.42	4.06	µs	Load 100 pF
Integral Nonlinearity*	INL		- 16	-	+ 16	LSB	
Differential Nonlinearity*	DNL		- 0.98	-	+ 1.5	LSB	
Output voltage offset	V_{OFF}		-	-	10.0	mV	When setting 0x000
			- 20.0	-	+ 1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current*	IDDA	AVCC	260	330	410	µA	D/A 1unit operation AV_{CC}=3.3 V
			400	510	620	µA	D/A 1unit operation AV_{CC}=5.0 V
	IDSA		-	-	14	µA	When D/A stop

*: During no load

13.7 Low-Voltage Detection Characteristics

13.7.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

13.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	4480× t_{CYCP}*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.