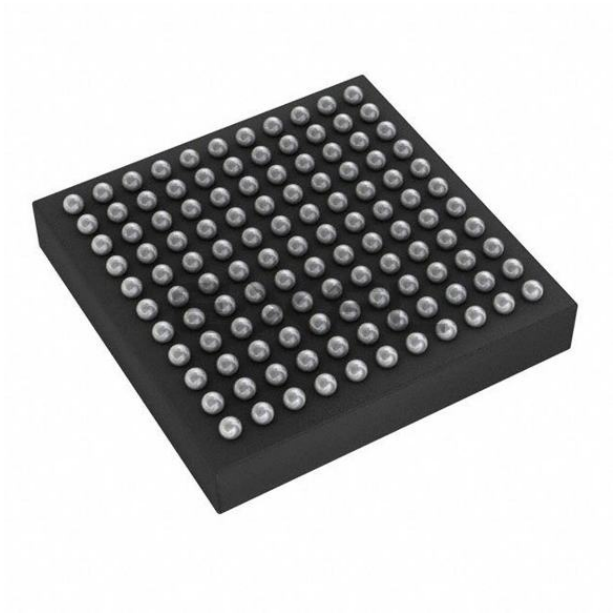

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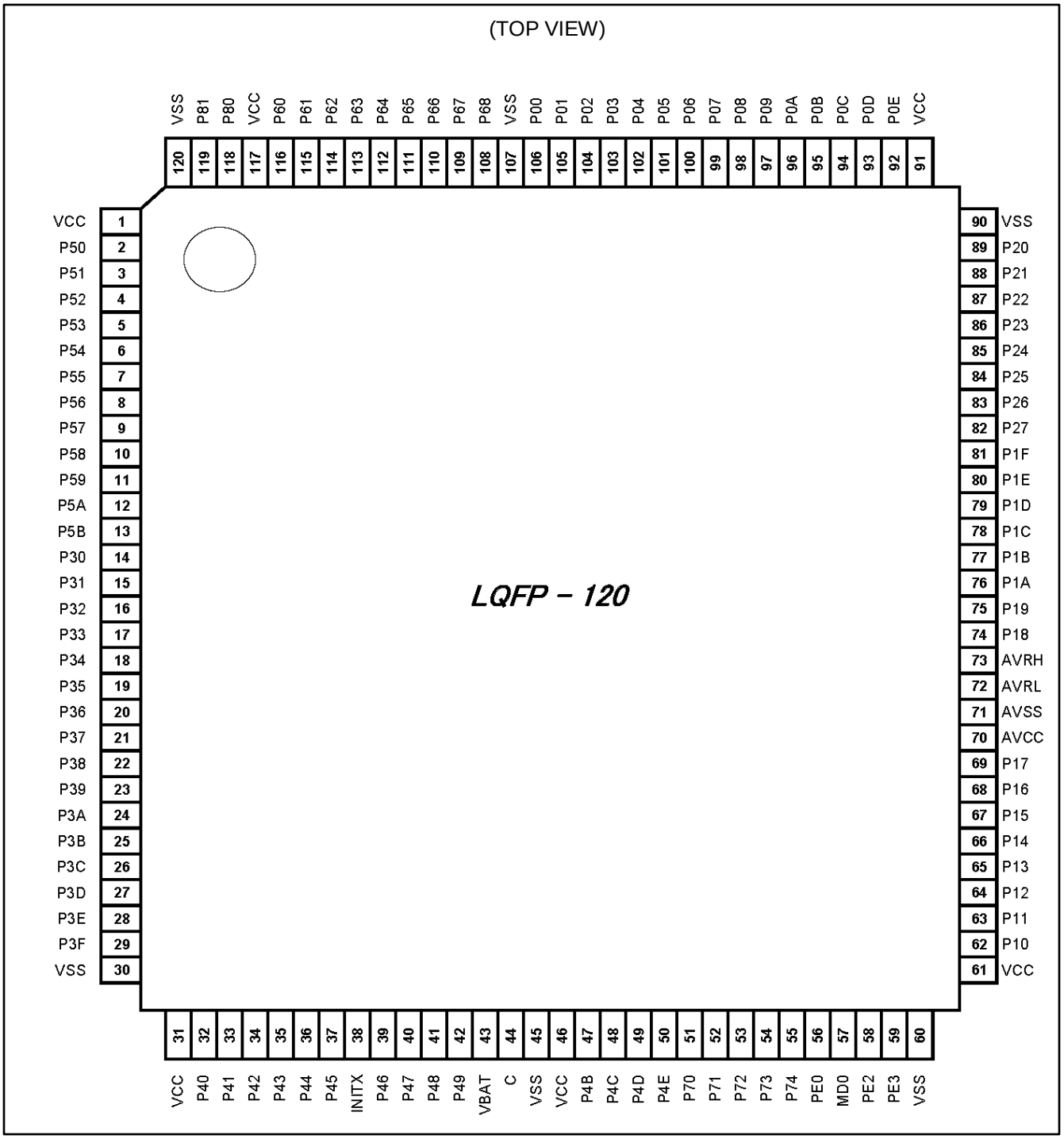
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2hg6g0agb3000a

LQM120


(TOP VIEW)
LQFP – 120
1 VCC
2 P50
3 P51
4 P52
5 P53
6 P54
7 P55
8 P56
9 P57
10 P58
11 P59
12 P5A
13 P5B
14 P30
15 P31
16 P32
17 P33
18 P34
19 P35
20 P36
21 P37
22 P38
23 P39
24 P3A
25 P3B
26 P3C
27 P3D
28 P3E
29 P3F
30 VSS
31 VCC
32 P40
33 P41
34 P42
35 P43
36 P44
37 P45
38 INITX
39 P46
40 P47
41 P48
42 P49
43 VBAT
44 C
45 VSS
46 VCC
47 P4B
48 P4C
49 P4D
50 P4E
51 P70
52 P71
53 P72
54 P73
55 P74
56 PE0
57 MD0
58 PE2
59 PE3
60 VSS
61 VCC
62 P10
63 P11
64 P12
65 P13
66 P14
67 P15
68 P16
69 P17
70 AVCC
71 AVSS
72 AVRL
73 AVRH
74 P18
75 P19
76 P1A
77 P1B
78 P1C
79 P1D
80 P1E
81 P1F
82 P27
83 P26
84 P25
85 P24
86 P23
87 P22
88 P21
89 P20
90 VSS
91 VCC
92 P0E
93 P0D
94 P0C
95 P0B
96 P0A
97 P09
98 P08
99 P07
100 P06
101 P05
102 P04
103 P03
104 P02
105 P01
106 P00
107 VSS
108 P68
109 P67
110 P66
111 P65
112 P64
113 P63
114 P62
115 P61
116 P60
117 VCC
118 P80
119 P81
120 VSS

6. Pin Description

6.1 List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
1	1	1	B1	VCC	-	-
2	2	2	C1	P50 CTS4_0 AIN0_2 RTO10_0 (PPG10_0) INT00_0 MADATA00_0	E	K
3	3	3	C2	P51 RTS4_0 BIN0_2 RTO11_0 (PPG10_0) INT01_0 MADATA01_0	E	K
4	4	4	D1	P52 SCK4_0 (SCL4_0) ZIN0_2 RTO12_0 (PPG12_0) MADATA02_0	E	I
5	5	5	D2	P53 TIOA1_2 SOT4_0 (SDA4_0) RTO13_0 (PPG12_0) MADATA03_0	E	I
6	6	6	D3	P54 TIOB1_2 SIN4_0 RTO14_0 (PPG14_0) INT02_0 MADATA04_0	E	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
52	-	-	H7	P71 TIOB4_2 BIN0_1 IC12_1 INT15_1 RX0_0	E	K
53	-	-	G7	P72 TIOA6_0 SIN2_0 ZIN0_1 IC11_1 INT14_2	E	K
54	-	-	H8	P73 TIOB6_0 SOT2_0 (SDA2_0) IC10_1 INT03_2	E	K
55	-	-	J9	P74 SCK2_0 (SCL2_0) DTTI1X_1	E	I
56	46	36	L8	PE0 MD1	C	E
57	47	37	K9	MD0	J	D
58	48	38	L9	PE2 X0	A	A
59	49	39	L10	PE3 X1	A	B
60	50	40	L11	VSS	-	-
61	51	-	K11	VCC	-	-
62	52	41	J10	P10 AN00 SIN1_1 FRCK0_2 INT02_1 MAD07_0 RX1_2	F	M
63	53	42	H10	P11 AN01 SOT1_1 (SDA1_1) IC00_2 MAD08_0 TX1_2	F	L

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Multi-function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	53	-	-	G7
	SIN2_1		85	-	-	B10
	SIN2_2		68	58	47	F10
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I2C (operation mode 4).	54	-	-	H8
	SOT2_1 (SDA2_1)		84	-	-	C9
	SOT2_2 (SDA2_2)		69	59	48	F9
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I2C (operation mode 4).	55	-	-	J9
	SCK2_1 (SCL2_1)		83	-	-	D8
	SCK2_2 (SCL2_2)		74	64	53	F8
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	110	-	-	D5
	SIN3_1		15	10	10	F4
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I2C (operation mode 4).	109	-	-	E5
	SOT3_1 (SDA3_1)		16	11	11	F3
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I2C (operation mode 4).	108	-	-	E6
	SCK3_1 (SCL3_1)		17	12	12	F2
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	6	6	6	D3
	SIN4_1		75	65	54	E11
	SIN4_2		10	-	-	F5
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I2C (operation mode 4).	5	5	5	D2
	SOT4_1 (SDA4_1)		76	66	55	E10
	SOT4_2 (SDA4_2)		11	-	-	F6
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an I2C (operation mode 4).	4	4	4	D1
	SCK4_1 (SCL4_1)		77	67	56	E9
	SCK4_2 (SCL4_2)		12	-	-	G5
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	2	2	2	C1
	CTS4_1		78	68	-	E8
	CTS4_2		13	-	-	G6
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	3	3	3	C2
	RTS4_1		79	69	-	D10
	RTS4_2		14	9	9	E1

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
CAN0	TX0_0	CAN interface ch.0 TX output pin	51	-	-	H6
	TX0_1		18	13	-	F1
	TX0_2		114	94	74	C3
	RX0_0	CAN interface ch.0 RX input pin	52	-	-	H7
	RX0_1		19	14	-	G1
	RX0_2		113	93	73	B4
CAN1	TX1_0	CAN interface ch.1 TX output pin	84	-	-	C9
	TX1_1		12	-	-	G5
	TX1_2		63	53	42	H10
	RX1_0	CAN interface ch.1 RX input pin	85	-	-	B10
	RX1_1		11	-	-	F6
	RX1_2		62	52	41	J10
Reset	INITX	External Reset Input pin. A reset is valid when INITX=L.	38	33	23	L3
Mode	MD1	Mode 1 pin. During serial programming to Flash memory, MD1=L must be input.	56	46	36	L8
	MD0	Mode 0 pin. During normal operation, MD0=L must be input. During serial programming to Flash memory, MD0=H must be input.	57	47	37	K9
Power	VCC	Power supply Pin	1	1	1	B1
			31	26	-	K1
			46	41	31	K7
			61	51	-	K11
			91	76	61	A10
			117	97	77	A4
GND	VSS	GND Pin	107	92	-	A6
			30	25	20	L1
			45	40	30	L7
			60	50	40	L11
			90	75	60	A11
			120	100	80	A1
			-	-	-	K10
Clock	X0	Main clock (oscillation) input pin	58	48	38	L9
	X1	Main clock (oscillation) I/O pin	59	49	39	L10
	X0A	Sub clock (oscillation) input pin	39	34	24	L4
	X1A	Sub clock (oscillation) I/O pin	40	35	25	K4
	CROUT_0	Built-in high-speed CR-osc clock output port	87	72	58	C10
	CROUT_1		113	93	73	B4
ADC Power	AVCC	A/D converter and D/A converter analog power supply pin	70	60	49	J11
	AVRL	A/D converter analog reference voltage input pin	72	62	51	G11
	AVRH	A/D converter analog reference voltage input pin	73	63	52	F11
VBAT Power	VBAT	VBAT power supply pin. Backup power supply (battery etc.) and system power supply.	43	38	28	L5
ADC GND	AVSS	A/D converter and D/A converter GND pin	71	61	50	H11
C pin	C	Power supply stabilization capacity pin	44	39	29	L6

Note:

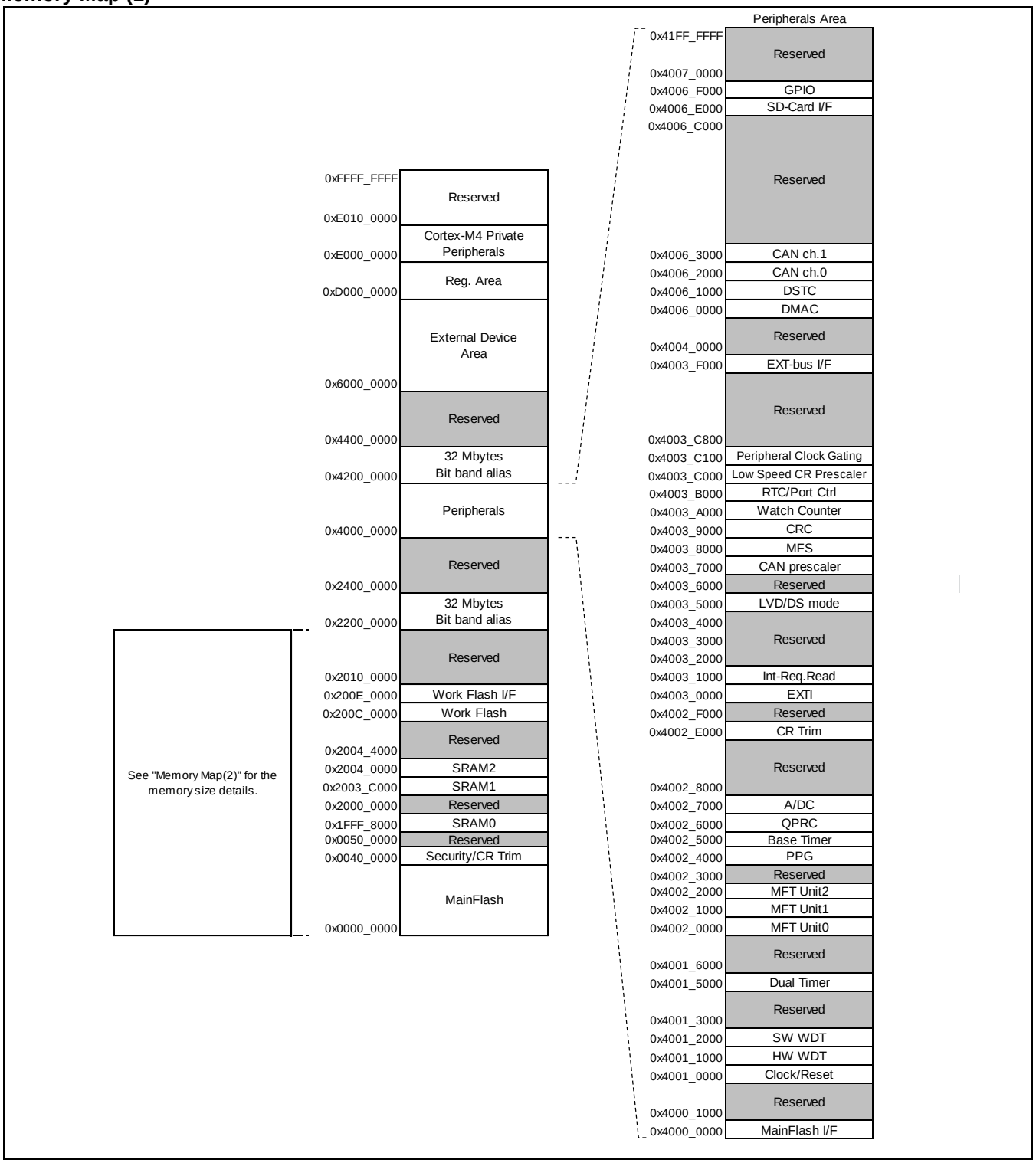
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

10. Memory Size

See Memory size in 2. Product Lineup to confirm the memory size.

11. Memory Map

Memory Map (1)



Current Explanation Diagram

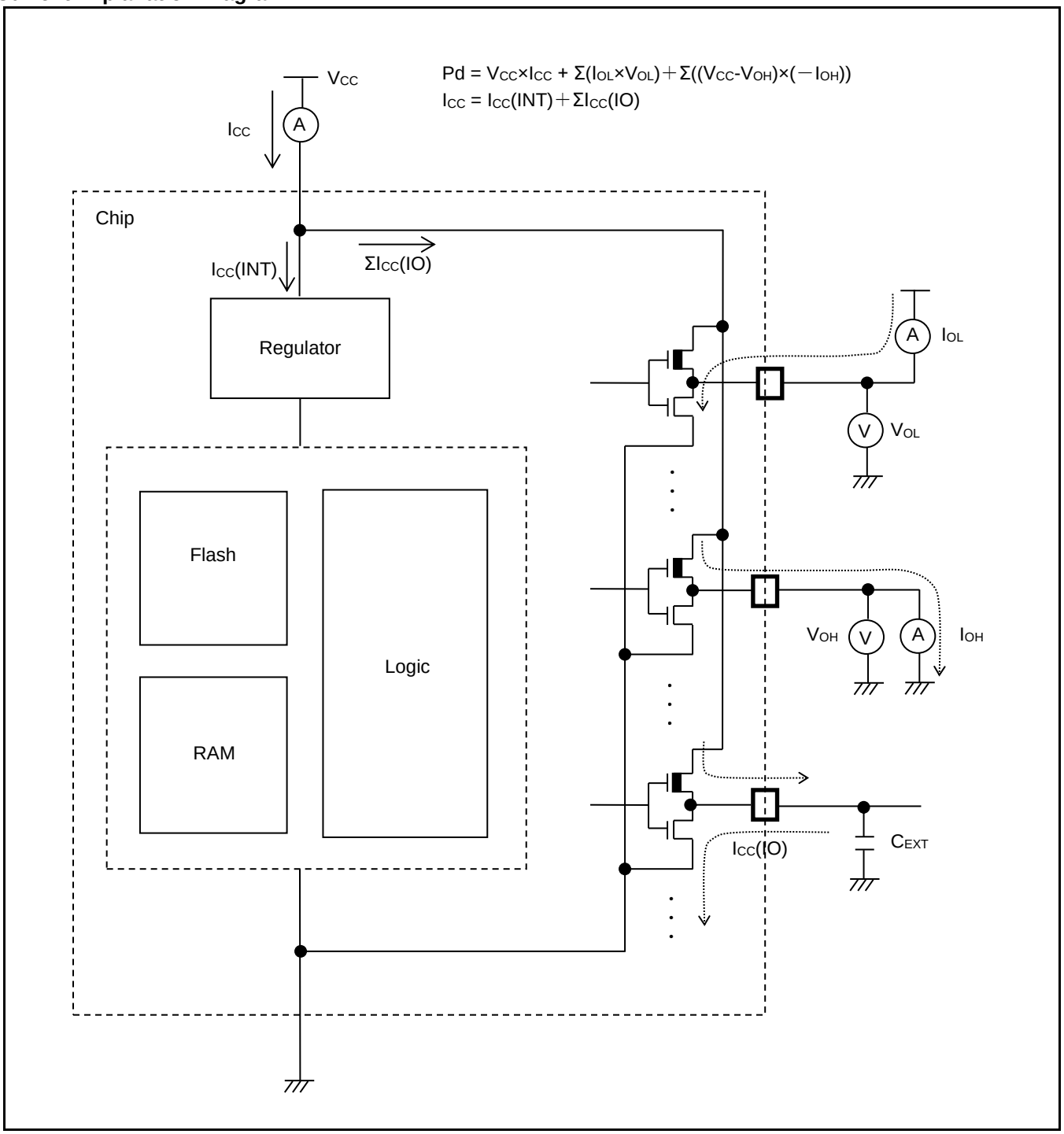


Table 12-4 Typical and Maximum Current Consumption in Normal Operation(other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 wait-cycle Mode and Read Access 0 wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (main oscillation)	*5*6	4 MHz	4.0	24	mA	*3 When all peripheral clocks are ON
						3.2	24	mA	*3 When all peripheral clocks are OFF
			Normal operation (built-in high-speed CR)	*5	4 MHz	3.2	24	mA	*3 When all peripheral clocks are ON
						2.7	23	mA	*3 When all peripheral clocks are OFF
			Normal operation (sub oscillation)	*5	32 kHz	0.34	21	mA	*3 When all peripheral clocks are ON
						0.30	21	mA	*3 When all peripheral clocks are OFF
			Normal operation (built-in low-speed CR)	*5	100 kHz	0.36	21	mA	*3 When all peripheral clocks are ON
						0.33	21	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, VC_C=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0"

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 000)

*6: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-9 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCHD}	VCC	Deep standby Stop mode (When RAM is OFF)	-	24	40	µA	*3, *4 T_A=+25°C
					-	640	µA	*3, *4 T_A=+85°C
					-	813	µA	*3, *4 T_A=+105°C
			Deep standby Stop mode (When RAM is ON)		41	146	µA	*3, *4 T_A=+25°C
					-	1616	µA	*3, *4 T_A=+85°C
					-	2059	µA	*3, *4 T_A=+105°C
	I_{CCRD}		Deep standby RTC mode (When RAM is OFF)	32 kHz	24	40	µA	*3, *4 T_A=+25°C
					-	640	µA	*3, *4 T_A=+85°C
					-	813	µA	*3, *4 T_A=+105°C
			Deep standby RTC mode (When RAM is ON)		41	146	µA	*3, *4 T_A=+25°C
					-	1616	µA	*3, *4 T_A=+85°C
					-	2059	µA	*3, *4 T_A=+105°C
	I_{CCVBAT}	VBAT	RTC stop*7	-	0.015	0.14	µA	*3, *4, *5 T_A=+25°C
					-	4.0	µA	*3, *4, *5 T_A=+85°C
					-	9.4	µA	*3, *4, *5 T_A=+105°C
			RTC operation *6, *7		1.3	2.4	µA	*3, *4 T_A=+25°C
					-	6.2	µA	*3, *4 T_A=+85°C
					-	12	µA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0"

*4: When LVD is OFF

*5: When sub oscillation is OFF

*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

*7: In the case of setting RTC after VCC power on

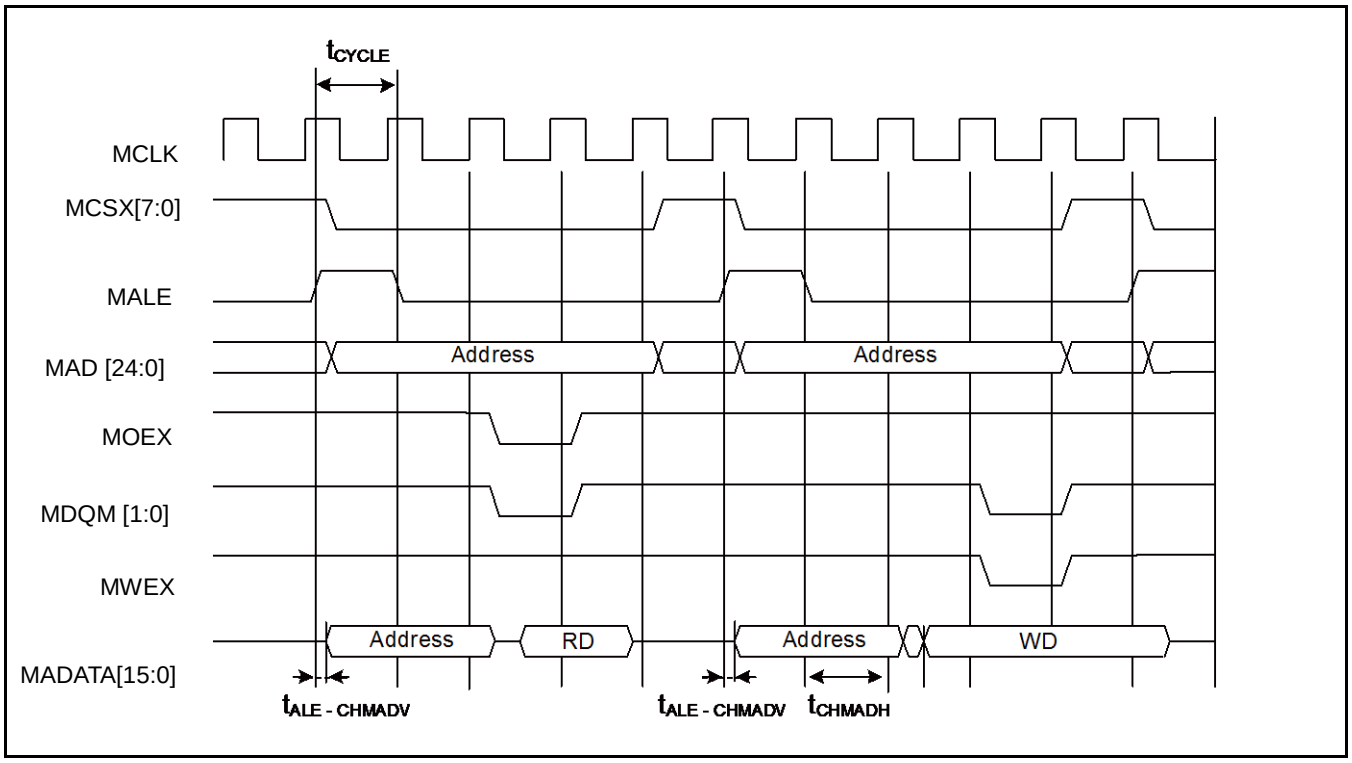
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

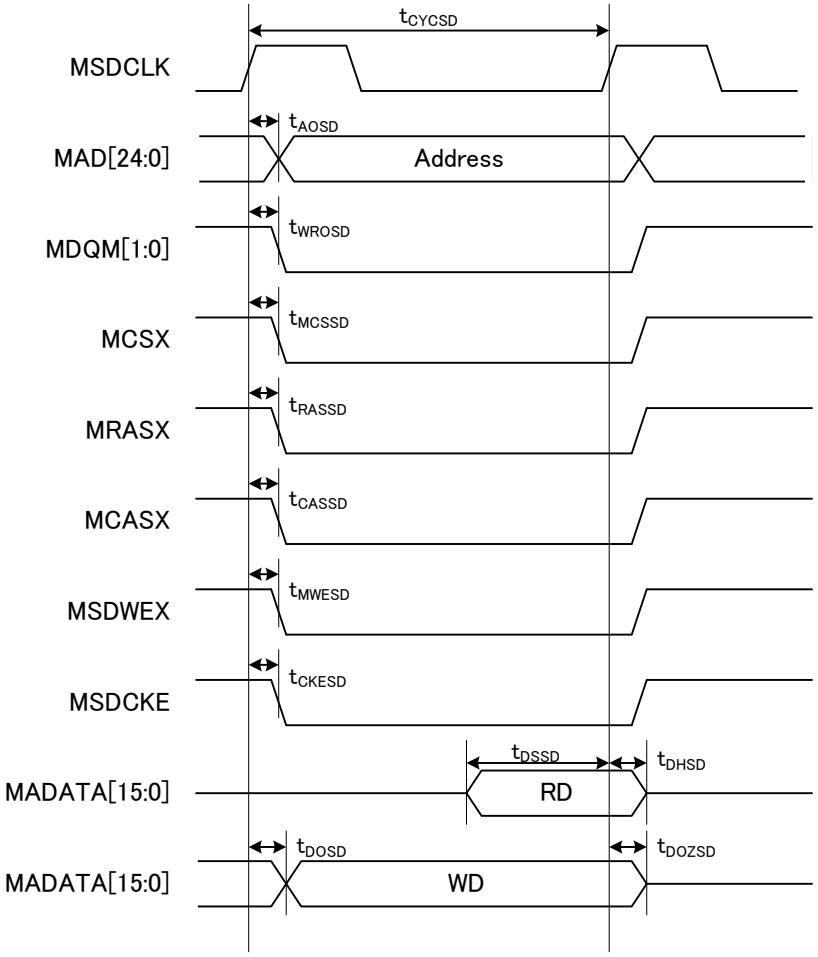
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	10	ns
			$V_{CC} < 4.5$ V		20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 4.5$ V	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 4.5$ V	MCLK×n+0	MCLK×n+20	

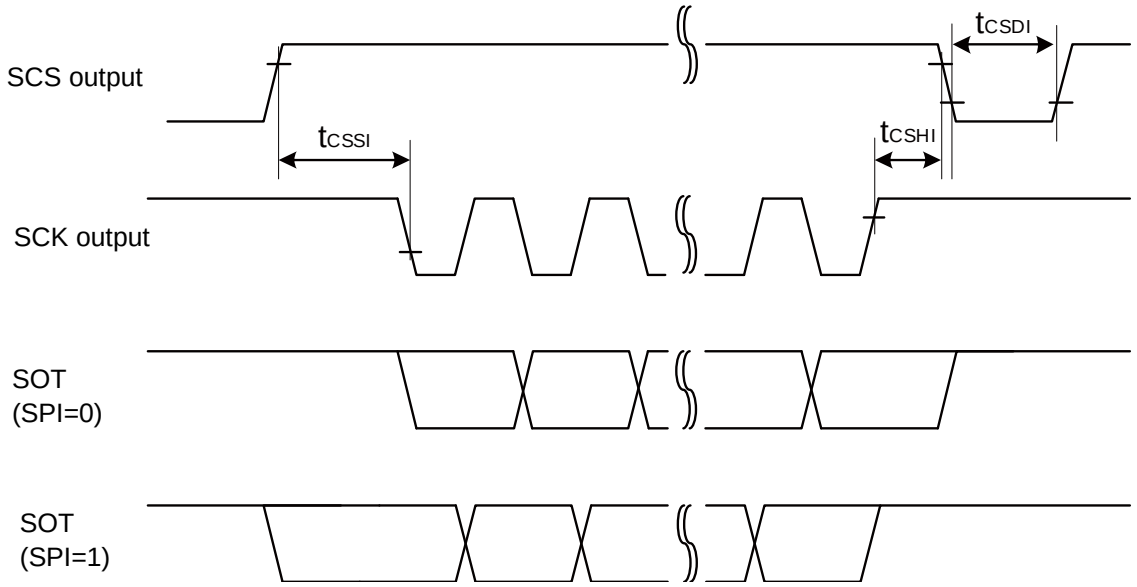
Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*

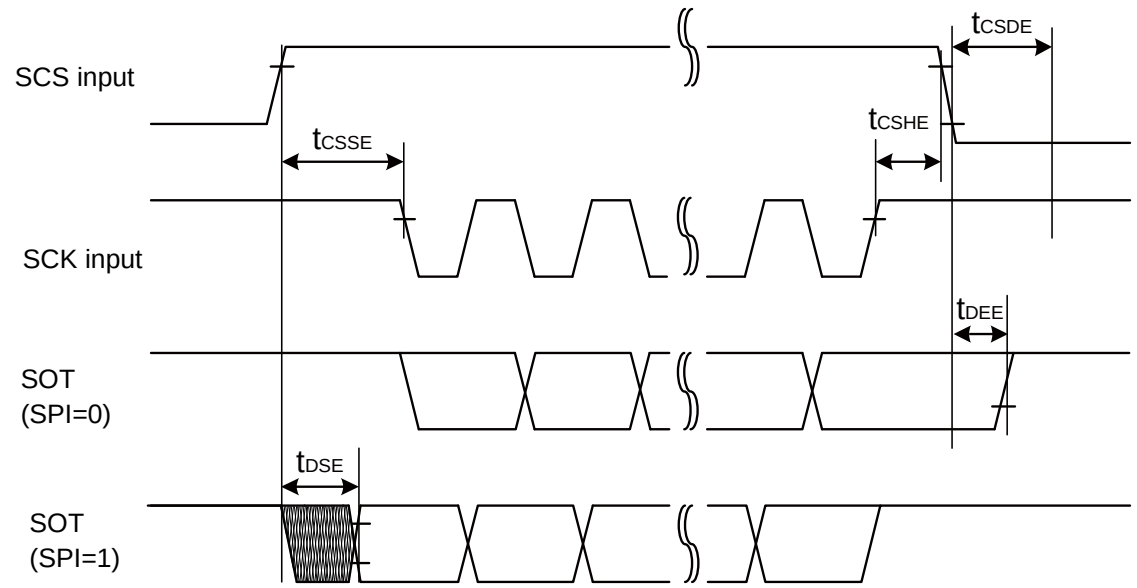


SDRAM Access

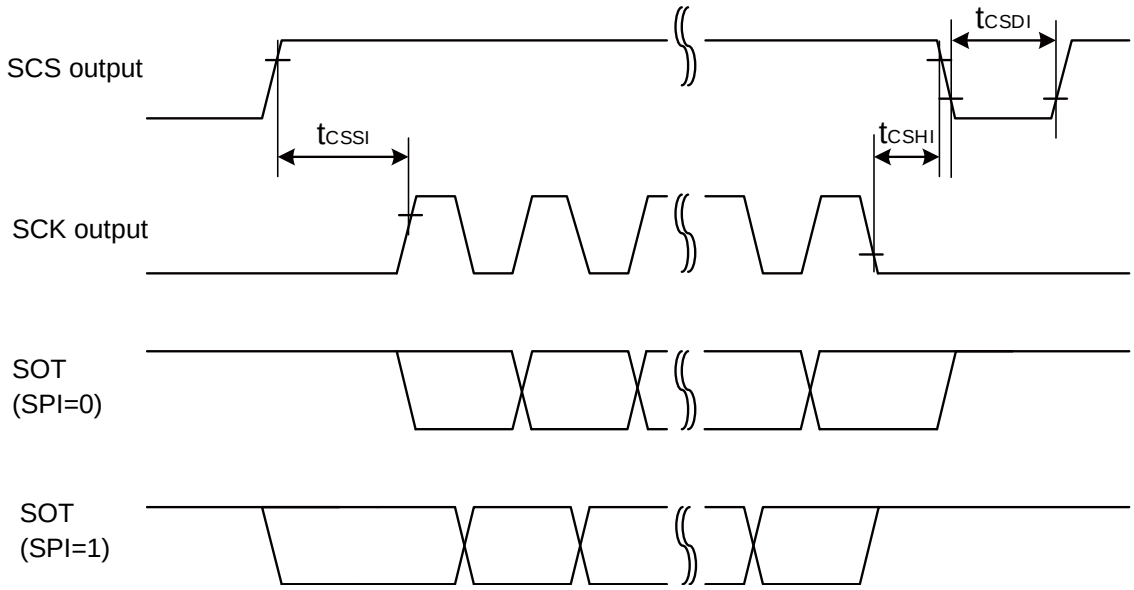




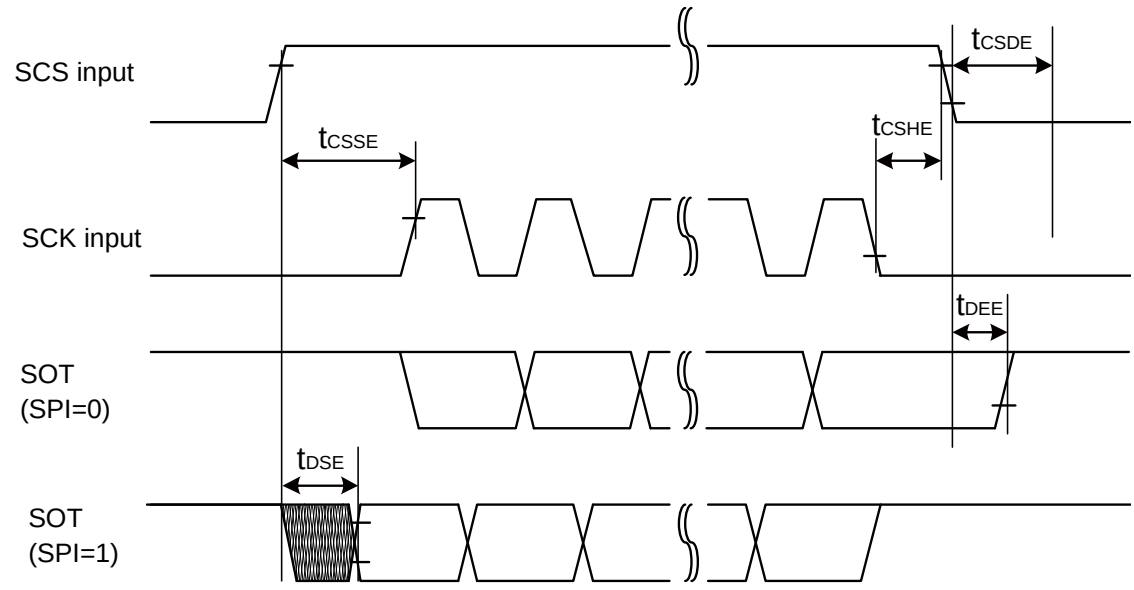
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

13.4.12 External Input Timing

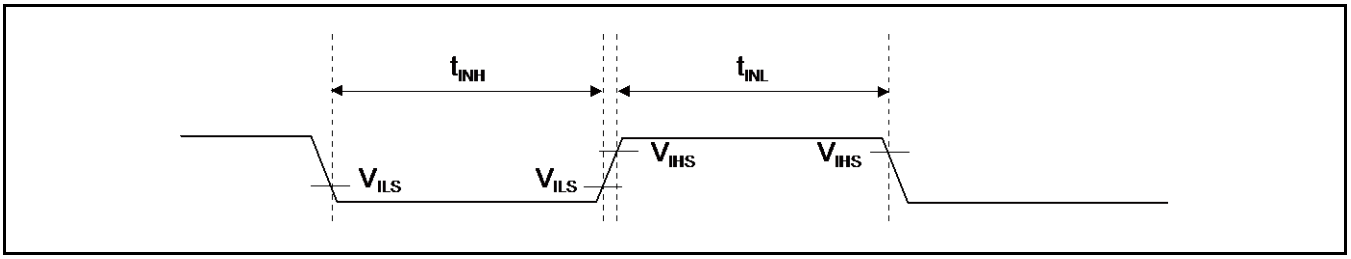
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT15, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

*1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode.
About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see 1. S6E2H Series Block Diagram in this data sheet.

*2: When in Stop mode, in timer mode.

*3: When in deep standby RTC mode, in deep standby Stop mode.

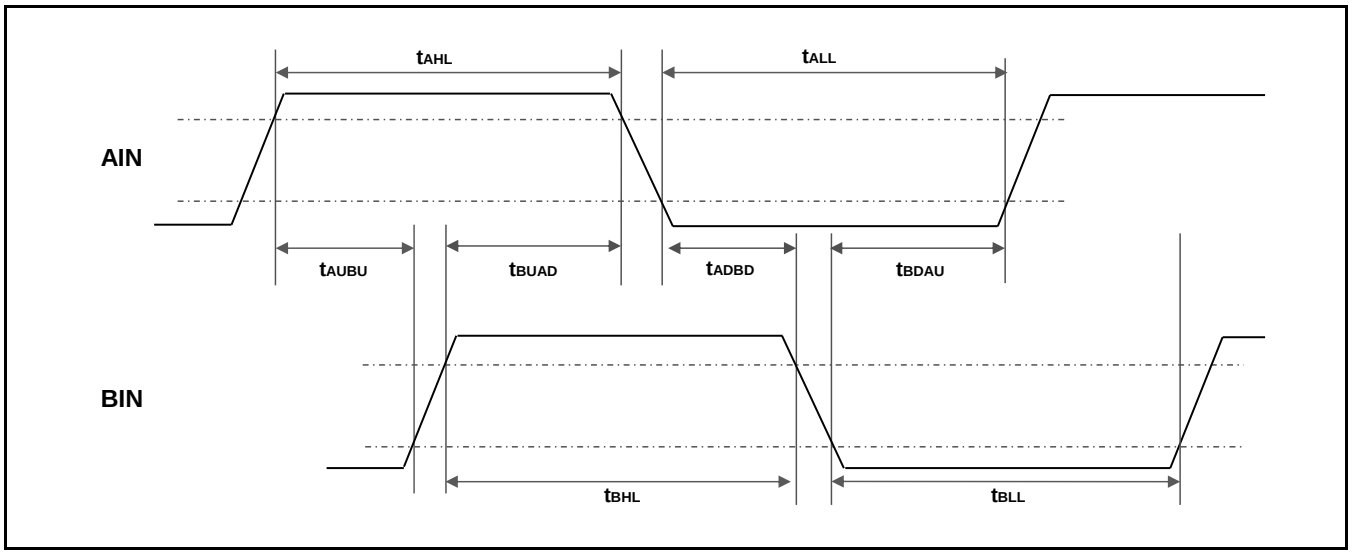


13.4.13 Quadrature Position/Revolution Counter Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC="0"			
ZIN pin L width	t_{ZLL}	QCR:CGSC="0"			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC="1"			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC="1"			

*: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see 1. S6E2H Series Block Diagram in this data sheet.



13.7 Low-Voltage Detection Characteristics

13.7.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

13.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	4480× t_{CYCP}*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

13.10 Standby Recovery Time

13.10.1 Recovery Cause: Interrupt/WKUP

The time from recovery cause reception of the internal circuit to the program operation start is shown.

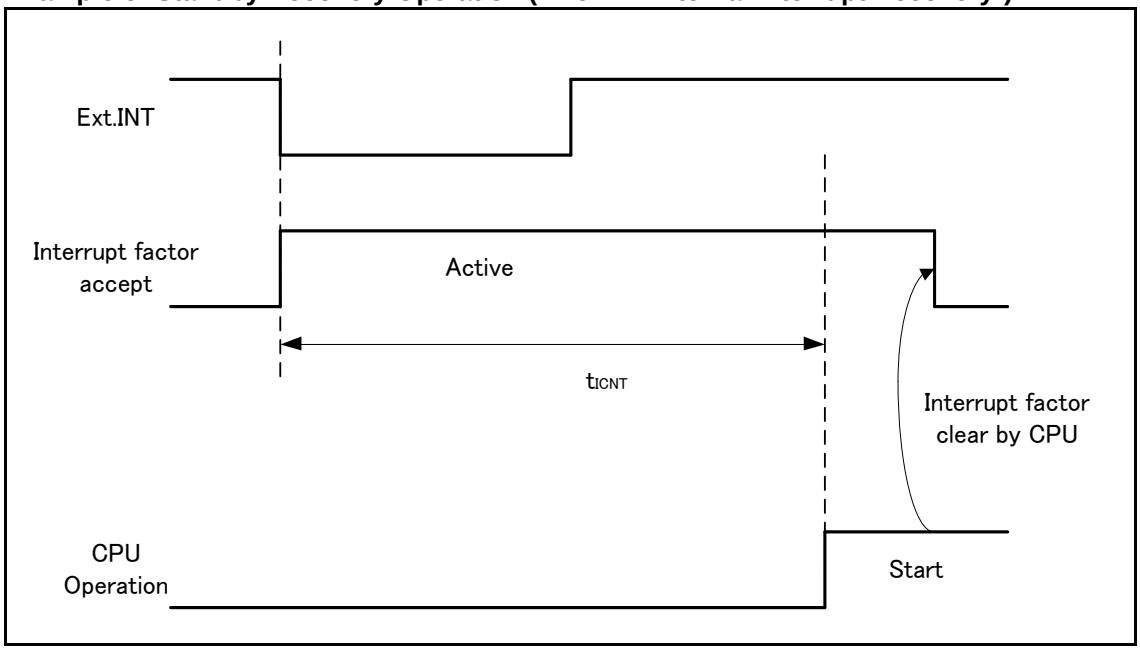
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR timer mode		450	900	µs	
Sub timer mode		896	1136	µs	
RTC mode stop mode (High-speed CR /Main/PLL run mode return)		316	581	µs	
RTC mode stop mode (Low-speed CR/sub run mode return)		270	540		
Deep standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep standby stop mode with RAM retention		365	667	µs	with RAM retention

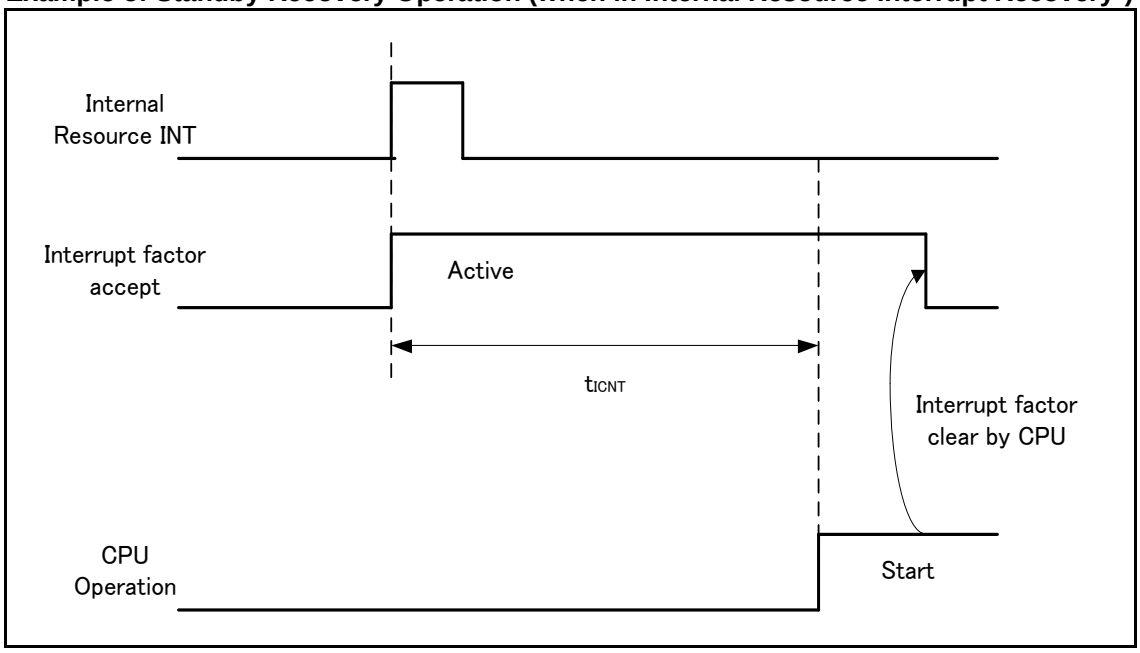
*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery*)

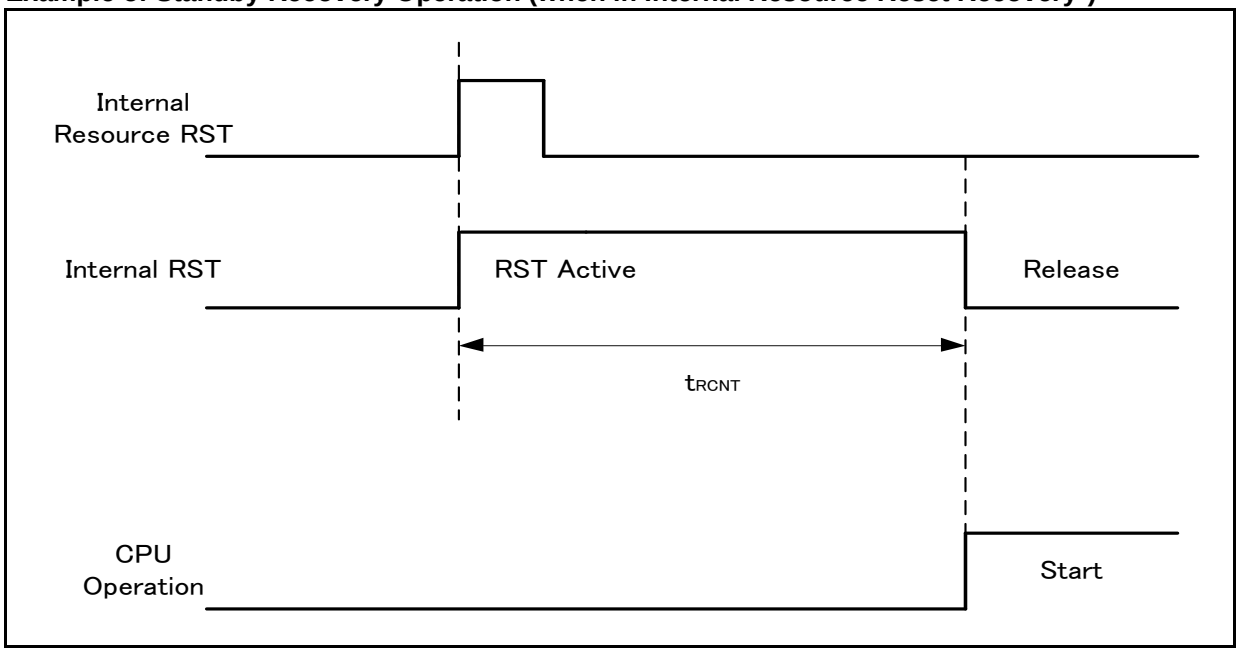


*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main part (002-04856).
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM4 Family Peripheral Manual Main part (002-04856).*

Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)

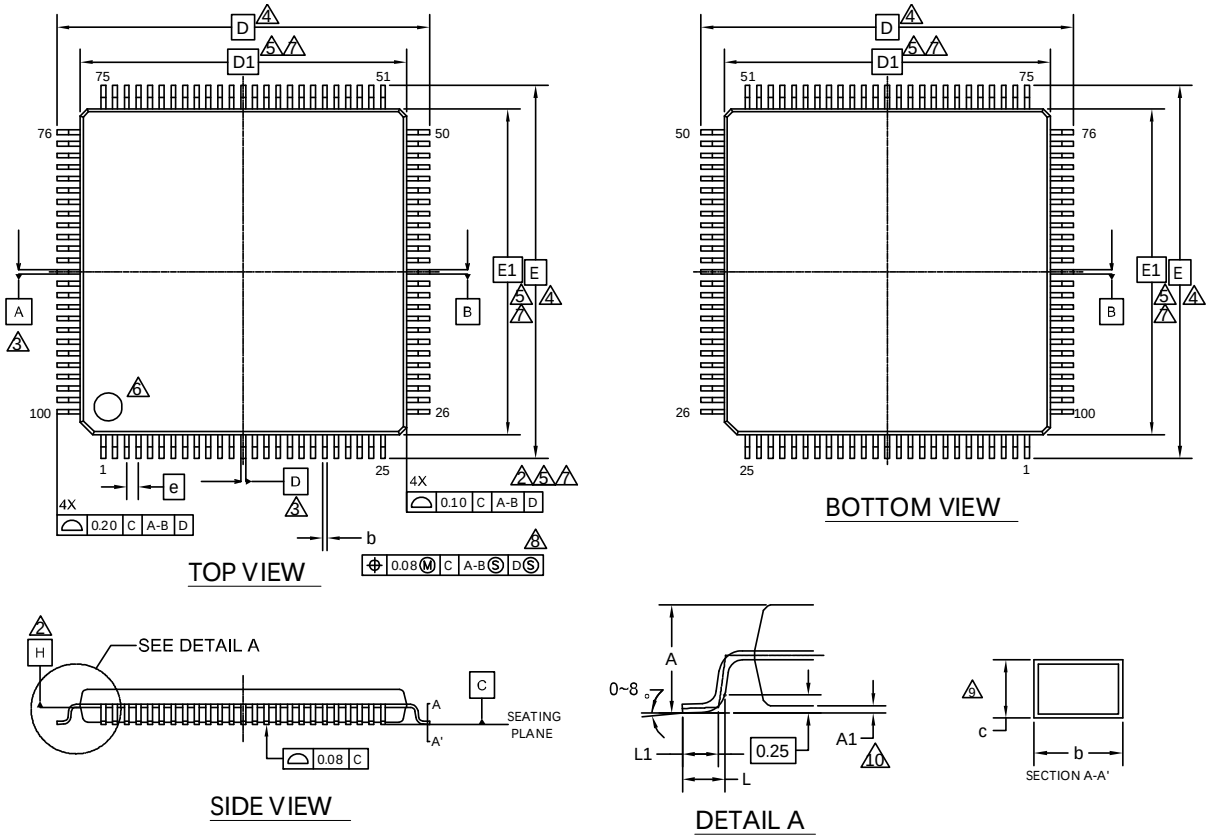


*: Depending on the standby mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main part (002-04856).
- *The time during the power-on reset/low-voltage detection reset is excluded to the recovery source. See (6) Power-on Reset Timing in 13.4. AC Characteristics in 13. Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

Package Type	Package Code
LQFP 100	LQI100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 Rev** 002-11500 **