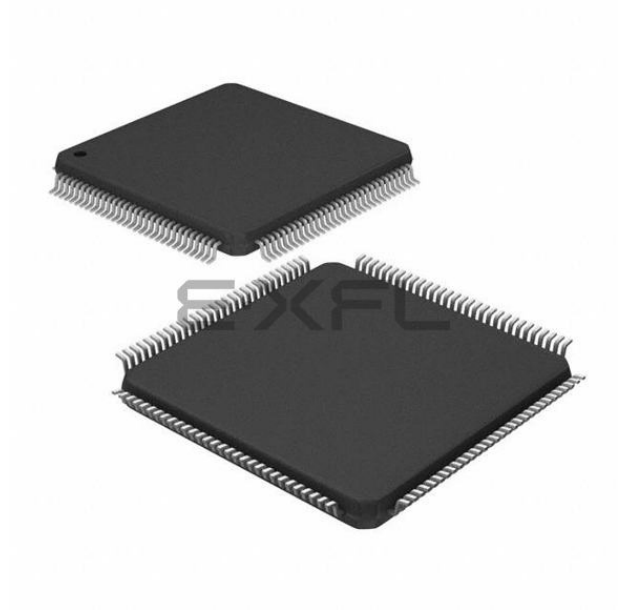

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What is "Embedded - Microcontrollers"?

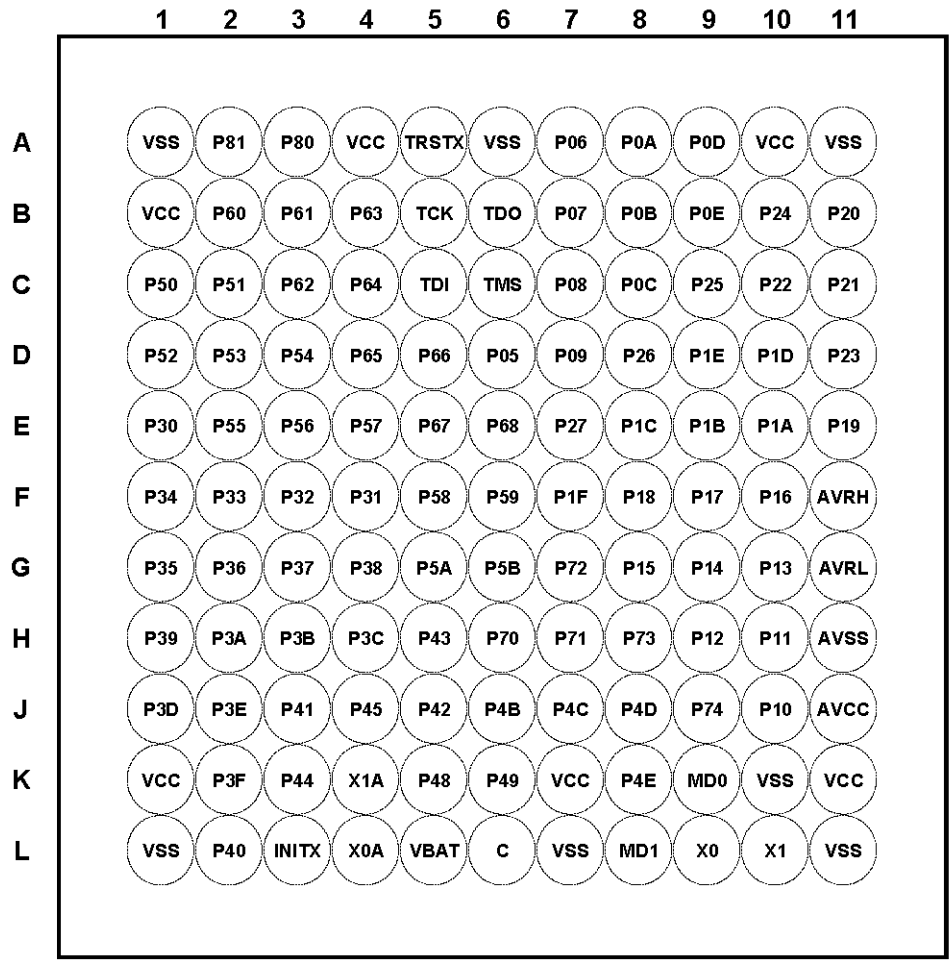
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2hg6g0agv20000

FDI121

(TOP VIEW)



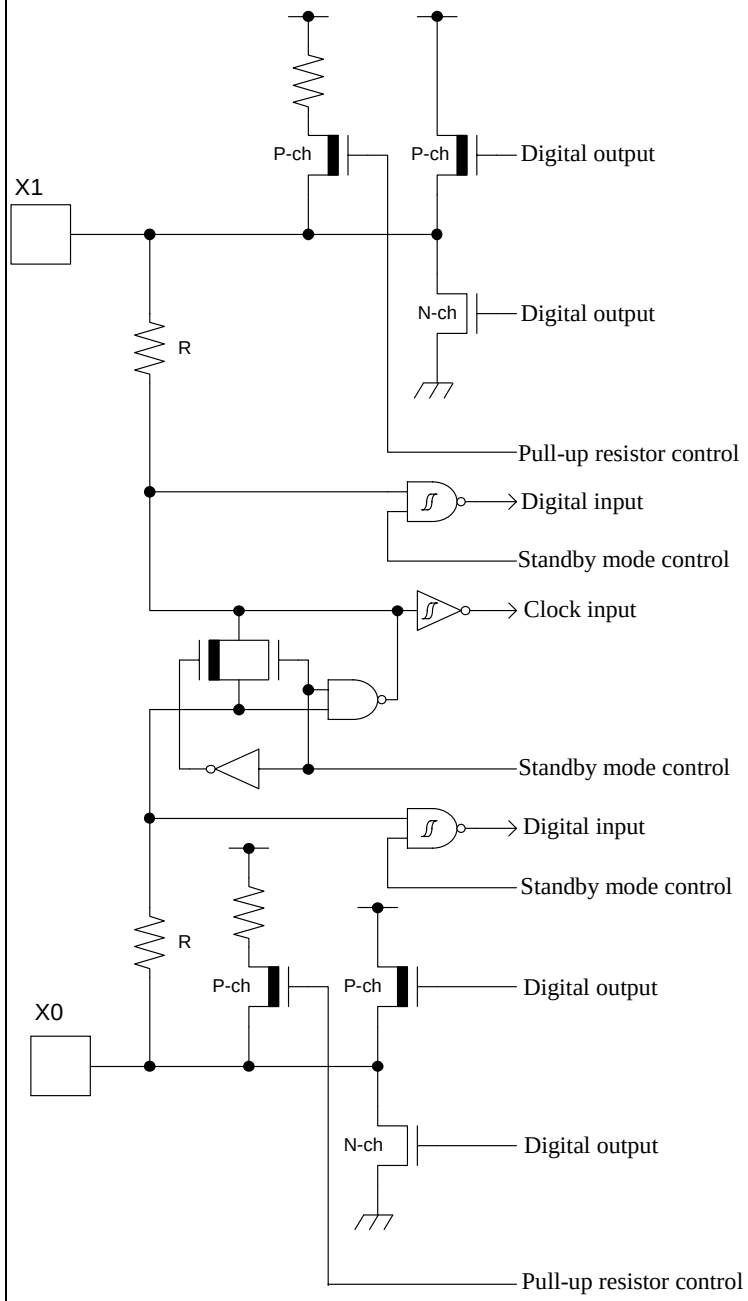
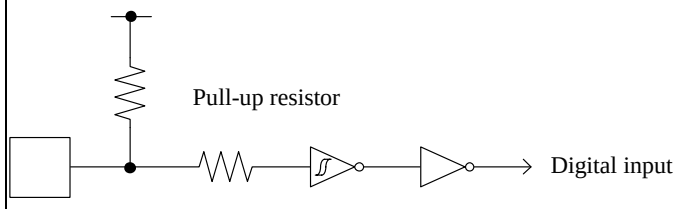
PFBGA-121

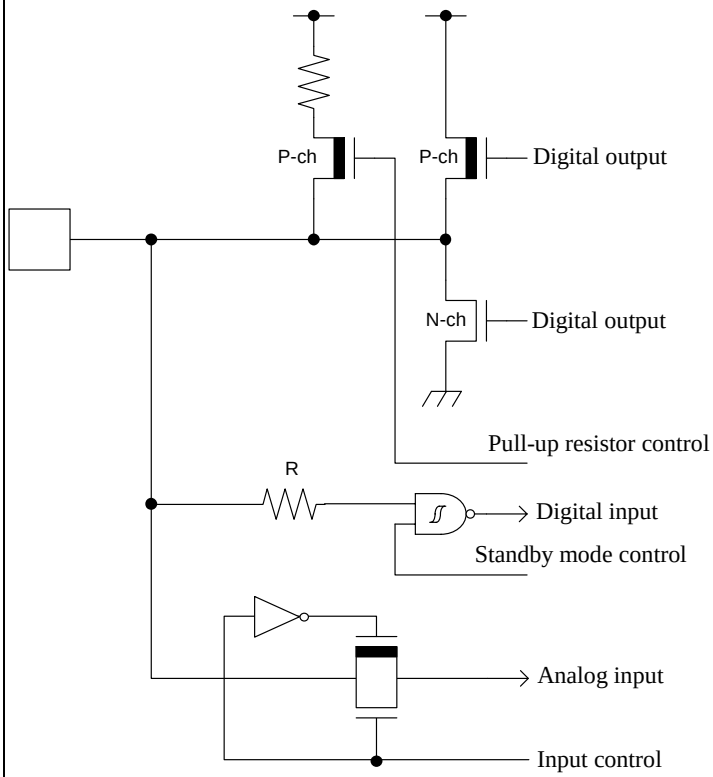
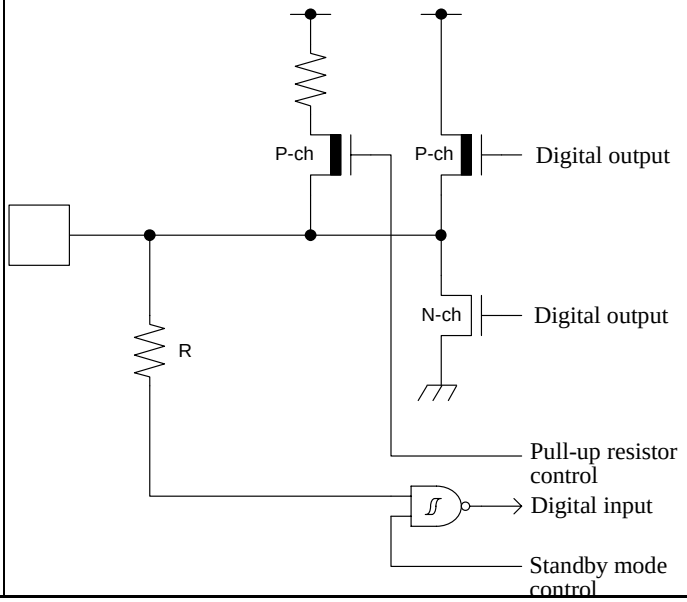
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
20	15	-	G2	P36	E	K
				SIN5_2		
				IC02_0		
				INT09_1		
-			-	MADATA13_0		
20	-	-	G2	MNWEX_0		
21	16	-	G3	P37	E	K
				SOT5_2 (SDA5_2)		
				IC01_0		
				INT05_2		
-			-	MADATA14_0		
21	-	-	G3	MNREX_0		
22	17	-	G4	P38	E	K
				SCK5_2 (SCL5_2)		
				IC00_0		
				INT06_2		
-			-	MADATA15_0		
23	18	13	H1	P39	L	I
				ADTG_2		
				DTTI0X_0		
				RTCCO_2		
				SUBOUT_2		
		-		MSDCLK_0		
24	19	14	H2	P3A	G	I
				TIOA0_1		
				AIN0_0		
				RTO00_0 (PPG00_0)		
		-		MSDCKE_0		
25	20	15	H3	P3B	G	I
				TIOA1_1		
				BIN0_0		
				RTO01_0 (PPG00_0)		
		-		MRASX_0		
26	21	16	H4	P3C	G	I
				TIOA2_1		
				ZIN0_0		
				RTO02_0 (PPG02_0)		
		-		MCASX_0		
27	22	17	J1	P3D	G	I
				TIOA3_1		
				RTO03_0 (PPG02_0)		
				MAD00_0		

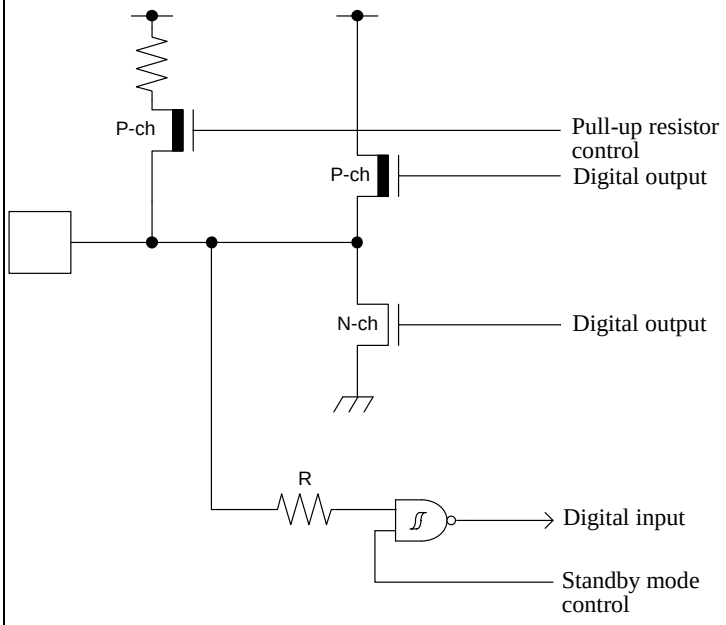
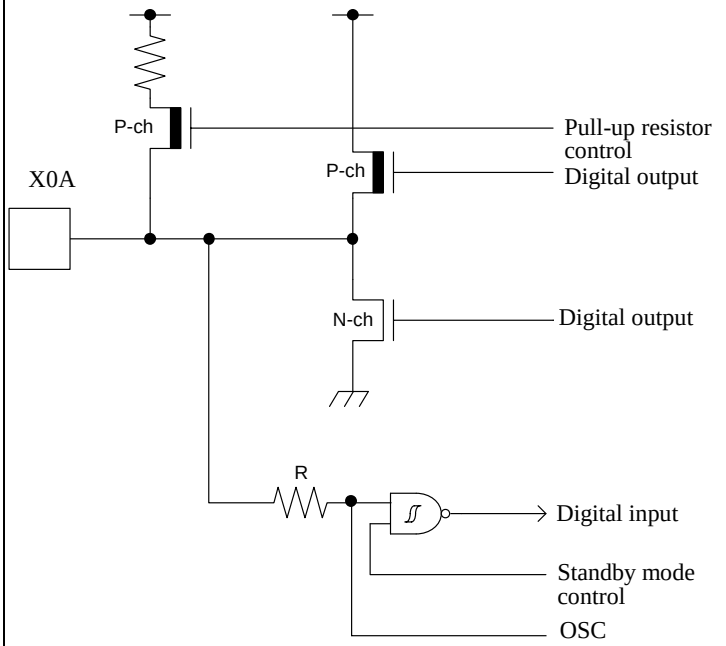
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
28	23	18	J2	P3E TIOA4_1 RTO04_0 (PPG04_0) MAD01_0	G	I
29	24	19	K2	P3F TIOA5_1 RTO05_0 (PPG04_0) MAD02_0	G	I
30	25	20	L1	VSS	-	-
31	26	-	K1	VCC	-	-
32	27	-	L2	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	K
33	28	-	J3	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1 AIN2_0	G	K
34	29	-	J5	P42 TIOA2_0 RTO12_1 (PPG12_1) MSDWEX_0 BIN2_0	G	I
35	30	-	H5	P43 ADTG_7 TIOA3_0 RTO13_1 (PPG12_1) MCSX8_0 ZIN2_0	G	I
36	31	21	K3	P44 TIOA4_0 RTO14_1 (PPG14_1) DA0	R	J
37	32	22	J4	P45 TIOB0_0 RTO15_1 (PPG14_1) DA1	R	J
38	33	23	L3	INITX	B	C

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
97	82	67	D7	P09	M	N
				AN19		
		-		TRACED0		
		67		TIOA3_2		
				SOT1_0 (SDA1_0)		
				S_DATA2_0		
				MCSX5_0		
				IC23_1		
98	83	-	C7	P08	F	N
				AN20		
				TRACED1		
				TIOB3_2		
				SCK1_0 (SCL1_0)		
				MCSX4_0		
				IC22_1		
99	84	-	B7	P07	M	N
				AN21		
				TRACED2		
				TIOA0_2		
				SCK7_0 (SCL7_0)		
				MCLKOUT_0		
				IC21_1		
100	85	-	A7	P06	F	N
				AN22		
				TRACED3		
				TIOB0_2		
				SOT7_0 (SDA7_0)		
				MCSX3_0		
				IC20_1		
101	86	-	D6	P05	F	O
				AN23		
				ADTG_0		
				TRACECLK		
				SIN7_0		
				INT01_1		
				MCSX2_0		
				FRCK2_1		
102	87	68	B6	P04	E	G
				TDO		
				SWO		
103	88	69	C6	P03	E	G
				TMS		
				SWDIO		

7. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. – Oscillation feedback resistor : Approximately 1MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA
B		– CMOS level hysteresis input – Pull-up resistor : Approximately 50 kΩ

Type	Circuit	Remarks
F		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
G		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -12 mA, I_{OL} = 12 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
O		– CMOS level output – CMOS level hysteresis input – 5 V tolerant – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual
P		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual

Notes on Power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.
VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(A) in FM4 Family Peripheral Manual Main Part (002-04856).
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on: VBAT → VCC
VCC → AVCC → AVRH
Turning off: AVRH → AVCC → VCC
VCC → VBAT

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

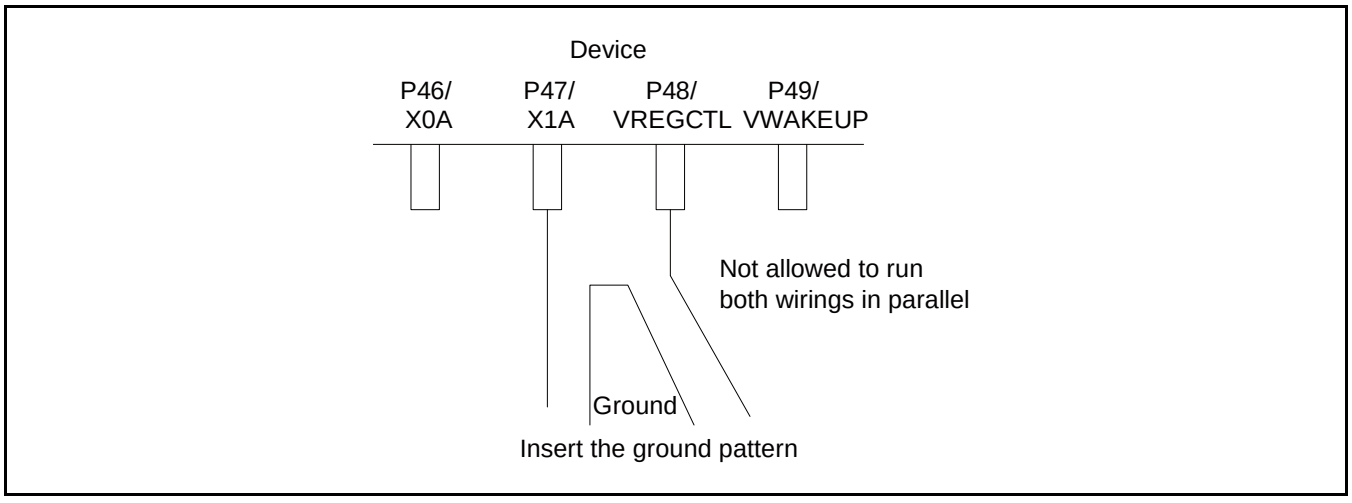
If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Adjoining Wiring on Circuit Board

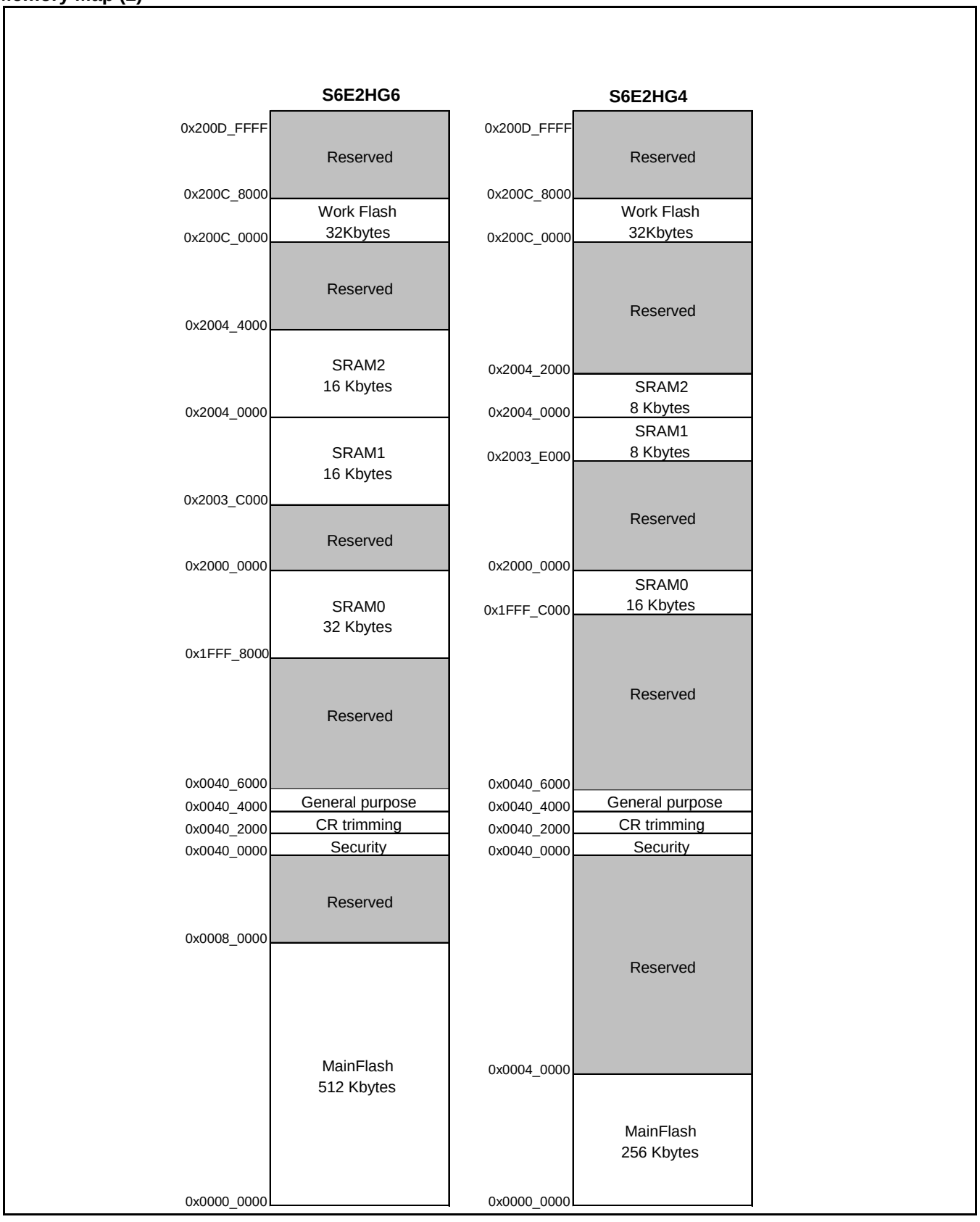
If wiring of the crystal oscillation circuit X1A adjoins and also runs in parallel with the wiring of P48/VREGCTL, there is a possibility that the oscillation erroneously counts because X1A has noise with the change of P48/VREGCTL. Keep as much distance as possible between both wirings and insert the ground pattern between them in order to avoid this possibility.



Handling when Using Debug Pins

When debug pins(TDO/TMS/TDI/TCK/TRSTX or SWO/SWDIO/SWCLK) are set to GPIO or other peripheral functions, only set them as output, do not set them as input.

Memory Map (2)


S6E2HG6
0x200D_FFFF
Reserved
0x200C_8000
Work Flash
32Kbytes
0x200C_0000
Reserved
0x2004_4000
SRAM2
16 Kbytes
0x2004_0000
SRAM1
16 Kbytes
0x2003_C000
Reserved
0x2000_0000
SRAM0
32 Kbytes
0x1FFF_8000
Reserved
0x0040_6000
0x0040_4000
General purpose
0x0040_2000
CR trimming
0x0040_0000
Security
Reserved
0x0008_0000
MainFlash
512 Kbytes
0x0000_0000
S6E2HG4
0x200D_FFFF
Reserved
0x200C_8000
Work Flash
32Kbytes
0x200C_0000
Reserved
0x2004_2000
SRAM2
8 Kbytes
0x2004_0000
SRAM1
8 Kbytes
0x2003_E000
Reserved
0x2000_0000
SRAM0
16 Kbytes
0x1FFF_C000
Reserved
0x0040_6000
0x0040_4000
General purpose
0x0040_2000
CR trimming
0x0040_0000
Security
Reserved
0x0004_0000
MainFlash
256 Kbytes
0x0000_0000

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									Maintain previous state
G	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
J	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*2	*3	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled		Maintain previous state	Hi-Z / Internal input fixed at 0			
	GPIO selected									

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$$

- I_{OL}: L level output current
- I_{OH}: H level output current
- V_{OL}: L level output voltage
- V_{OH}: H level output voltage

I_{CC} is a current consumed in device.
It can be analyzed as follows.

$$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$$

I_{CC}(INT): Current consumed in internal logic and memory, etc. through regulator

ΣI_{CC}(IO): Sum of current (I/O switching current) consumed in output pin

For I_{CC} (INT), it can be anticipated by (1) Current Rating in 3. DC Characteristics (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$$

- C_{INT}: Pin internal load capacitance
- C_{EXT}: External load capacitance of output pin
- f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself.

1. Measure current value I_{CC} (Typ) at normal temperature (+25°C).
2. Add maximum leak current value I_{CC} (leak_max) at operating on a value in (1).

$$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$$

Parameter	Symbol	Conditions	Current Value
Maximum leak current at operating	I_{CC}(leak_max)	T_J = +125°C	16.8 mA
		T_J = +105°C	8.6 mA
		T_J = +85°C	5.8 mA

Table 12-4 Typical and Maximum Current Consumption in Normal Operation(other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 wait-cycle Mode and Read Access 0 wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (main oscillation)	*5*6	4 MHz	4.0	24	mA	*3 When all peripheral clocks are ON
						3.2	24	mA	*3 When all peripheral clocks are OFF
			Normal operation (built-in high-speed CR)	*5	4 MHz	3.2	24	mA	*3 When all peripheral clocks are ON
						2.7	23	mA	*3 When all peripheral clocks are OFF
			Normal operation (sub oscillation)	*5	32 kHz	0.34	21	mA	*3 When all peripheral clocks are ON
						0.30	21	mA	*3 When all peripheral clocks are OFF
			Normal operation (built-in low-speed CR)	*5	100 kHz	0.36	21	mA	*3 When all peripheral clocks are ON
						0.33	21	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, VC_C=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0"

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 000)

*6: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation(other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation *5 (main oscillation)	4MHz	2.1	22	mA	*3 When all peripheral clocks are ON
					1.3	22	mA	*3 When all peripheral clocks are OFF
			Sleep operation (built-in high-speed CR)	4 MHz	1.3	22	mA	*3 When all peripheral clocks are ON
					0.8	21	mA	*3 When all peripheral clocks are OFF
			Sleep operation (sub oscillation)	32 kHz	0.28	21	mA	*3 When all peripheral clocks are ON
					0.27	21	mA	*3 When all peripheral clocks are OFF
			Sleep operation (built-in low-speed CR)	100 kHz	0.29	21	mA	*3 When all peripheral clocks are ON
					0.28	21	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0"

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

13.4.9 External Bus Timing

External Bus Clock Output Characteristics

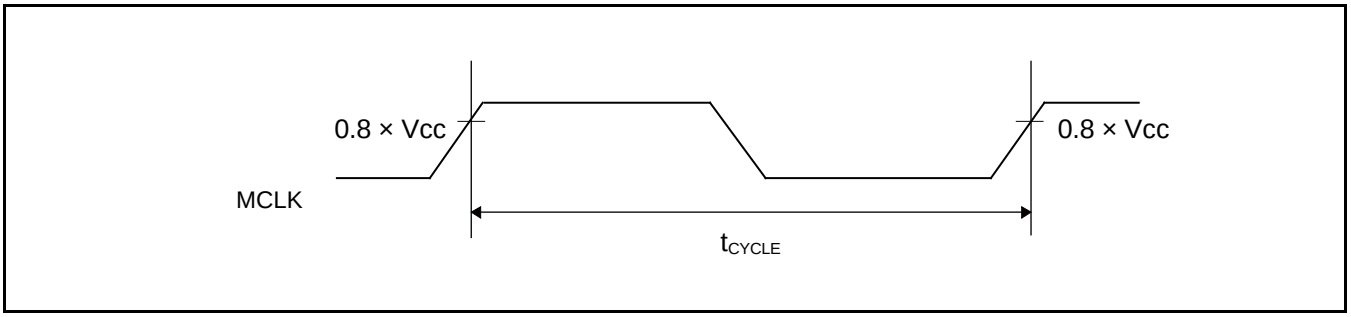
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	$V_{CC} \geq 4.5$ V	-	50*2	MHz
			$V_{CC} < 4.5$ V	-	32*3	MHz

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main part (002-04856).

*2: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 100 MHz.

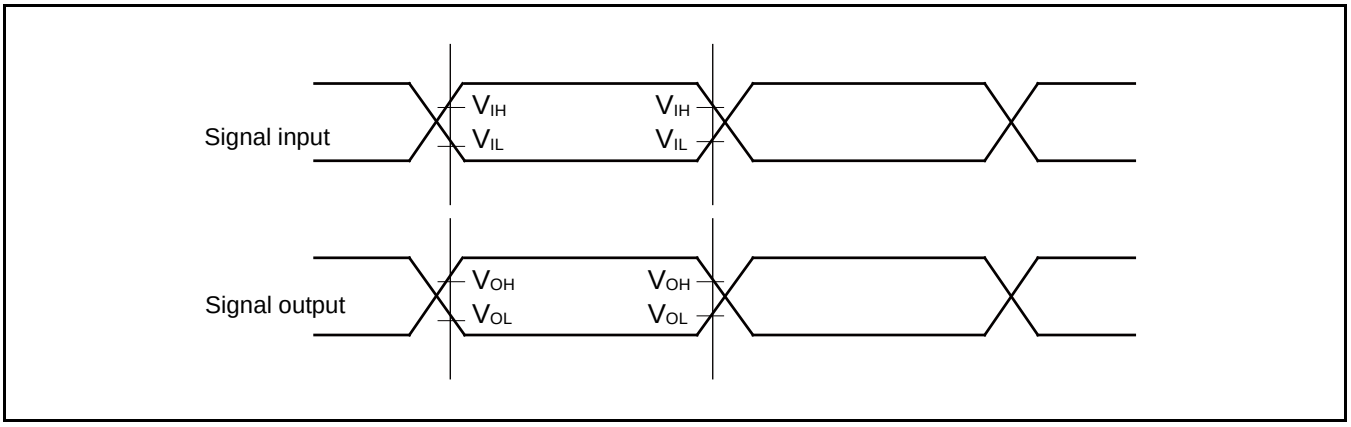
*3: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 64 MHz.



External Bus Signal Input/output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



When Using High-speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↓→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

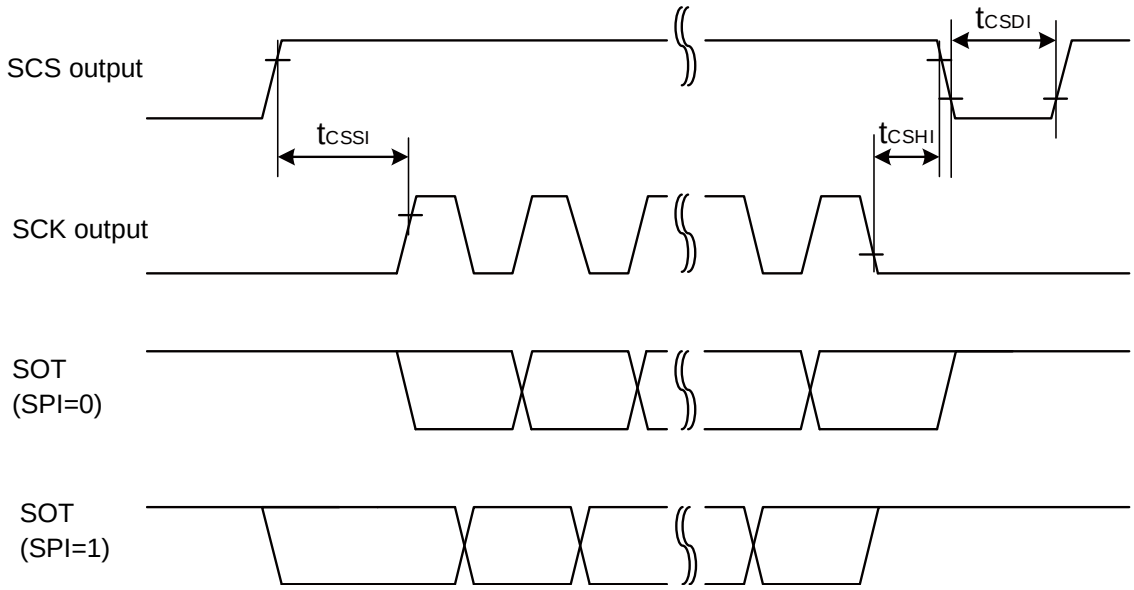
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

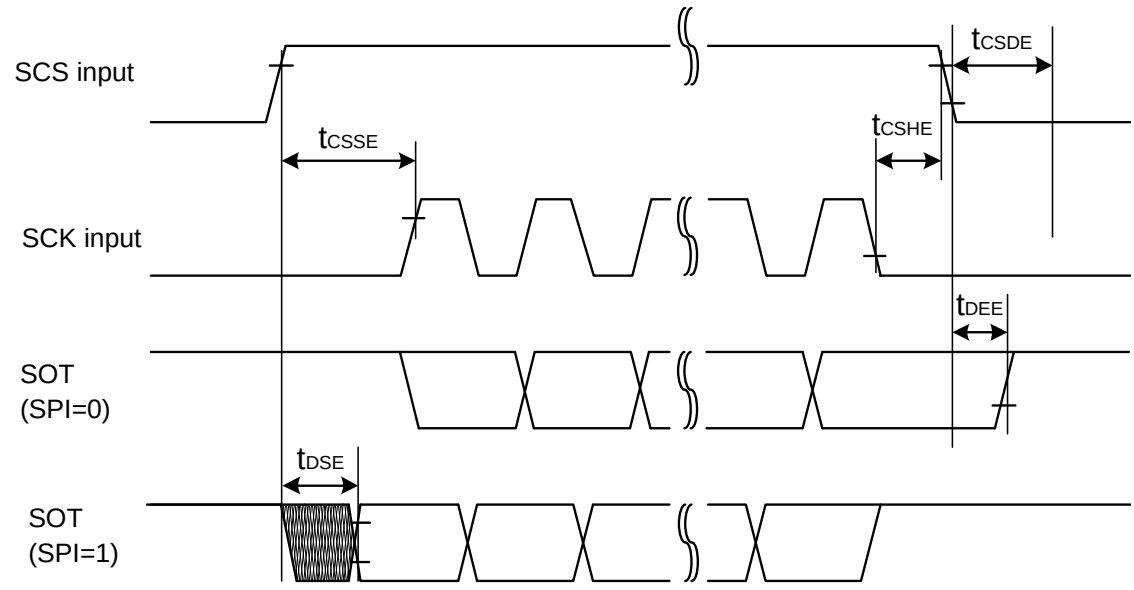
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 1. S6E2H Series Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0

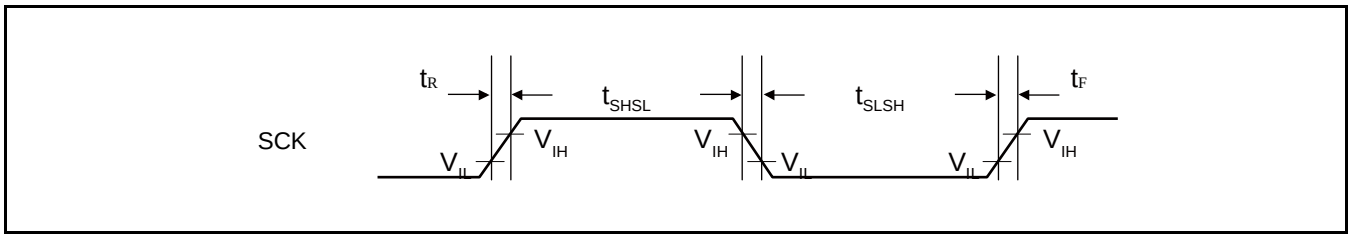


MS bit = 1

External Clock (EXT = 1): when in Asynchronous Mode Only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



13.4.14 I²C Timing

Standard-mode, Fast-mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP}<40 MHz	$2t_{CYCP}$*4	-	$2t_{CYCP}$*4	-	ns	*5
		40 MHz ≤ t_{CYCP}<60 MHz	$4t_{CYCP}$*4	-	$4t_{CYCP}$*4	-	ns	
		60 MHz ≤ t_{CYCP}<80 MHz	$6t_{CYCP}$*4	-	$6t_{CYCP}$*4	-	ns	
		80 MHz ≤ t_{CYCP}<100 MHz	$8t_{CYCP}$*4	-	$8t_{CYCP}$*4	-	ns	
		100 MHz ≤ t_{CYCP}<120 MHz	$10t_{CYCP}$*4	-	$10t_{CYCP}$*4	-	ns	
		120 MHz ≤ t_{CYCP}<140 MHz	$12t_{CYCP}$*4	-	$12t_{CYCP}$*4	-	ns	
		140 MHz ≤ t_{CYCP}<160 MHz	$14t_{CYCP}$*4	-	$14t_{CYCP}$*4	-	ns	
		160 MHz ≤ t_{CYCP}<180 MHz	$16t_{CYCP}$*4	-	$16t_{CYCP}$*4	-	ns	

1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

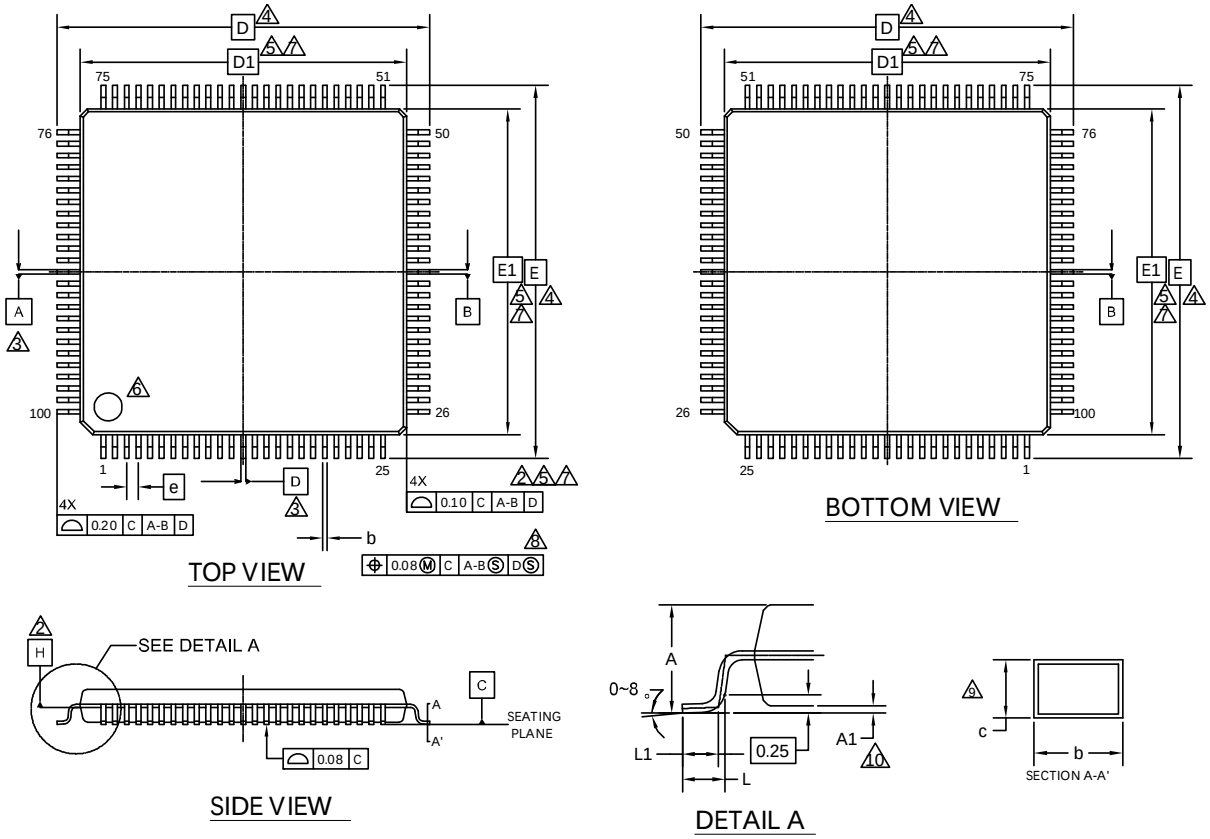
2: The maximum t_{HDDAT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

3: Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I²C is connected, see 1.S6E2H Series Block Diagram in this data sheet.
When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.
When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.

5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

Package Type	Package Code
LQFP 100	LQI100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 Rev** 002-11500 **

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*E	5639294	NOSU	02/22/2017	Updated Circuit of “type N” in 7 I/O Circuit Type. Added the Baud rate spec in 13.4.11 CSIO Timing (Page 102, 104, 106, 108) Corrected MPNs as below to 14. Ordering Information. S6E2H14G0AGB30000 → S6E2H14G0AGB3000A S6E2H16G0AGB30000 → S6E2H16G0AGB3000A S6E2H44G0AGB30000 → S6E2H44G0AGB3000A S6E2H46G0AGB30000 → S6E2H46G0AGB3000A S6E2HE4G0AGB30000 → S6E2HE4G0AGB3000A S6E2HE6F0AGV20000 → S6E2HE6F0AGV2000A S6E2HE6G0AGB30000 → S6E2HE6G0AGB3000A S6E2HG4G0AGB30000 → S6E2HG4G0AGB3000A S6E2HG6G0AGB30000 → S6E2HG6G0AGB3000A Updated figures in 15. Package Dimensions.