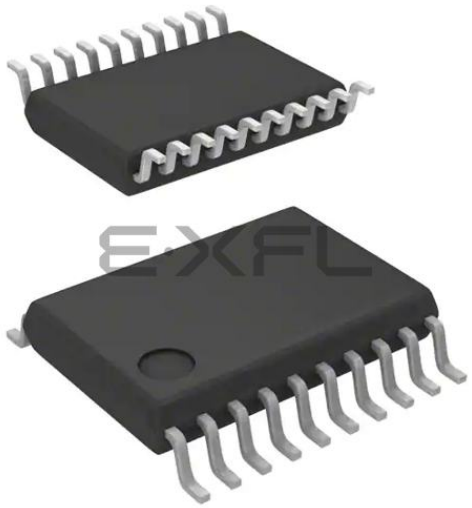
# Renesas Electronics America Inc - R5F21321DNSP#U0 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 15 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21321dnsp-u0 |

| Address | Register | Symbol | Page |
|---|---|---|---|
| 0180h | Timer RA Pin Select Register | TRASR | 63, 166 |
| 0181h | Timer RC Pin Select Register | TRBRCSR | 63, 210 |
| 0182h | Timer RC Pin Select Register 0 | TRCPSR0 | 64, 211 |
| 0183h | Timer RC Pin Select Register 1 | TRCPSR1 | 64, 211 |
| 0184h | | | |
| 0185h | | | |
| 0186h | | | |
| 0187h | | | |
| 0188h | UART0 Pin Select Register | U0SR | 65, 267 |
| 0189h | | | |
| 018Ah | UART2 Pin Select Register 0 | U2SR0 | 65, 293 |
| 018Bh | UART2 Pin Select Register 1 | U2SR1 | 66, 293 |
| 018Ch | | | |
| 018Dh | | | |
| 018Eh | INT Interrupt Input Pin Select Register | INTSR | 66, 132 |
| 018Fh | I/O Function Pin Select Register | PINSR | 67 |
| 0190h | | | |
| 0191h | | | |
| 0192h | | | |
| 0193h | | | |
| 0194h | | | |
| 0195h | | | |
| 0196h | | | |
| 0197h | | | |
| 0198h | | | |
| 0199h | | | |
| 019Ah | | | |
| 019Bh | | | |
| 019Ch | | | |
| 019Dh | | | |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | |
| 01A4h | | | |
| 01A5h | | | |
| 01A6h | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | Flash Memory Status Register | FST | 364 |
| 01B3h | | | |
| 01B4h | Flash Memory Control Register 0 | FMR0 | 366 |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 368 |
| 01B6h | Flash Memory Control Register 2 | FMR2 | 369 |
| 01B7h | | | |
| 01B8h | | | |
| 01B9h | | | |
| 01BAh | | | |
| 01BBh | | | |
| 01BCh | | | |
| 01BDh | | | |
| 01BEh | | | |

Note:
1. The blank regions are reserved. Do not access locations in these regions.

| Address | Register | Symbol | Page |
|---|---|---|---|
| 01C0h | Address Match Interrupt Register 0 | RMAD0 | 138 |
| 01C1h | | | |
| 01C2h | | | |
| 01C3h | Address Match Interrupt Enable Register | AIER | 138 |
| 01C4h | Address Match Interrupt Register 1 | RMAD1 | 138 |
| 01C5h | | | |
| 01C6h | | | |
| 01C7h | | | |
| 01C8h | | | |
| 01C9h | | | |
| 01CAh | | | |
| 01CBh | | | |
| 01CCh | | | |
| 01CDh | | | |
| 01CEh | | | |
| 01CFh | | | |
| 01D0h | | | |
| 01D1h | | | |
| 01D2h | | | |
| 01D3h | | | |
| 01D4h | | | |
| 01D5h | | | |
| 01D6h | | | |
| 01D7h | | | |
| 01D8h | | | |
| 01D9h | | | |
| 01DAh | | | |
| 01DBh | | | |
| 01DCh | | | |
| 01DDh | | | |
| 01DEh | | | |
| 01DFh | | | |
| 01E0h | Pull-Up Control Register 0 | PUR0 | 68 |
| 01E1h | Pull-Up Control Register 1 | PUR1 | 68 |
| 01E2h | | | |
| 01E3h | | | |
| 01E4h | | | |
| 01E5h | | | |
| 01E6h | | | |
| 01E7h | | | |
| 01E8h | | | |
| 01E9h | | | |
| 01EAh | | | |
| 01EBh | | | |
| 01ECh | | | |
| 01EDh | | | |
| 01EEh | | | |
| 01EFh | | | |
| 01F0h | Port P1 Drive Capacity Control Register | P1DRR | 69 |
| 01F1h | | | |
| 01F2h | Drive Capacity Control Register 0 | DRR0 | 70 |
| 01F3h | Drive Capacity Control Register 1 | DRR1 | 70 |
| 01F4h | | | |
| 01F5h | Input Threshold Control Register 0 | VLT0 | 71 |
| 01F6h | Input Threshold Control Register 1 | VLT1 | 71 |
| 01F7h | | | |
| 01F8h | Comparator B Control Register 0 | INTCMP | 354 |
| 01F9h | | | |
| 01FAh | External Input Enable Register 0 | INTEN | 133, 354 |
| 01FBh | | | |
| 01FCh | INT Input Filter Select Register 0 | INTF | 133, 355 |
| 01FDh | | | |
| 01FEh | Key Input Enable Register 0 | KIEN | 136 |
| 01FFh | | | |

| | | | |
|---|---|---|---|
| FFDBh | Option Function Select Register 2 | OFS2 | 26, 150, 157 |
| : | | | |
| FFFFh | Option Function Select Register | OFS | 25, 44, 149, 156, 362 |

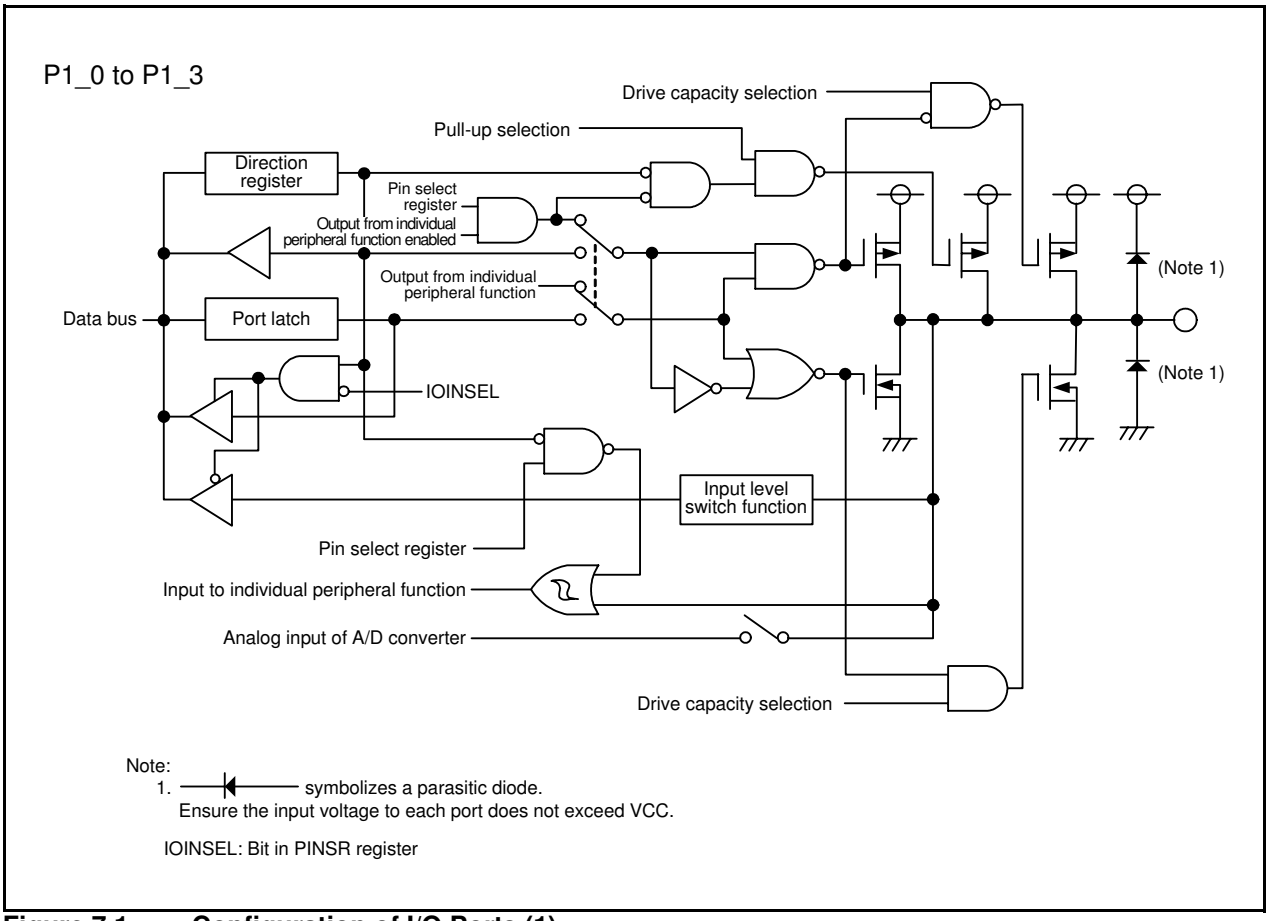



**Figure 7.1 Configuration of I/O Ports (1)**

### 7.4.11 I/O Function Pin Select Register (PINSR)

Address 018Fh

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | — | — | — | — | IOINSEL | — | — | — |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | — | Reserved bits | Set to 0. | R/W |
| b1 | — | | | |
| b2 | — | Nothing is assigned. If necessary, set to 0. When read, the content is 0. | | — |
| b3 | IOINSEL | I/O port input function select bit | 0: The I/O port input function depends on the PDi (i = 1, 3, 4) register.<br>When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read.<br>When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read.<br>1: The I/O port input function reads the pin input level regardless of the PDi register. | R/W |
| b4 | — | Reserved bits | Set to 0. | R/W |
| b5 | — | | | |
| b6 | — | | | |
| b7 | — | | | |

#### IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi_j (j = 0 to 7) bit in the PDi (i = 1, 3, 4) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 7.4 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports except P4_2.

**Table 7.4 I/O Port Values Read by Using IOINSEL Bit**

| PDi_j bit in PDi register | 0 (input mode) | | 1 (output mode) | |
|---|---|---|---|---|
| IOINSEL bit | 0 | 1 | 0 | 1 |
| I/O port values read | Pin input level | | Port latch value | Pin input level |

**Table 7.10 Port P1_5/RXD0/TRAIO/$\overline{\text{INT1}}$**

| Register | PD1 | U0SR | TRASR | | TRAIOC | TRAMR | | | INTSR | | | INTEN | INTCMP | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | PD1_5 | RXD0SEL0 | TRAIOSEL | | TOPCR | TMOD | | | INT1SEL | | | INT1EN | INT1CP0 | |
| | | | 1 | 0 | | 2 | 1 | 0 | 2 | 1 | 0 | | | |
| Setting Value | 0 | X | Other than 10b | | X | X | X | X | X | X | X | X | X | Input port (1) |
| | 1 | X | Other than 10b | | X | X | X | X | X | X | X | X | X | Output port (2) |
| | 0 | 1 | Other than 10b | | X | X | X | X | X | X | X | X | X | RXD0 input (1) |
| | 0 | X | 1 | 0 | 0 | Other than 000b, 001b | | | X | X | X | X | X | TRAIO input (1) |
| | 0 | X | Other than 10b | | X | X | X | X | 0 | 0 | 1 | 1 | 0 | $\overline{\text{INT1}}$ input (1) |
| | 0 | X | 1 | 0 | 0 | Other than 000b, 001b | | | 0 | 0 | 1 | 1 | 0 | TRAIO/$\overline{\text{INT1}}$ input (1) |
| | X | X | 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | X | X | TRAIO pulse output (2) |

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR5 bit in the P1DRR register to 1.

**Table 7.11 Port P1_6/CLK0/IVREF1**

| Register | PD1 | U0SR | U0MR | | | | INTCMP | Function |
|---|---|---|---|---|---|---|---|---|
| Bit | PD1_6 | CLK0SEL0 | SMD | | | CKDIR | INT1CP0 | |
| | | | 2 | 1 | 0 | | | |
| Setting Value | 0 | 0 | X | X | X | X | X | Input port (1) |
| | 1 | 0 | X | X | X | X | X | Output port (2) |
| | 0 | 1 | X | X | X | 1 | X | CLK0 (external clock) input (1) |
| | X | 1 | 0 | 0 | 1 | 0 | X | CLK0 (internal clock) output (2) |
| | 0 | 0 | X | X | X | X | 1 | Comparator B1 reference voltage input (IVREF1) |

X: 0 or 1

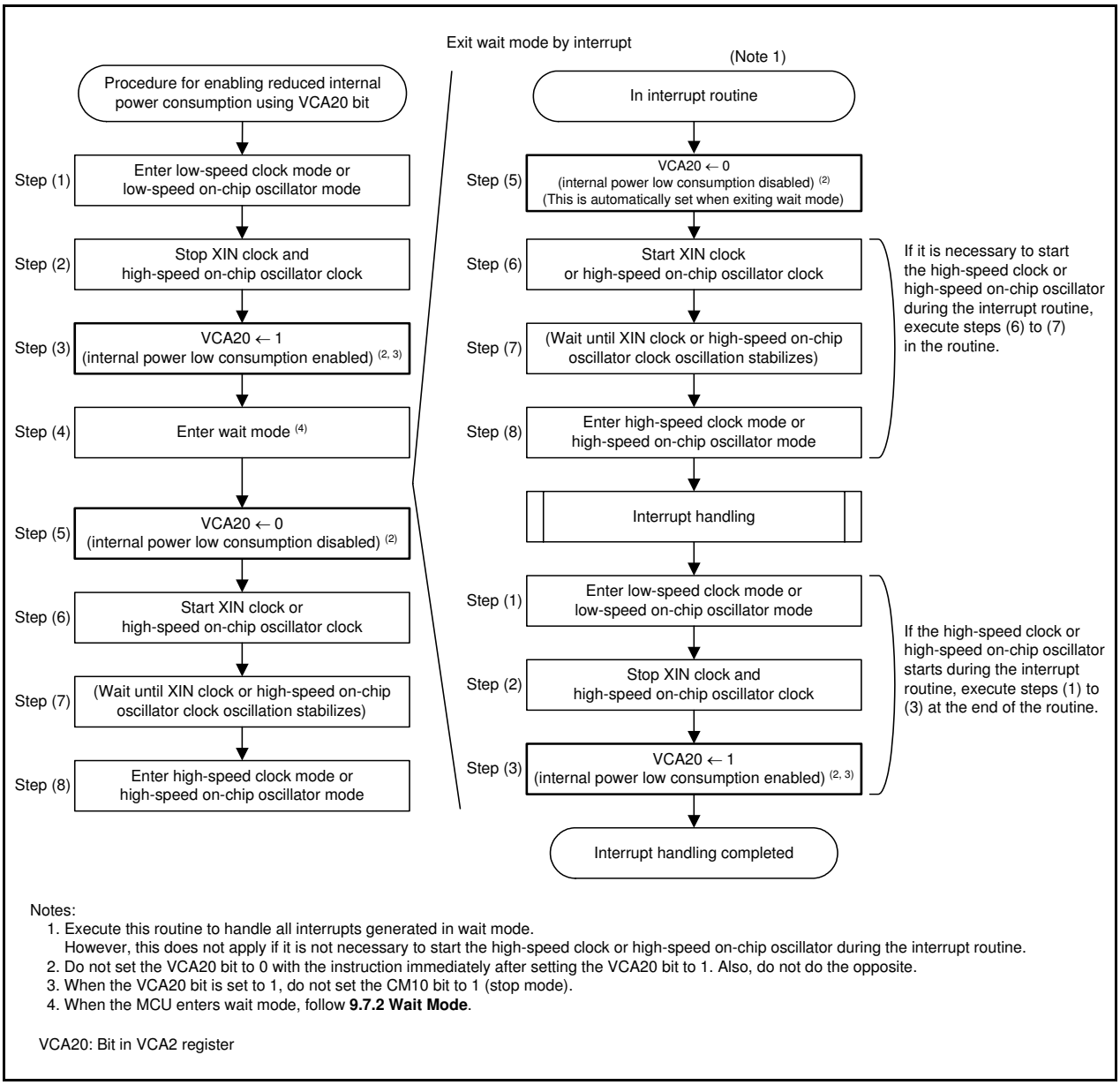
Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR6 bit in the P1DRR register to 1.

**Table 7.12 Port P1_7/$\overline{\text{INT1}}$/TRAIO/IVCMP1**

| Register | PD1 | TRASR | | TRAIOC | TRAMR | | | INTSR | | | INTEN | INTCMP | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | PD1_7 | TRAIOSEL | | TOPCR | TMOD | | | INT1SEL | | | INT1EN | INT1CP0 | |
| | | 1 | 0 | | 2 | 1 | 0 | 2 | 1 | 0 | | | |
| Setting Value | 0 | Other than 01b | | X | X | X | X | X | X | X | X | X | Input port (1) |
| | 1 | Other than 01b | | X | X | X | X | X | X | X | X | X | Output port (2) |
| | 0 | 0 | 1 | 0 | Other than 000b, 001b | | | X | X | X | X | X | TRAIO input (1) |
| | 0 | Other than 01b | | X | X | X | X | 0 | 0 | 0 | 1 | 0 | $\overline{\text{INT1}}$ input (1) |
| | 0 | 0 | 1 | 0 | Other than 000b, 001b | | | 0 | 0 | 0 | 1 | 0 | TRAIO/$\overline{\text{INT1}}$ input (1) |
| | X | 0 | 1 | 0 | 0 | 0 | 1 | X | X | X | X | X | TRAIO pulse output (2) |
| | 0 | Other than 01b | | X | X | X | X | X | X | X | 1 | 1 | Comparator B1 input (IVCMP1) |

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR7 bit in the P1DRR register to 1.




Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **9.7.2 Wait Mode**.

VCA20: Bit in VCA2 register

**Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit**

## 11.2 Registers

### 11.2.1 Interrupt Control Register (TREIC, S2TIC, S2RIC, KUPIC, ADIC, S0TIC, S0RIC, TRAIC, TRBIC, U2BCNIC, VCMP1IC, VCMP2IC)

Address 004Ah (TREIC), 004Bh (S2TIC), 004Ch (S2RIC), 004Dh (KUPIC), 004Eh (ADIC), 0051h (S0TIC), 0052h (S0RIC), 0056h (TRAIC), 0058h (TRBIC), 005Eh (U2BCNIC), 0072h (VCMP1IC), 0073h (VCMP2IC),

| Bit | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | — | — | — | — | IR | ILVL2 | ILVL1 | ILVL0 |
| After Reset | X | X | X | X | X | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Function | R/W |
|---|---|---|---|---|
| b0 | ILVL0 | Interrupt priority level select bit | b2 b1 b0<br>0 0 0: Level 0 (interrupt disabled)<br>0 0 1: Level 1<br>0 1 0: Level 2<br>0 1 1: Level 3<br>1 0 0: Level 4<br>1 0 1: Level 5<br>1 1 0: Level 6<br>1 1 1: Level 7 | R/W<br>R/W<br>R/W |
| b1 | ILVL1 | | | |
| b2 | ILVL2 | | | |
| b3 | IR | Interrupt request bit | 0: No interrupt requested<br>1: Interrupt requested | R/W (1) |
| b4 | — | Nothing is assigned. If necessary, set to 0.<br>When read, the content is undefined. | | — |
| b5 | — | | | |
| b6 | — | | | |
| b7 | — | | | |

Note:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.8.5 Rewriting Interrupt Control Register**.

### 11.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt.
Figure 11.8 shows the Interrupt Priority Level Selection Circuit.

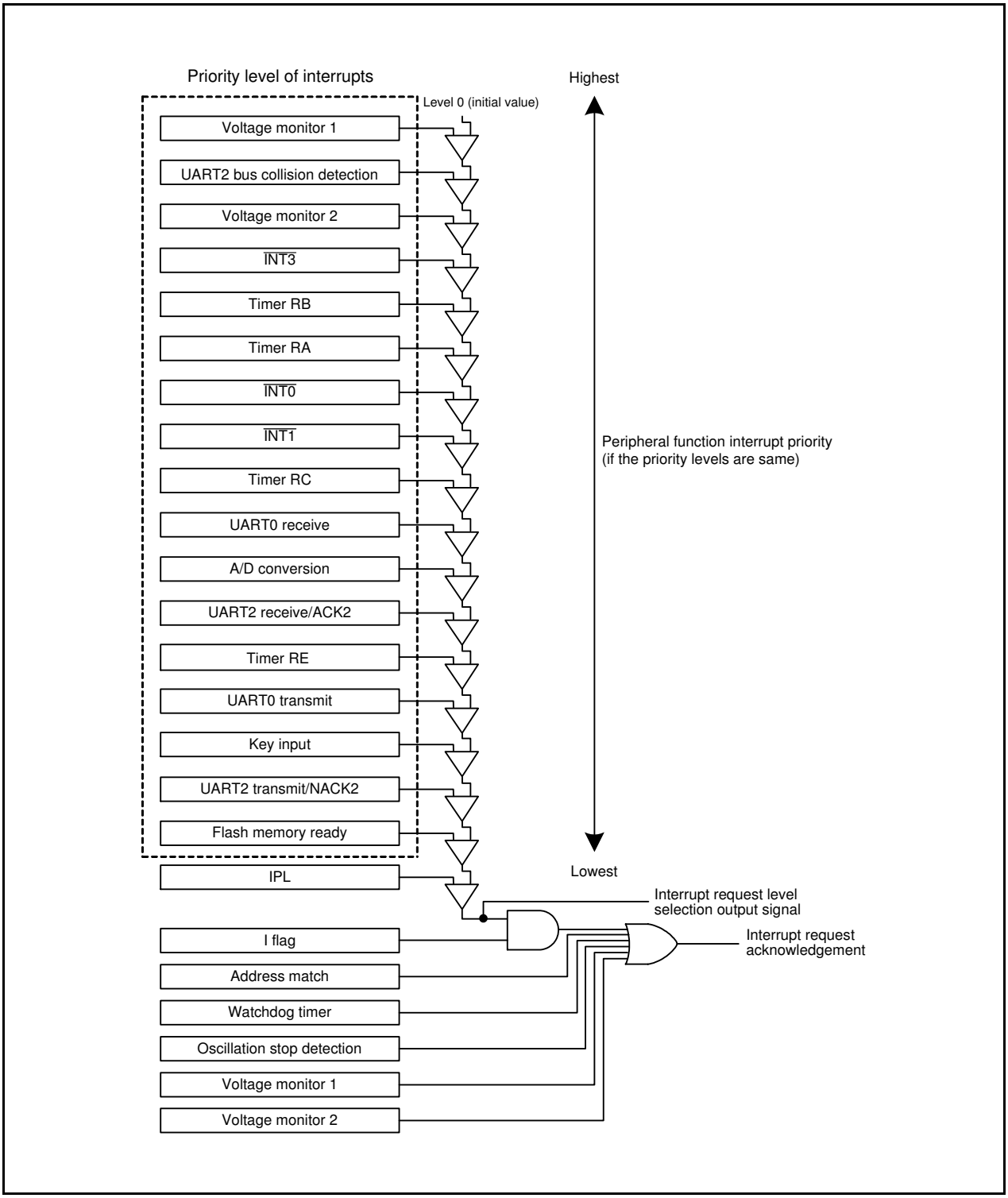



**Figure 11.8 Interrupt Priority Level Selection Circuit**

# 14. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

## 14.1 Overview

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 14.1 lists the Watchdog Timer Specifications.
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 14.1 shows a Watchdog Timer Block Diagram.

**Table 14.1 Watchdog Timer Specifications**

| Item | Count Source Protection Mode Disabled | Count Source Protection Mode Enabled |
|---|---|---|
| Count source | CPU clock | Low-speed on-chip oscillator clock for the watchdog timer |
| Count operation | Decrement | |
| Count start condition | Either of the following can be selected:<br>• After a reset, count starts automatically.<br>• Count starts by writing to the WDTS register. | |
| Count stop condition | Stop mode, wait mode | None |
| Watchdog timer initialization conditions | • Reset<br>• Write 00h and then FFh to the WDTR register (with acknowledgement period setting). (1)<br>• Underflow | |
| Operations at underflow | Watchdog timer interrupt or watchdog timer reset | Watchdog timer reset |
| Selectable functions | • Division ratio of the prescaler<br>Selected by the WDTC7 bit in the WDTC register or the CM07 bit in the CM0 register.<br>• Count source protection mode<br>Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory).<br>If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program).<br>• Start or stop of the watchdog timer after a reset<br>Selected by the WDTON bit in the OFS register (flash memory).<br>• Initial value of the watchdog timer<br>Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register.<br>• Refresh acknowledgement period for the watchdog timer<br>Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register. | |

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

# 16. Timer RA

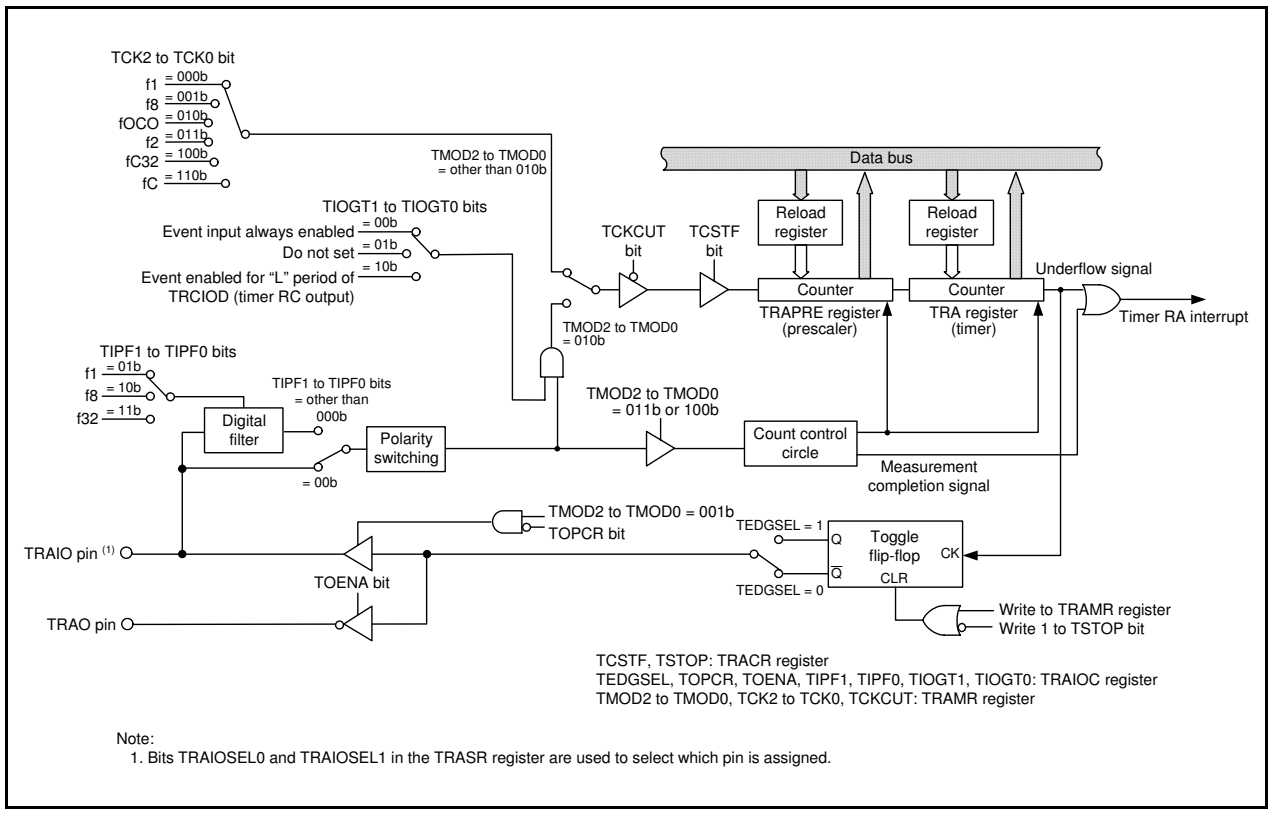
Timer RA is an 8-bit timer with an 8-bit prescaler.

## 16.1 Overview

The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA (refer to **Tables 16.2 to 16.6 the Specification of Each Modes**).
The count source for timer RA is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 16.1 shows a Timer RA Block Diagram. Table 16.1 lists Pin Configuration of Timer RA.

Timer RA contains the following five operating modes:

- Timer mode: The timer counts the internal count source.
- Pulse output mode: The timer counts the internal count source and outputs pulses which invert the polarity by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.




Note:
1. Bits TRAIOSEL0 and TRAIOSEL1 in the TRASR register are used to select which pin is assigned.

**Figure 16.1 Timer RA Block Diagram**

**Table 16.1 Pin Configuration of Timer RA**

| Pin Name | Assigned Pin | I/O | Function |
|---|---|---|---|
| TRAIO | P1_5 or P1_7 | I/O | Function differs according to the mode. Refer to descriptions of individual modes for details |
| TRAO | P3_7 | Output | |

## 16.4 Pulse Output Mode

In pulse output mode, the internally generated count source is counted, and a pulse with inverted polarity is output from the TRAIO pin each time the timer underflows (refer to **Table 16.3 Pulse Output Mode Specifications**).

**Table 16.3 Pulse Output Mode Specifications**

| Item | Specification |
|---|---|
| Count sources | f1, f2, f8, fOCO, fC32, fC |
| Count operations | • Decrement<br>• When the timer underflows, the contents in the reload register is reloaded and the count is continued. |
| Divide ratio | 1/(n+1)(m+1)<br>n: Value set in TRAPRE register, m: Value set in TRA register |
| Count start condition | 1 (count starts) is written to the TSTART bit in the TRACR register. |
| Count stop conditions | • 0 (count stops) is written to the TSTART bit in the TRACR register.<br>• 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register. |
| Interrupt request generation timing | When timer RA underflows [timer RA interrupt]. |
| TRAIO pin function | Pulse output, programmable output port |
| TRAO pin function | Programmable I/O port or inverted output of TRAIO |
| Read from timer | The count value can be read by reading registers TRA and TRAPRE. |
| Write to timer | • When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter.<br>• When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **16.3.2 Timer Write Control during Count Operation**). |
| Selectable functions | • TRAIO signal polarity switch function<br>The level when the pulse output starts is selected by the TEDGSEL bit in the TRAIOC register. (1)<br>• TRAO output function<br>Pulses inverted from the TRAIO output polarity can be output from the TRAO pin (selectable by the TOENA bit in the TRAIOC register).<br>• Pulse output stop function<br>Output from the TRAIO pin is stopped by the TOPCR bit in the TRAIOC register.<br>• TRAIO pin select function<br>P1_5 or P1_7 is selected by bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register. |

Note:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

### 18.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register for the TRCGRA or TRCGRB register.

- Buffer register for TRCGRA register: TRCGRC register
- Buffer register for TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

Table 18.6 lists the Buffer Operation in Each Mode, Figure 18.3 shows the Buffer Operation for Input Capture Function, and Figure 18.4 shows the Buffer Operation for Output Compare Function.

**Table 18.6 Buffer Operation in Each Mode**

| Function, Mode | Transfer Timing | Transfer Destination Register |
|---|---|---|
| Input capture function | Input capture signal input | Contents of TRCGRA (TRCGRB) register are transferred to buffer register |
| Output compare function<br>PWM mode | Compare match between TRC register and TRCGRA (TRCGRB) register | Contents of buffer register are transferred to TRCGRA (TRCGRB) register |
| PWM2 mode | • Compare match between TRC register and TRCGRA register<br>• TRCTRG pin trigger input | Contents of buffer register (TRCGRD) are transferred to TRCGRB register |

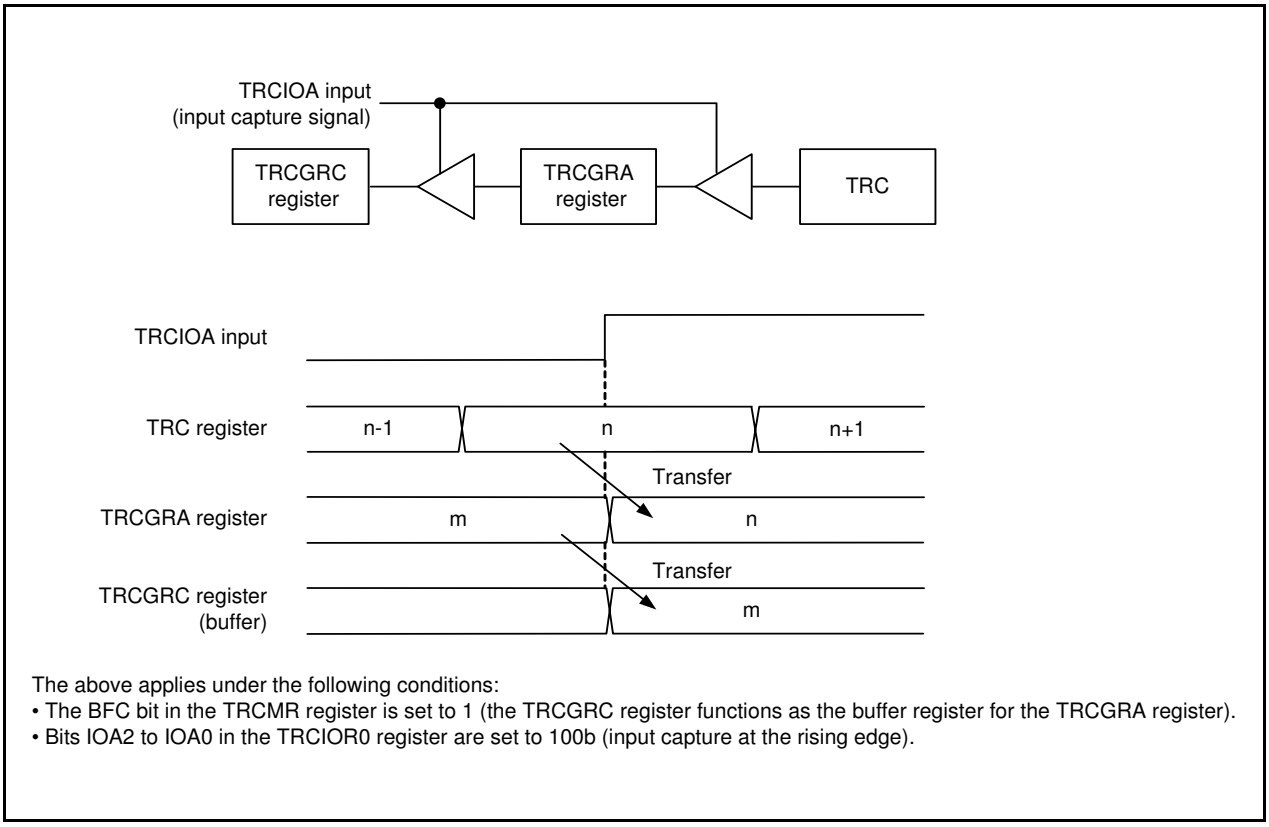



**Figure 18.3 Buffer Operation for Input Capture Function**

### 18.5.6 Changing Output Pins in Registers TRCGRC and TRCGRD

The TRCGRC register can be used for output control of the TRCIOA pin, and the TRCGRD register can be used for output control of the TRCIOB pin. Therefore, each pin output can be controlled as follows:

- TRCIOA output is controlled by the values in registers TRCGRA and TRCGRC.
- TRCIOB output is controlled by the values in registers TRCGRB and TRCGRD.

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and set the IOD3 bit to 0 (TRCIOB output register).
- Set bits BFC and BFD in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRC and TRCGRA. Also, set different values in registers TRCGRD and TRCGRB.

Figure 18.12 shows an Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin.

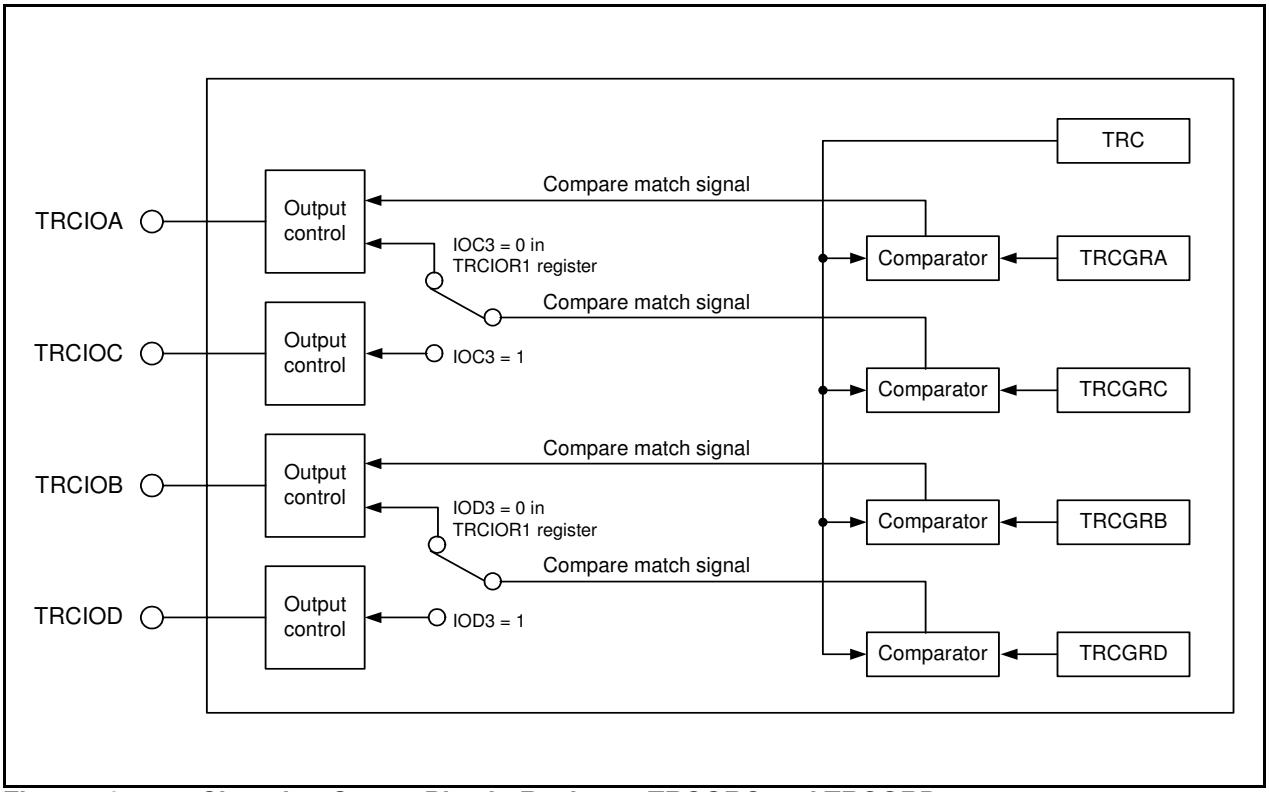



**Figure 18.11 Changing Output Pins in Registers TRCGRC and TRCGRD**

### 20.3.2 Polarity Select Function

Figure 20.4 shows the Transfer Clock Polarity. Use the CKPOL bit in the U0C0 register to select the transfer clock polarity.

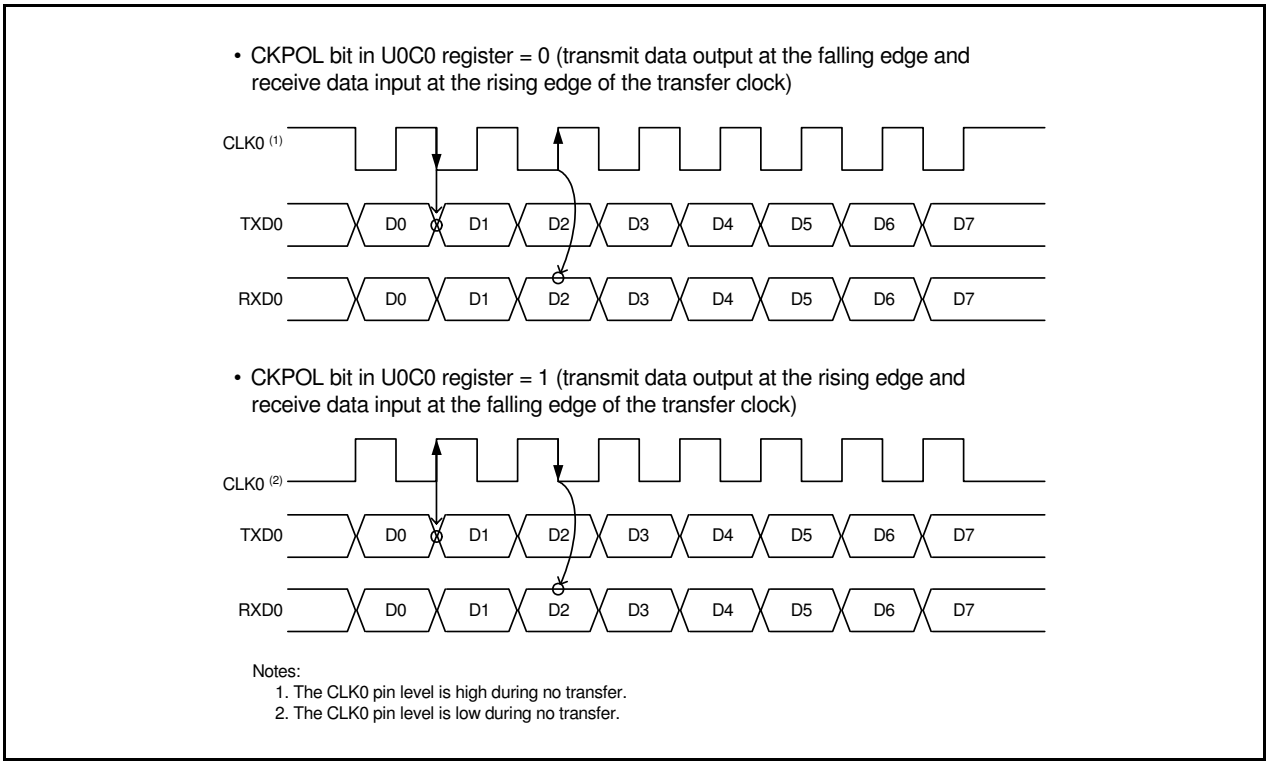



**Figure 20.4 Transfer Clock Polarity**

### 20.3.3 LSB First/MSB First Select Function

Figure 20.5 shows the Transfer Format. Use the UFORM bit in the U0C0 register to select the transfer format.

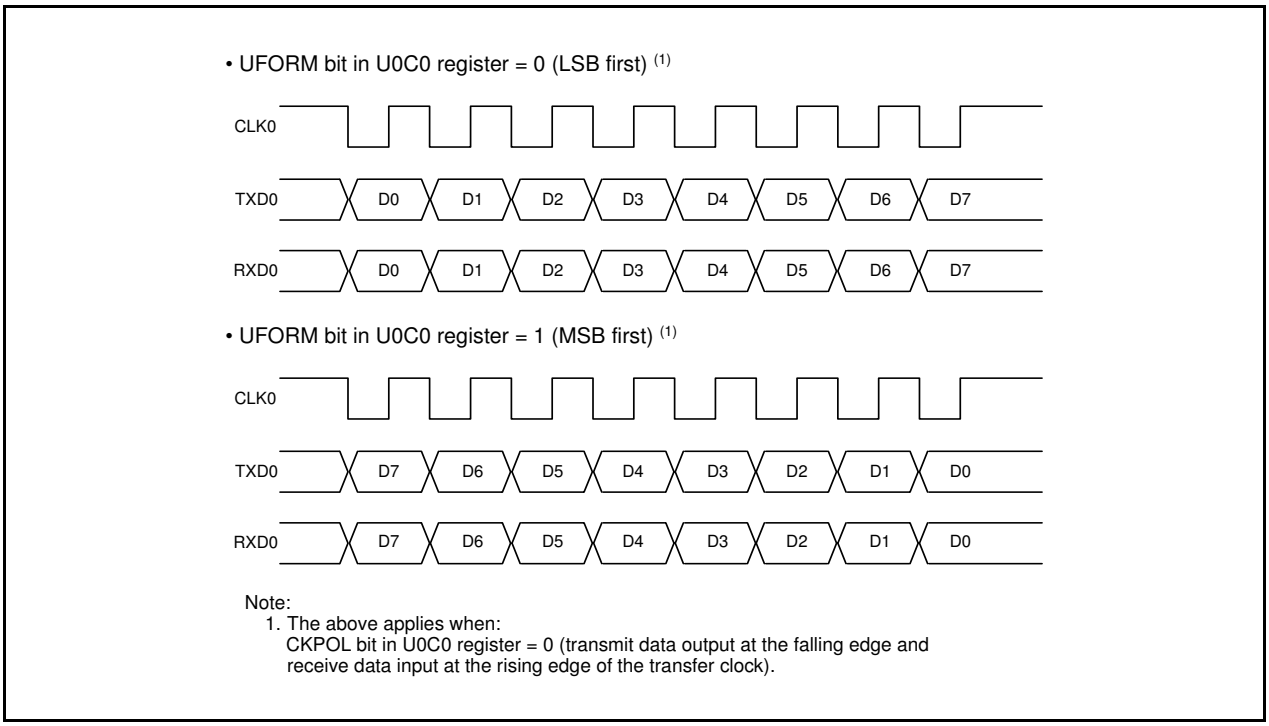
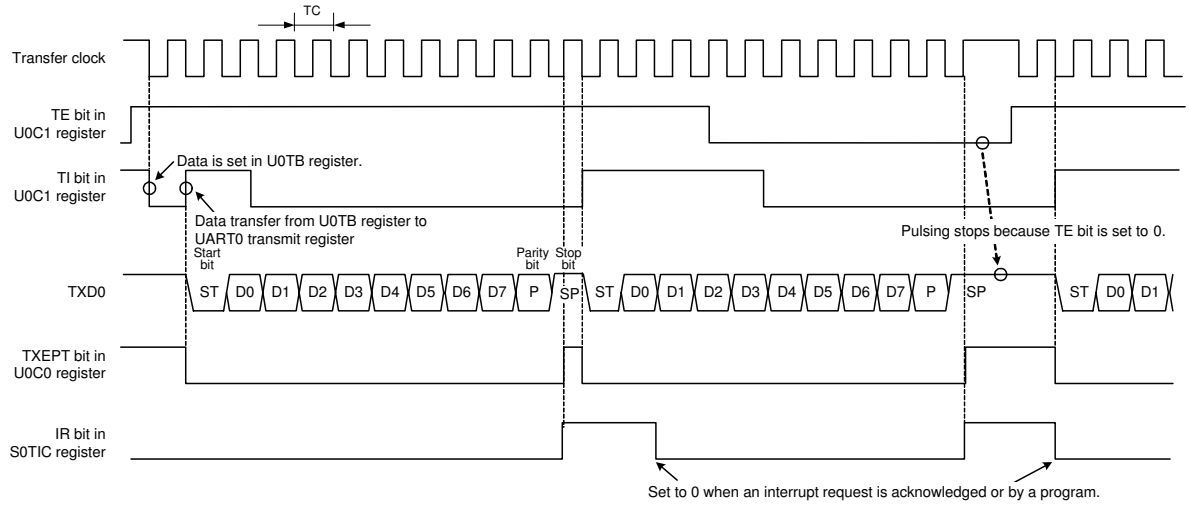



**Figure 20.5 Transfer Format**

### 20.3.4 Continuous Receive Mode

Continuous receive mode is selected by setting the U0RRM bit in the U0C1 register to 1 (continuous receive mode enabled). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to 0 (data present in the U0TB register). If the U0RRM bit is set to 1, do not write dummy data to the U0TB register by a program.

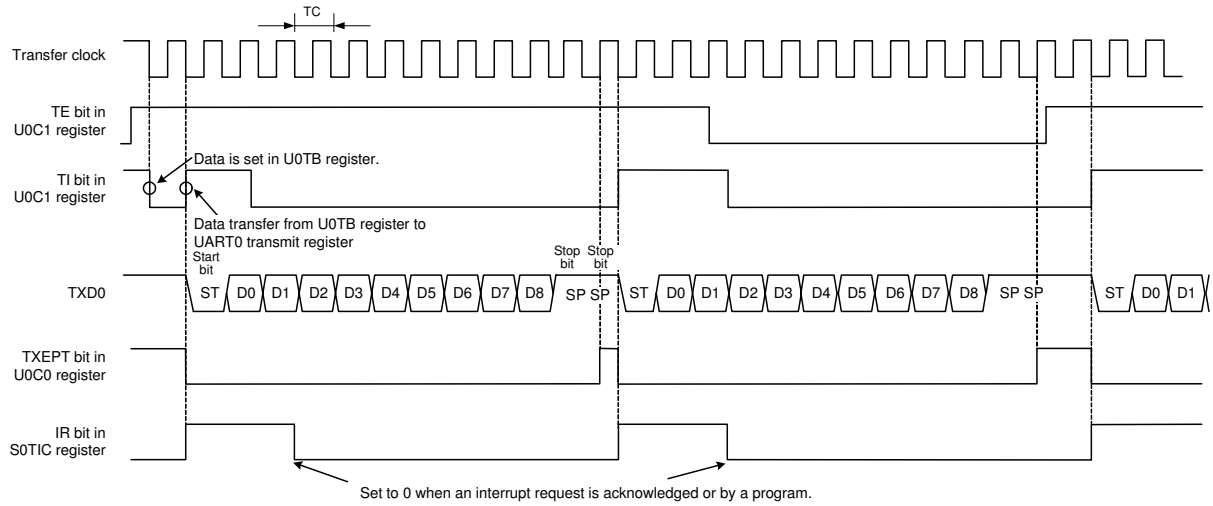
• Transmit Timing Example When Transfer Data 8 Bits is Long (Parity Enabled, One Stop Bit)




The above applies when:
- PRYE bit in U0MR register = 1 (parity enabled)
- STPS bit in U0MR register = 0 (one stop bit)
- U0IRS bit in U0C1 register = 1
  (interrupt request generation when transmission is completed)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of U0BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U0BRG count source (external clock)
n: Setting value in U0BRG register

• Transmit Timing Example When Transfer Data is 9 Bits Long (Parity Disabled, Two Stop Bits)




The above applies when:
- PRYE bit in U0MR register = 0 (parity disabled)
- STPS bit in U0MR register = 1 (two stop bits)
- U0IRS bit in U0C1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of U0BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U0BRG count source (external clock)
n: Setting value in U0BRG register

**Figure 20.6 Transmit Timing in UART Mode**

Table 21.4 lists the Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected).
Note that for a period from when UART2 operating mode is selected to when transfer starts, the TXD2 pin outputs a “H” level. (When N-channel open-drain output is selected, this pin is in the high-impedance state.)
Figure 21.3 shows the Transmit and Receive Timing in Clock Synchronous Serial I/O Mode.

**Table 21.4 Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected)**

| Pin Name | Function | Selection Method |
|---|---|---|
| TXD2 (P3_4 or P3_7) | Serial data output | • TXD2 (P3_4)<br>Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 10b (P3_4)<br>• TXD2 (P3_7)<br>Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 01b (P3_7)<br>• For reception only:<br>P3_4 and P3_7 can be used as ports by setting TXD2SEL1 to TXD2SEL0 to 00b. |
| RXD2 (P3_4, P3_7, or P4_5) | Serial data input | • RXD2 (P3_4)<br>Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 01b (P3_4)<br>PD3_4 bit in PD3 register = 0<br>• RXD2 (P3_7)<br>Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 10b (P3_7)<br>PD3_7 bit in PD3 register = 0<br>• RXD2 (P4_5)<br>Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 11b (P4_5)<br>PD4_5 bit in PD4 register = 0<br>• For transmission only:<br>P3_4, P3_7, and P4_5 can be used as ports by setting RXD2SEL1 to RXD2SEL0 to 00b. |
| CLK2 (P3_5) | Transfer clock output | CLK2SEL0 bit in U2SR1 register = 1<br>CKDIR bit in U2MR register = 0 |
| | Transfer clock input | CLK2SEL0 bit in U2SR1 register = 1<br>CKDIR bit in U2MR register = 1<br>PD3_5 bit in PD3 register = 0 |
| $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ (P3_3) | $\overline{\text{CTS}}$ input | CTS2SEL0 bit in U2SR1 register = 1<br>CRD bit in U2C0 register = 0<br>CRS bit in U2C0 register = 0<br>PD3_3 bit in PD3 register = 0 |
| | $\overline{\text{RTS}}$ output | CTS2SEL0 bit in U2SR1 register = 1<br>CRD bit in U2C0 register = 0<br>CRS bit in U2C0 register = 1 |
| | I/O port | CTS2SEL0 bit in U2SR1 register = 0 |

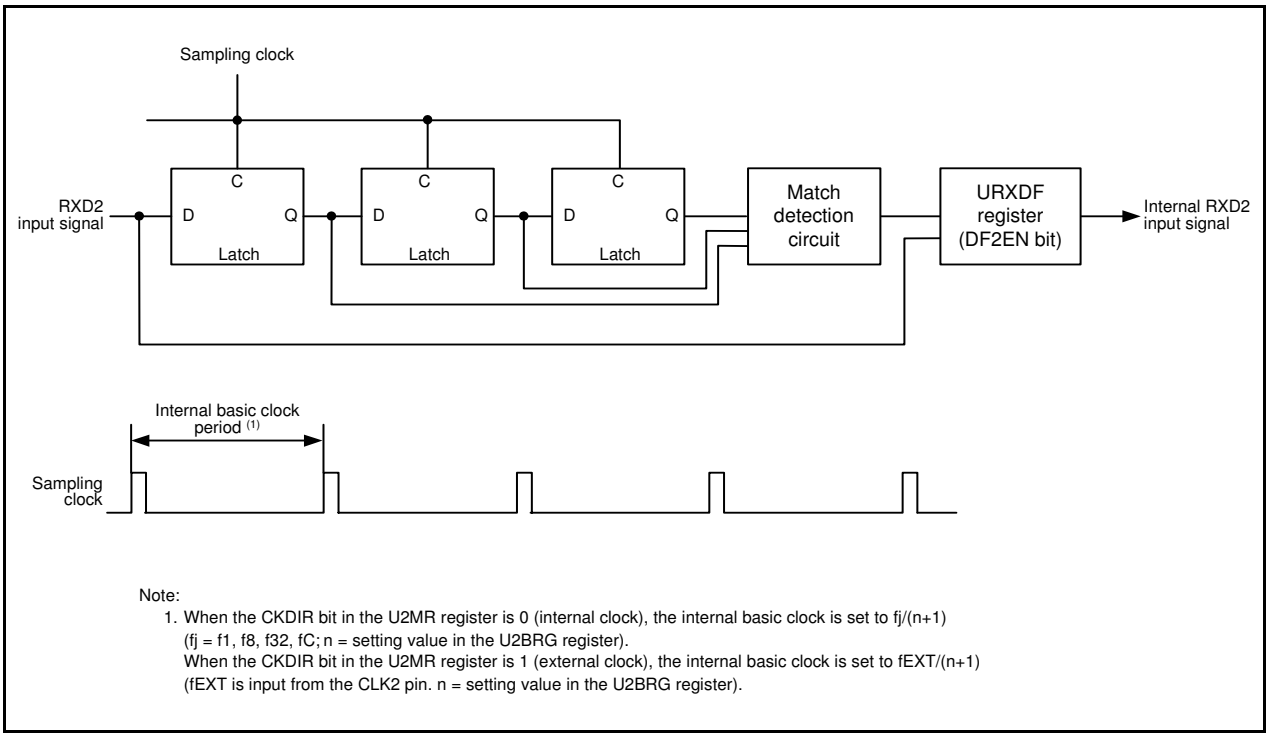
### 21.4.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit operation when "L" is applied to the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin. Transmit operation begins when the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin is held low. If the "L" signal is switched to "H" during transmit operation, the operation stops after the ongoing transmit/receive operation is completed.
When the $\overline{\text{RTS}}$ function is used, the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin outputs "L" when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the CLK2 pin.

- The CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{CTS}}$ function.
- The CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{RTS}}$ function.

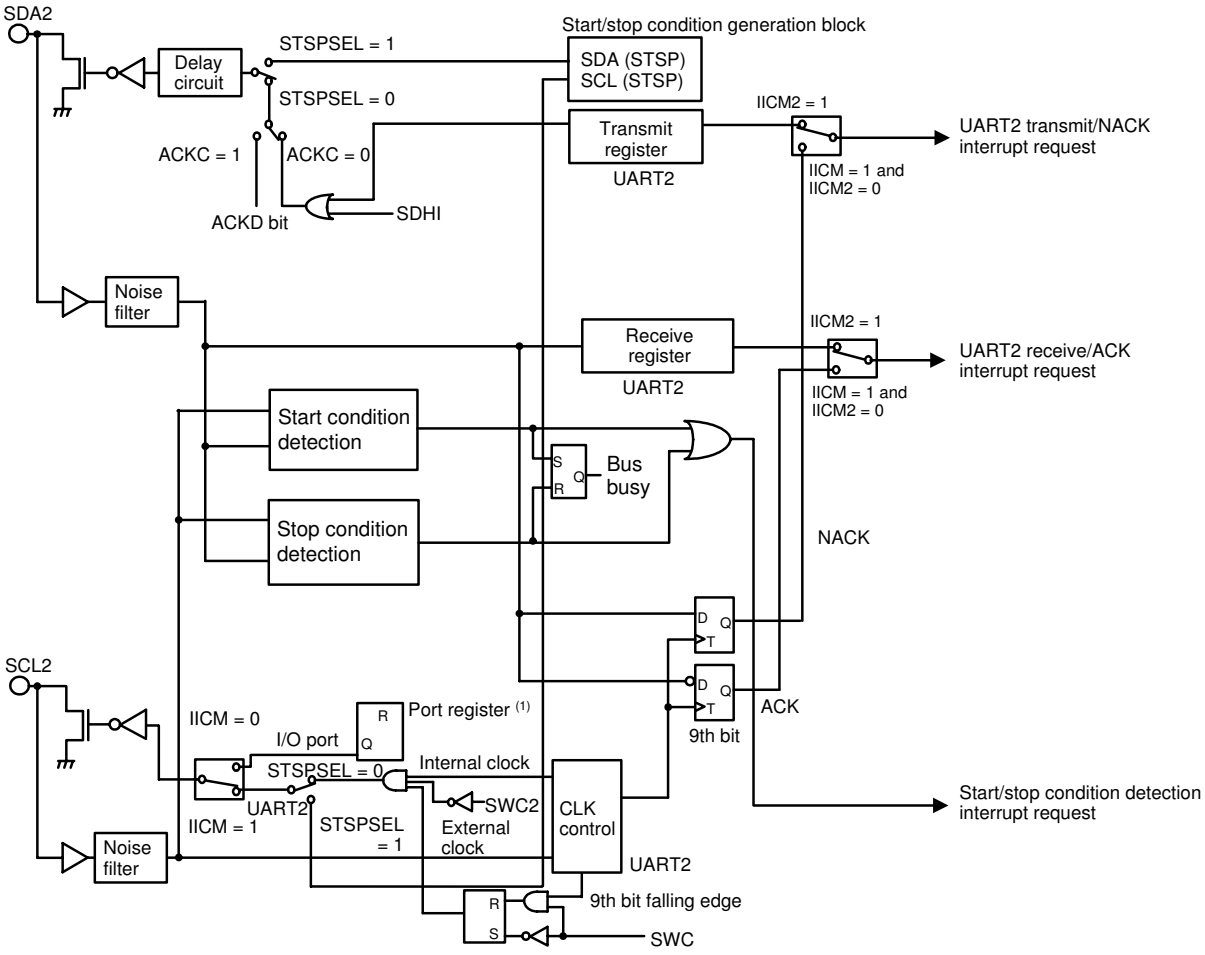
### 21.4.7 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filer enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the internal basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.
In other words, when the level is changed within three clocks, the change is recognized as not a signal but noise.
Figure 21.12 shows a Block Diagram of RXD2 Digital Filter Circuit.




Note:
1. When the CKDIR bit in the U2MR register is 0 (internal clock), the internal basic clock is set to fj/(n+1)
(fj = f1, f8, f32, fC; n = setting value in the U2BRG register).
When the CKDIR bit in the U2MR register is 1 (external clock), the internal basic clock is set to fEXT/(n+1)
(fEXT is input from the CLK2 pin. n = setting value in the U2BRG register).

**Figure 21.12 Block Diagram of RXD2 Digital Filter Circuit**




IICM: Bit in U2SMR register
IICM2, SWC, SWC2, SDHI: Bits in U2SMR2 register
STSPSEL, ACKD, ACKC: Bits in U2SMR4 register

The above applies when:
- Bits SMD2 to SMD0 in U2MR register = 010b
- IICM bit in U2SMR register = 1

Note:
If the IICM bit is set to 1, the pin can be read even when the port direction bit corresponding to the SCL2 pin is set to 1 (output mode).

**Figure 21.13 I²C Mode Block Diagram**

## 24.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.
The flash module has an erase-suspend function which halts the erase operation temporarily during an erase operation in CPU rewrite mode. During erase-suspend, the flash memory can be read or programmed.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 24.3 lists the Differences between EW0 Mode and EW1 Mode.

**Table 24.3 Differences between EW0 Mode and EW1 Mode**

| Item | EW0 Mode | EW1 Mode |
|---|---|---|
| Operating mode | Single-chip mode | Single-chip mode |
| Rewrite control program allocatable area | User ROM | User ROM |
| Rewrite control program executable areas | RAM (The rewrite control program must be transferred before being executed.) | User ROM or RAM |
| Rewritable area | User ROM | User ROM<br>However, blocks which contain the rewrite control program are excluded. |
| Software command restrictions | — | Program and block erase commands<br>Cannot be executed to any block which contains the rewrite control program. |
| Mode after programming or block erasure or after entering erase-suspend | Read array mode | Read array mode |
| CPU state during programming and block erasure | The CPU operates. | The CPU is put in a hold state while the program ROM area is being programmed or block erased. (I/O ports retain the state before the command execution). |
| Flash memory status detection | Read bits FST7, FMT5, and FMT4 in the FST register by a program. | Read bits FST7, FMT5, and FMT4 in the FST register by a program. |
| Conditions for entering erase-suspend | • Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program.<br>• Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated. | Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated. |
| CPU clock | Max. 20 MHz | Max. 20 MHz |

### FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)

When the FMR 22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) at the time an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when using erase-suspend while rewriting the user ROM area in EW1 mode.

### FMR27 Bit (Low-Current-Consumption Read Mode Enable Bit)

When the FMR 27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed clock mode (XIN clock stopped) or low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **25.2.10 Low-Current-Consumption Read Mode** for details.
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).